Network Synthesis Automates Interactive Matching Circuit Design

Reducing product development time requires design tools that support and expedite all stages of development, from translating performance requirements into an initial design through to optimization, physical realization, and final verification—all before fabrication and test. This paper examines new network synthesis design software for the development of impedance-matching circuits. This technology is used largely for RF/microwave applications to ensure that performance is optimized across the frequency band of interest. It can be used to establish the best possible conjugate match to the system impedance for a broadband antenna, synthesizing an output-matching network that enables a power amplifier (PA) to meet efficiency and power performance targets, or creating an input-matching network that gives the best possible noise figure across frequency for a low-noise amplifier (LNA).

This RF/microwave component design flow must offer design entry (most often schematic-based), nonlinear simulation, the ability to review results, the ability to generate physical (layout) design from the schematic, and support for electromagnetic (EM) analysis for characterization/verification of the electrical response of the physical design. The network synthesis tool should leverage this flow using device data that is incorporated in any given design project and generate networks in a schematic form that are recognizable to the simulator. Such a flow is offered in NI AWR Design Environment software, a leading platform used throughout the RF/microwave industry for nonlinear/linear circuit design of devices such as PAs, which provides engineers with capabilities to tackle design entry and simulation prior to manufacturing, while allowing a smooth transition to fabrication and test with minimal design iterations.

Complementing these capabilities are recent advances in design automation and initiatives in specialized design wizards such as load-pull analysis. The most recent V14 release of NI AWR software introduces network synthesis for the development of impedance matching networks, as shown in Figure 1. This latest functionality accelerates design starts and enables designers to more fully explore design options through the creation of optimized two-port matching networks with discrete and distributed components based on user-defined performance goals. Network synthesis is helpful at the beginning of a design to determine reasonable performance targets based on device performance limits, device sizing (decisions on active device periphery), part selection (for discrete packaged transistors), and other early design decisions.

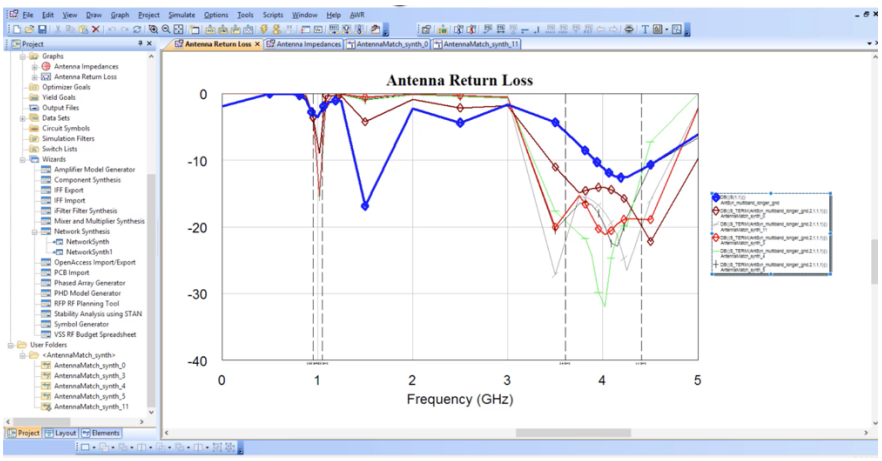

Figure 1: Network synthesis addresses multi-band matching challenges.

This new synthesis tool is particularly helpful for challenging broadband single- and multi-stage amplifiers and antenna/amplifier matching networks and is available as an add-on module. The tool also helps designers develop impedance-matching networks between front-end components. As the footprints of RF components shrink to meet market demand for smaller embedded radios in internet of things (IoT) smart devices (Figure 2), the network synthesis wizard helps designers save space, consolidating component-to-component matching networks by directly transforming the impedance between each component rather than to an intermediary characteristic impedance (such as 50 ohms).

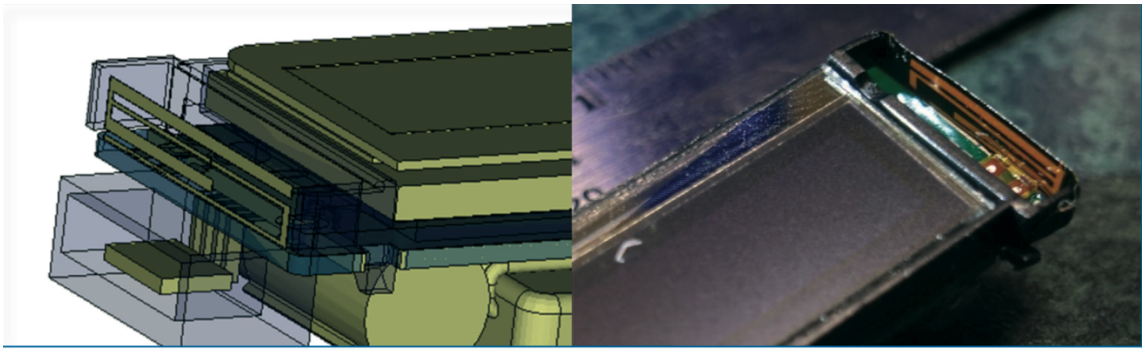

Figure 2: Embedded antenna and RF front-end in wireless wearable device (images courtesy of Striiv).

Networks can be optimized for noise, power, interstage conjugate, or single-stage conjugate matching. The optimum reflection coefficients are specified over frequency and can be provided in the form of

load-pull data, network parameter data files, or circuit schematics. Specifications for network topology include series and shunt component types and maximum number of sections. With a given set of user input specifications (performance requirements), the synthesis algorithm searches circuit topologies and optimizes component parameter values in order to generate candidate matching networks for power and LNAs, as well as inter-stage and inter-component impedance-matching networks.

The new network synthesis wizard is made possible with recent advances in computer processing power and the introduction of genetic algorithm methods, which have proven very effective at addressing circuit response problems. This technology leverages the algorithms employed within the AntSyn™ antenna design, synthesis, and optimization module (awrcorp.com/antsyn) and has nearly 10 years of development time, resulting in a rigorous optimizer. The optimizers use recombination and selection to rapidly and robustly explore a large number of points randomly distributed over the design space. This results in a more efficient and faster approach to investigating design possibilities and identifying optimum solutions.

The approach used by the search-based synthesis engine to determine candidate circuit topologies is based on input from the user-specification for the element types, such as capacitors, inductors, and transmission lines, that are to be used in the series and shunt slots. The synthesis tool then performs an exhaustive search, exploring all possible topologies by expanding the solution up to the maximum number of sections defined by the user, as shown in Figure 3. Heuristic methods are used to determine what element can follow an existing element. Through this self-learning process, the synthesizer understands that certain elements can be placed serially, such as two different width transmission lines to form a stepped-impedance transformer, or a fully-distributed transmission line network for higher frequencies. On the other hand, two serial capacitors would not make sense from a matching perspective and those search efforts are not pursued.

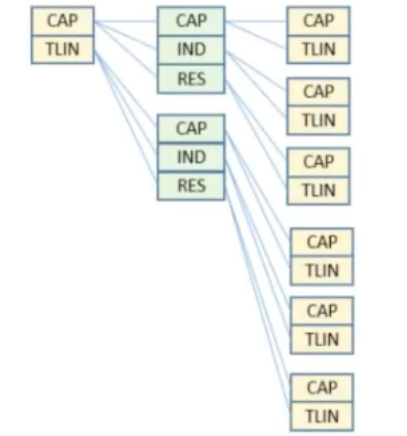

Figure 3: The search engine explores possible topologies by expanding the solution up to the maximum number of sections as defined by the user.

The optimization goals are specified in the wizard using a dedicated set of synthesis measurements, much like optimization goals are normally defined in the NI AWR Design Environment platform. Specialized measurements are provided for input noise matching, amplifier output power matching, and interstage matching.

Additional practical considerations coded into the synthesizer include the ability to constrain the DC open and short paths in the topology search. For instance, users can stipulate that the side of the matching circuit next to the device will be DC open, so as not to short the drain or collector. They can also stipulate minimum and maximum component limits and discrete values to reflect actual available (discrete) parts, and constraints can be placed on the first and last components in the network. This allows designers to ensure that the physical practicality of the synthesized network, such as designing a wide (low-impedance) transmission-line termination adjacent to a large periphery device. In addition, the impact of pre-existing bias or feed networks can be incorporated into the synthesis network. At the end of the synthesis, candidate networks can be sorted from best to worst, in terms of how well they address the performance goals.

The network synthesis user interface (UI) enables designers to interactively develop an unlimited number of networks optimized for noise, power, or matching networks between amplifier stages or between different components, such as an amplifier and an antenna. The optimum reflection coefficients are specified over frequency and can be provided in the form of load-pull data, network

parameter data files, or circuit schematics. Within the synthesis definition tab (Figure 4), users can specify a default impedance or the impedance of the desired source/load network as well as the desired match frequencies.

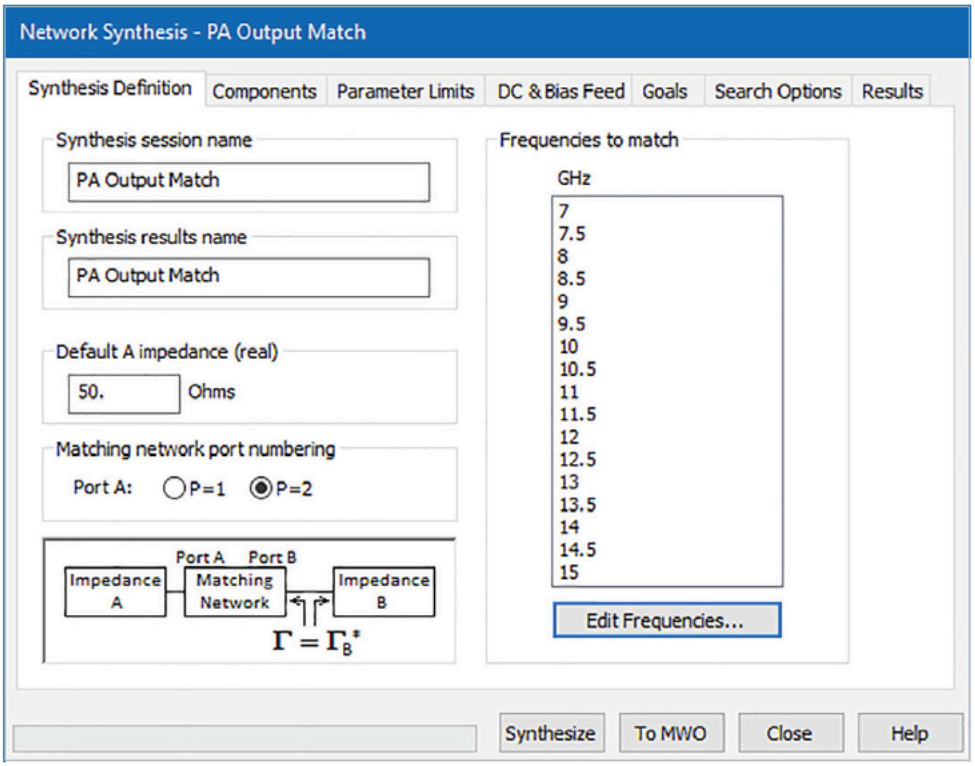

Figure 4: The synthesis definition dialog allows users to specify basic network parameters, including circuit location among networks to be matched, port numbering and frequency band

The wizard lets users specify the target network (or two target networks in the case of interstage problems) to be matched from an automatically populated list of project networks (schematics), and also allows them to set certain constraints on the matching network, including the number of sections, topology, component type, and configuration (series/shunt). Valid topologies are determined by the types of components selected and the value specified for the maximum number of sections. Each section is either a series component or a shunt component. The wizard considers topologies having the maximum number of sections, N, and fewer, as previously mentioned.

Load-Pull Example

The synthesizer is able to interface directly with load-pull data within Microwave Office software for the instances where designers want to development matching networks based on nonlinear, load-sensitive

performance data. For example, the locus of impedances resulting in power-added efficiency (PAE) and power contours over a given frequency range are plotted on a 5-ohm Smith chart (63 percent PAE and 51 dBm (~125 watts) at the 1 dB gain compression point, five frequencies from 1.8 to 2.0 GHz), as shown in Figure 5. Alternatively, the designers could plot the overlapping contours, which represent the intersection of the PAE and power capability contours, as shown on the right side of Figure 5.

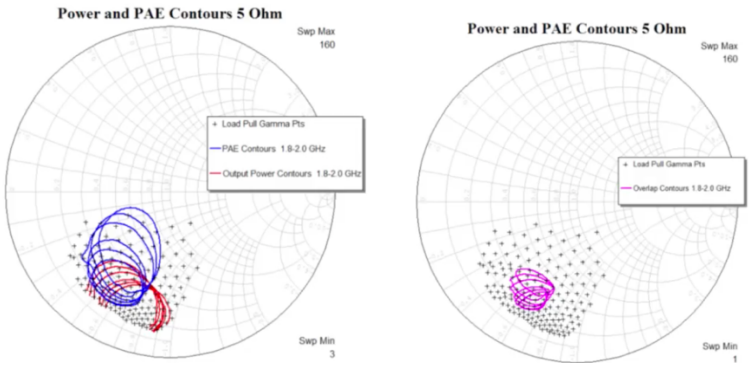

Figure 5: Load-pull contours for power and PAE (left), as well as the intersection of these contours (right), which will be provide the impedance targets for the network synthesizer.

Instead of providing impedance goals, designers can optionally specify load-pull results from directly within Microwave Office software. The user simply needs to stipulate the goals, in this case 63-percent PAE and 51 dBm output power, instead of a specific impedance for each frequency point. In this instance, the automation built into the synthesizer tool works from performance goals rather than impedances, which is a much more intuitive approach. The synthesizer provides this capability for sub-bands in support of multi-band matching networks. Goals can be weighted differently, with all the available functionality that is built into the Microwave Office optimizer, such as sloped goals, being supported by the network synthesizer as well.

Additional goals that aren't load-pull based can also be added. Figure 6 shows the overlap load-pull contours versus frequency and the initial synthesized matching network which follows the frequency trajectory of the contours over the desired bandwidth. User-specified target goals can be added to address harmonic terminations to improve linearity and efficiency. Extending the frequency range of the analysis shows that the synthesizer has generated a matching network to provide the desired impedance at the targeted fundamental frequencies as well as the second and third harmonic frequencies.

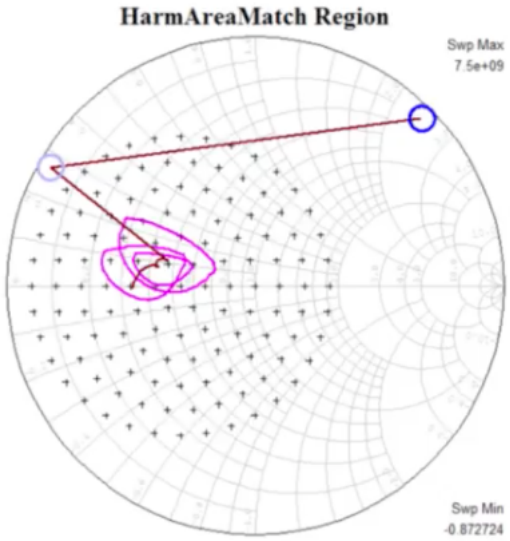

Figure 6: PAE/power overlap load-pull contours at three fundamental frequencies and user-defined additional goals for second and third harmonic terminations with resulting network-synthesis-generated matching circuit.

Post-Synthesis Review

At the end of the synthesizer run, a user-defined number of candidate networks will be generated. This provides the designer with an easy and quick method to compare performance results for each network along with a pictogram of the generated layout to provide a visual aid to the designer, as shown in Figure 7.

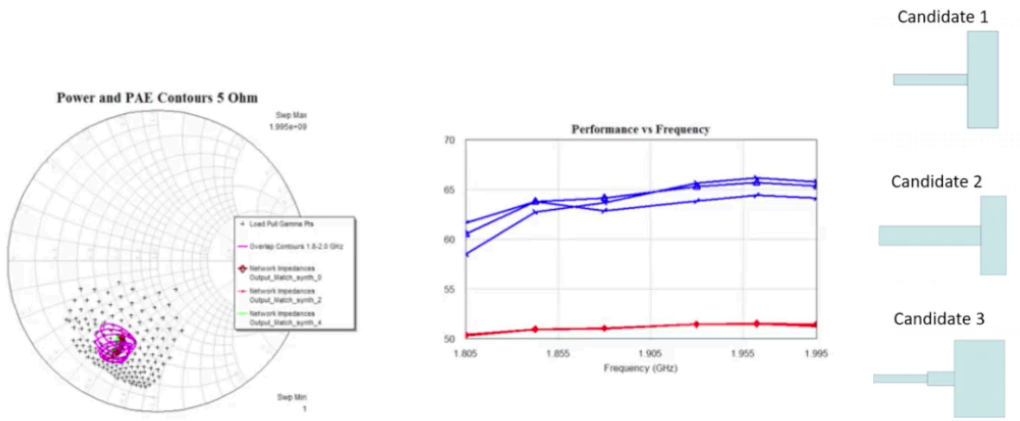

Figure 7: Candidate matching networks and corresponding performance provide users with a method to compare different results and help select the most appropriate circuit.

Conclusion

To help expedite the entire design cycle, a new network synthesis wizard has been added to NI AWR software for the generation of impedance-matching circuits. The synthesis tool generates candidate networks based on user-defined goals, suggested element types to be utilized in the topology search, element constraints/limits, and more. The search engine explores possible topologies by expanding the solution up to the maximum number of sections as defined by the user.