Designing and Measuring 100uOhm Power Rails

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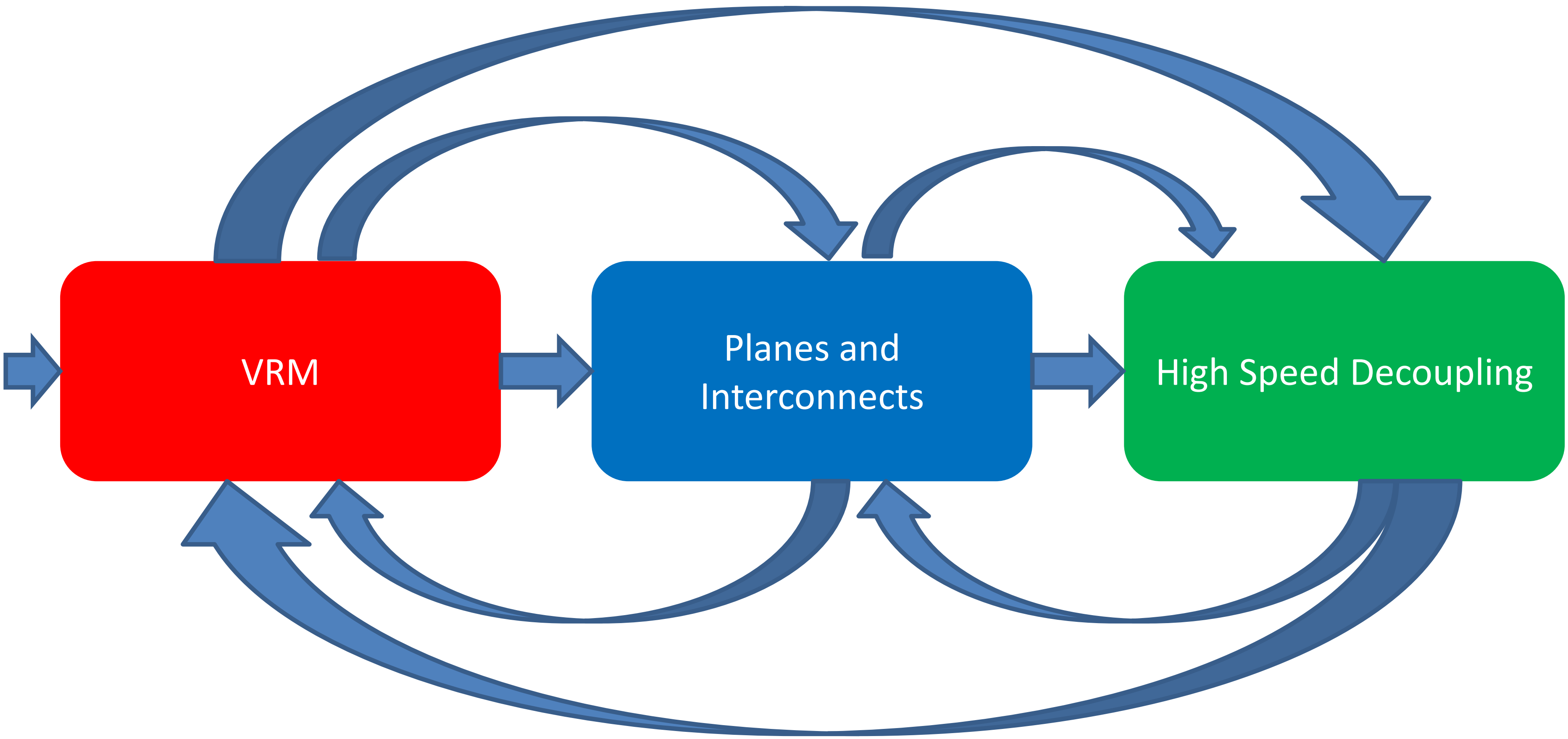

VRM
Planes and Interconnects
High Speed Decoupling

$$Rail\ Noise = \sum All\ noise\ sources$$

$$\Delta V_{out} = \Delta V_{DC} + \Delta V_{Ripple} + \Delta I_{load} \cdot R_{target} + \frac{\Delta V_{in}}{PSRR}$$

$$R_{target} = \frac{\Delta V_{out} - \ \Delta V_{DC} - \Delta V_{Ripple} - \frac{\Delta V_{in}}{PSRR}}{\Delta I_{load}}$$

$$Z_{target(f)} = \frac{\Delta V_{out}(f) - \ \Delta V_{DC} - \Delta V_{Ripple}(f) - \frac{\Delta V_{in}(f)}{PSRR\ (f)}}{\Delta I_{load}(f)}$$

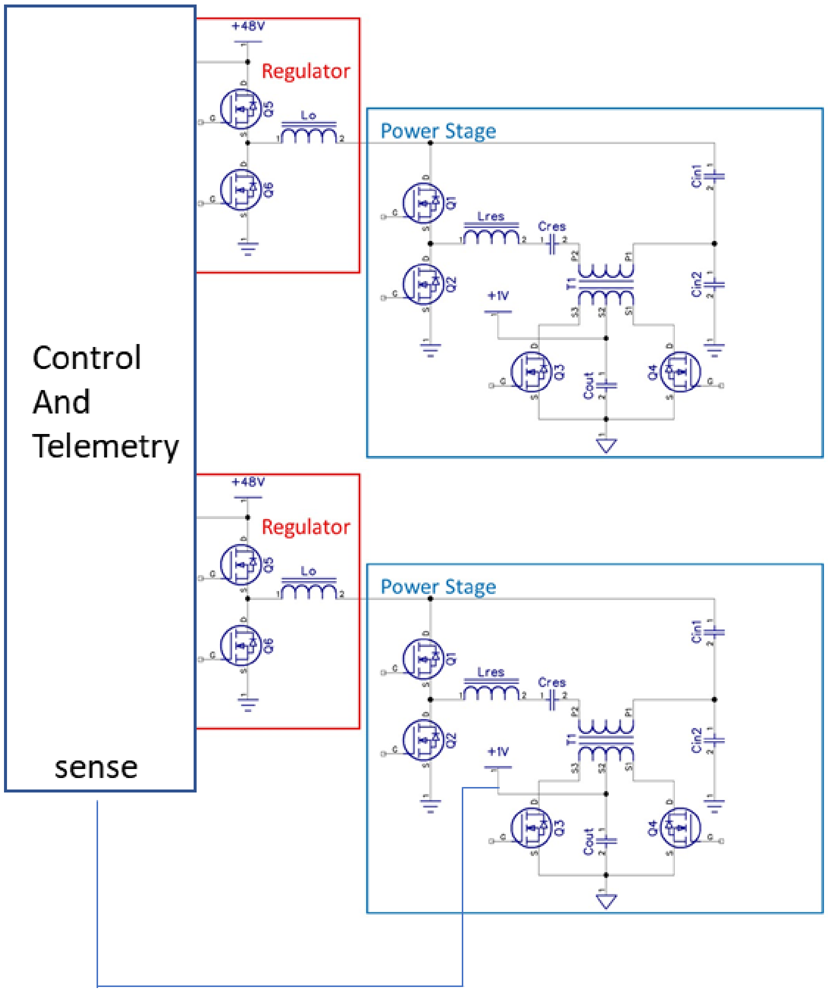
Example

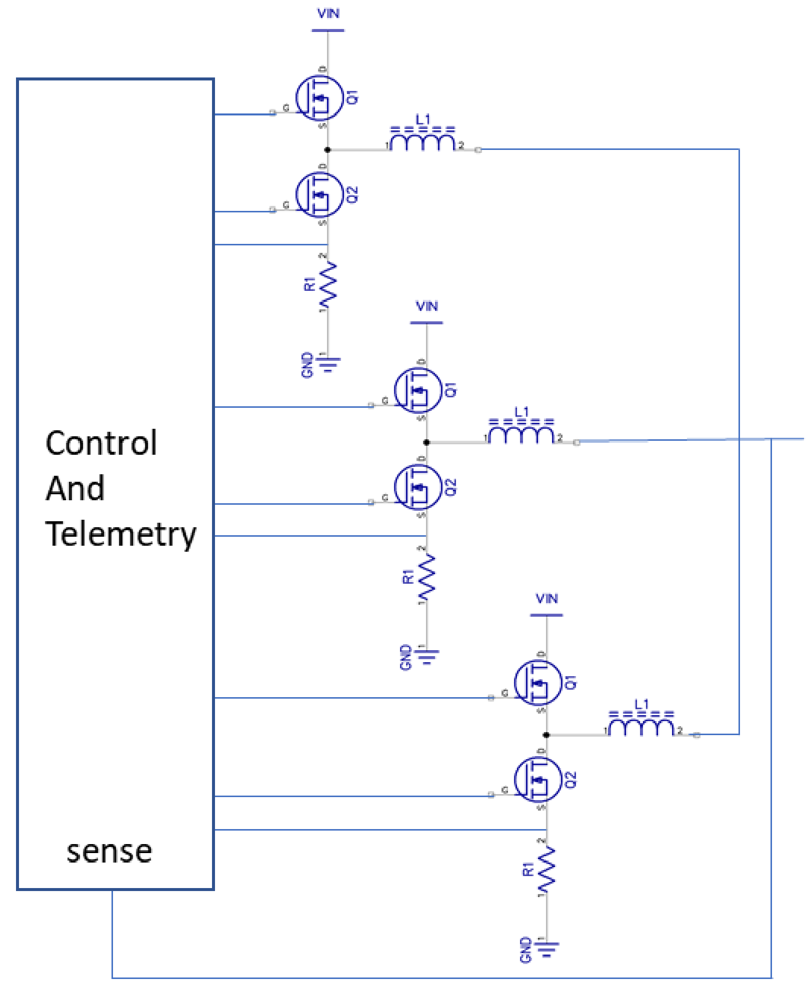
$V_{rail} = 0.7VDC$ $\qquad I_{rail} = 500Amps$

$\Delta V_{rail} = \underline{+}\ 50mV$ $\qquad \Delta I_{rail} = 250Amps$

Noise Source		
DC setpoint accuracy	1%	1%*700mV=7mV
$\Delta VRipple$	1% pk	1% * 700mV=7mV
ΔVin*PSRR	1% pk	1% * 700mV=7mV
ΔI	250Amps	
	Total other noise sources	$\underline{+}$ 21mV

$$R_{target} = \frac{50mV - \ 7mV - 7mV - \ 7mV}{250A} = \frac{29mV}{250A} = 116u\Omega$$

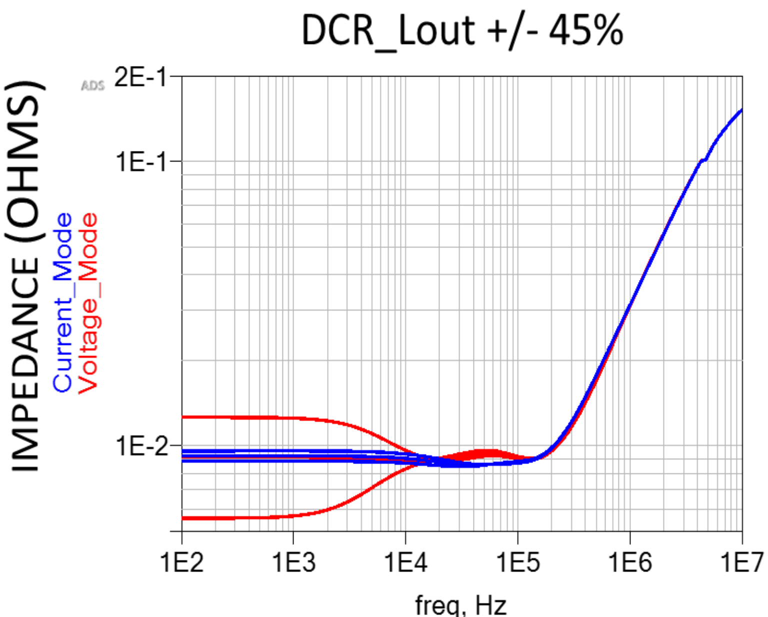

Control
And
Telemetry
sense
+48V
Regulator
Q5
Lo
Q6
Power Stage
Q1
Q2
Lres
Cres
T1
+1V
Cin1
Cin2
Q3
Cout
Q4


Control
And
Telemetry
sense
VIN
Q1
L1
Q2
R1
GND

$$R_{out} = \frac{\frac{2 \cdot Fs \cdot Lo \cdot Ri \cdot Vin}{Ri \cdot Vin - 2 \cdot Ri \cdot Vo + 2 \cdot Fsw \cdot Lo \cdot Vramp} + DCR_{Lo} + RDSon_{bot} + (RDSon_{top} - RDSon_{bot}) \cdot \frac{Vo}{Vin}}{1 + Av \cdot \frac{2 \cdot Fs \cdot Lo \cdot Vin}{Ri \cdot Vin - 2 \cdot Ri \cdot Vo + 2 \cdot Fsw \cdot Lo \cdot Vramp}}$$

$$R_{out_{cm}} \approx \frac{R_i}{(1 + Av)} = \frac{1}{PS_{gfs} \cdot (1 + A_v)}$$

Designation	
Lo	Output filter inductor of each regulator
Fs	Switching frequency
Ri	Current Sense resistance $= {}^{1}/_{PS_{gfs}}$
Vin	Voltage regulator DC input voltage
Vo	Voltage regulator output voltage
Vramp	Modulation or slope compensation ramp amplitude
Av	Feedback amplifier gain
N	Number of parallel switching regulators
K	Number of parallel current multiplier modules



$$L_{excess} = \frac{Lo}{1 + \frac{2 \cdot Fs \cdot Lo \cdot Vin}{Ri \cdot Vin - 2 \cdot Ri \cdot Vo + 2 \cdot Fs \cdot Lo \cdot Vramp} \cdot Av}$$

For Flat Impedance →

$$Q = \frac{\sqrt{\frac{L\_excess}{Cout}}}{R\_out} \approx 1$$

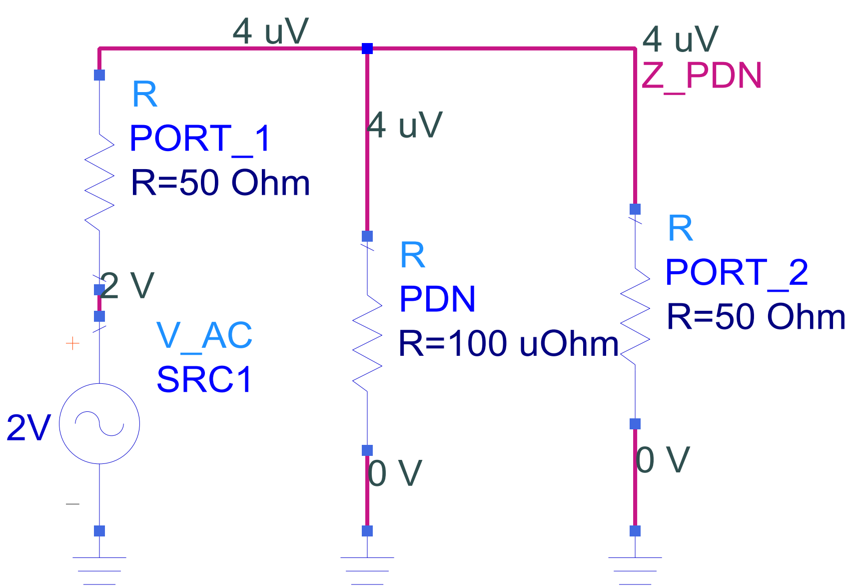
Solving for capacitance →

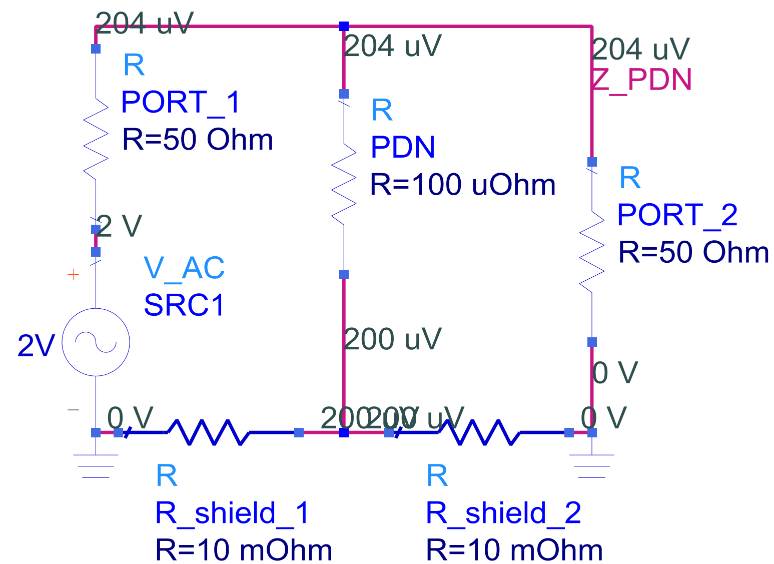
$$C_{out} \cong \frac{L_{excess}}{Rout^2}$$

$$ESR_{C_{out}} \cong Rout$$

Measurement Challenges at 100uΩ

$$S21 = \frac{DUT}{DUT + 25} = \frac{100u\Omega}{100u\Omega + 25} = 4u \qquad DUT = \frac{25 \cdot S21}{1 - S21} = \frac{25 \cdot 4u}{1 - 4u} = 100u\Omega$$

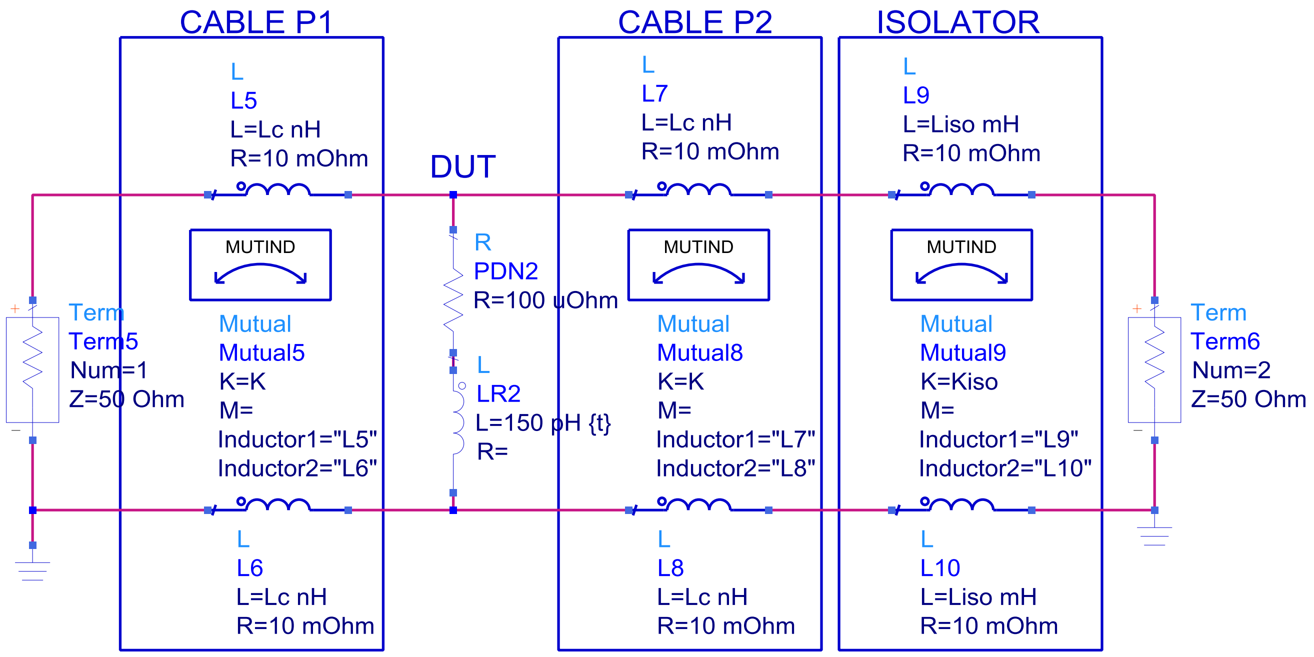




Measurement Challenges at 100uΩ

$$S21 = \frac{R\_shield\_1 \cdot \left(1 - \frac{1}{CMRR}\right) + DUT}{25 + R\_shield\_1 \cdot \left(1 - \frac{1}{CMRR}\right) + DUT}$$

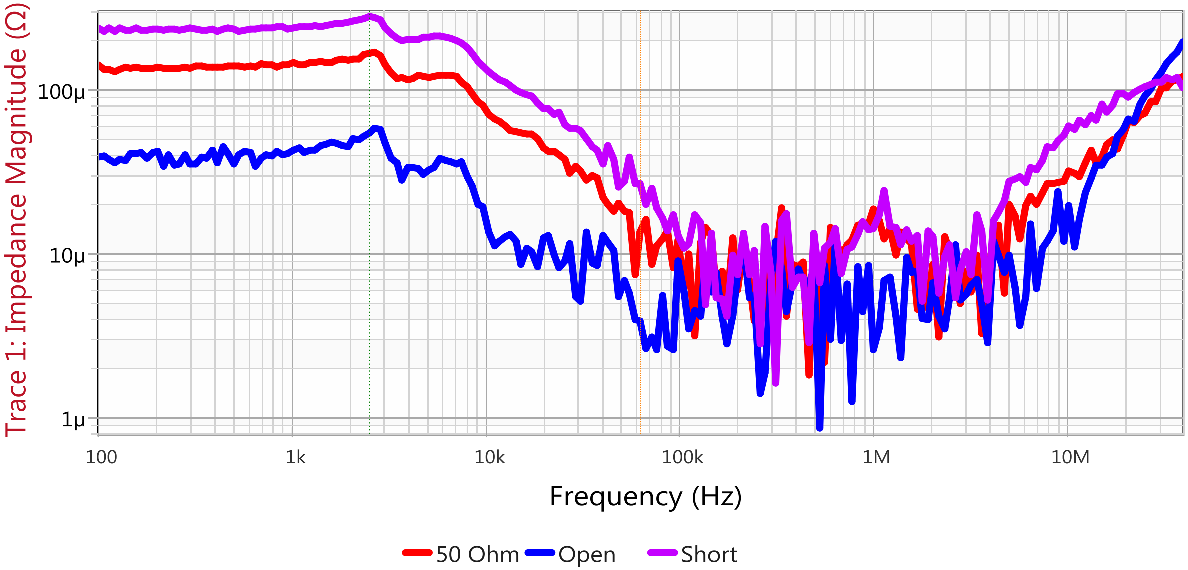
$$Error = \frac{R\_shield\_1}{CMRR}$$



Crosstalk Issues

Probe tip coupling

Near end port to port coupling due to cable loading



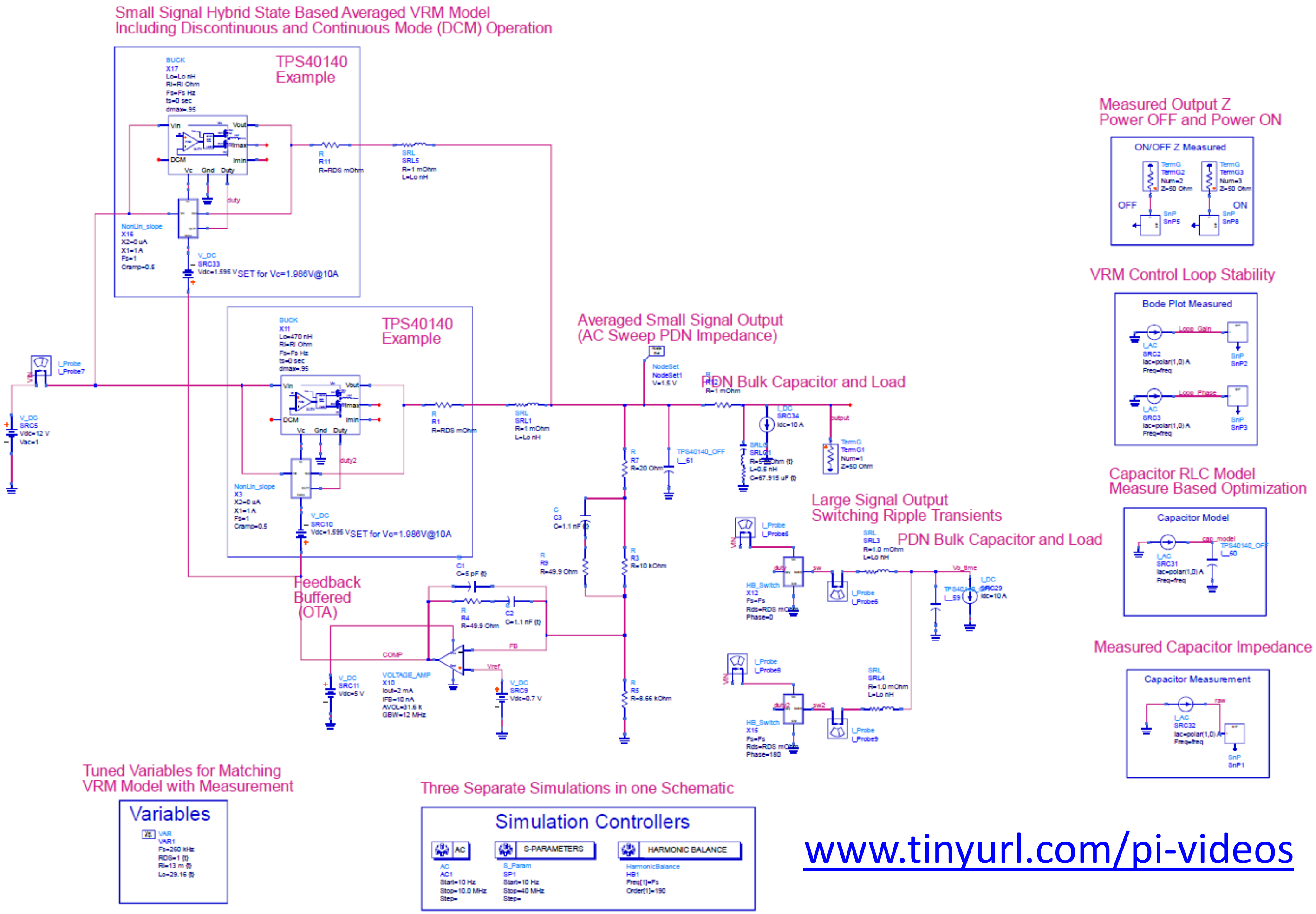
MEASUREMENT TIPS

- Use ONLY SOLDERED connectors!
- Use low resistance, multi-shield cable
- Keep connections SHORT from SOURCE to DUT.
- ALWAYS check cable integrity!
- ALWAYS measure something you know, and of similar magnitude
- Probe from both sides of the board if possible
- Include quality PCB connectors if possible
- Minimize cable adapters – use metrology cable if you muse use one
- Adding a SOURCE power amplifier will improve the signal to noise ratio

EDI CON 2018

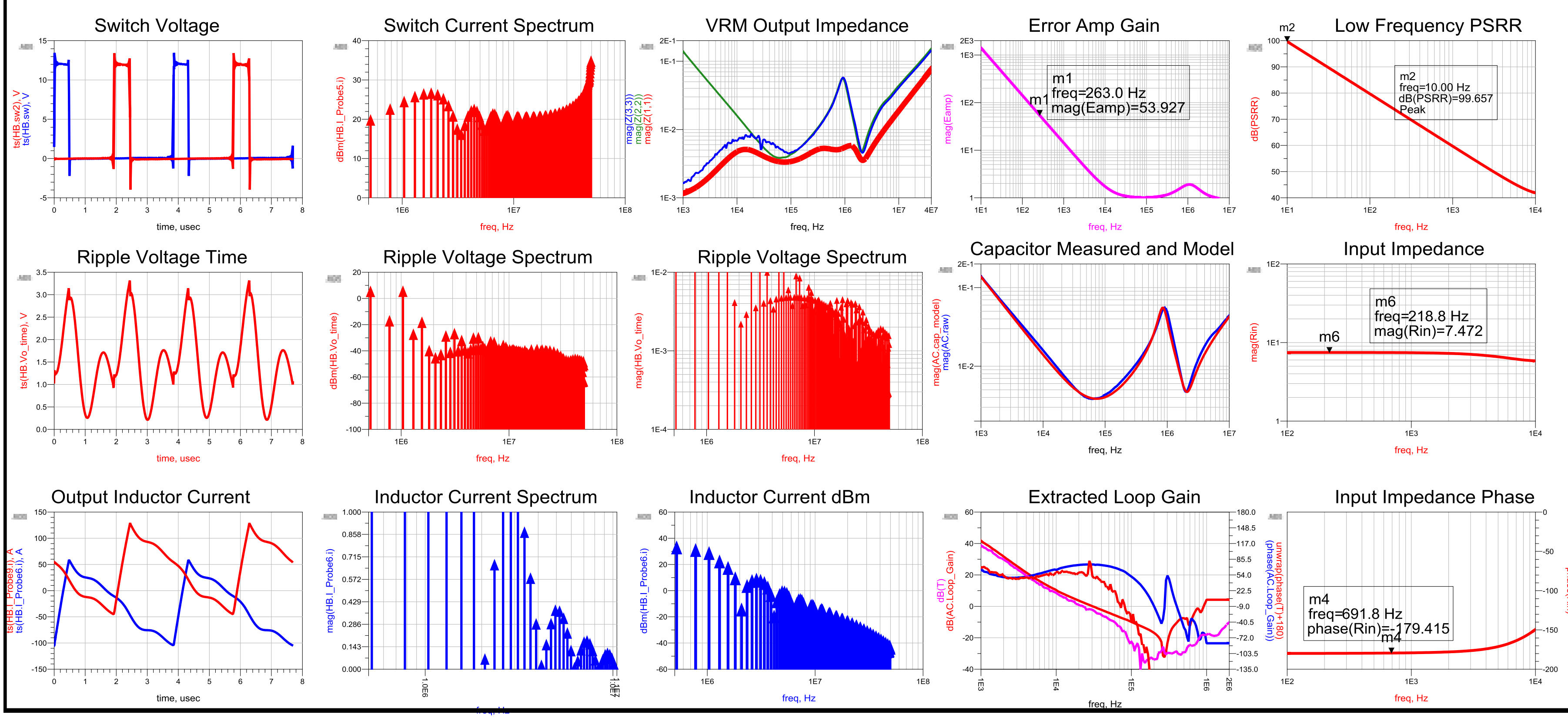
Electronic Design Innovation Conference & Exhibition

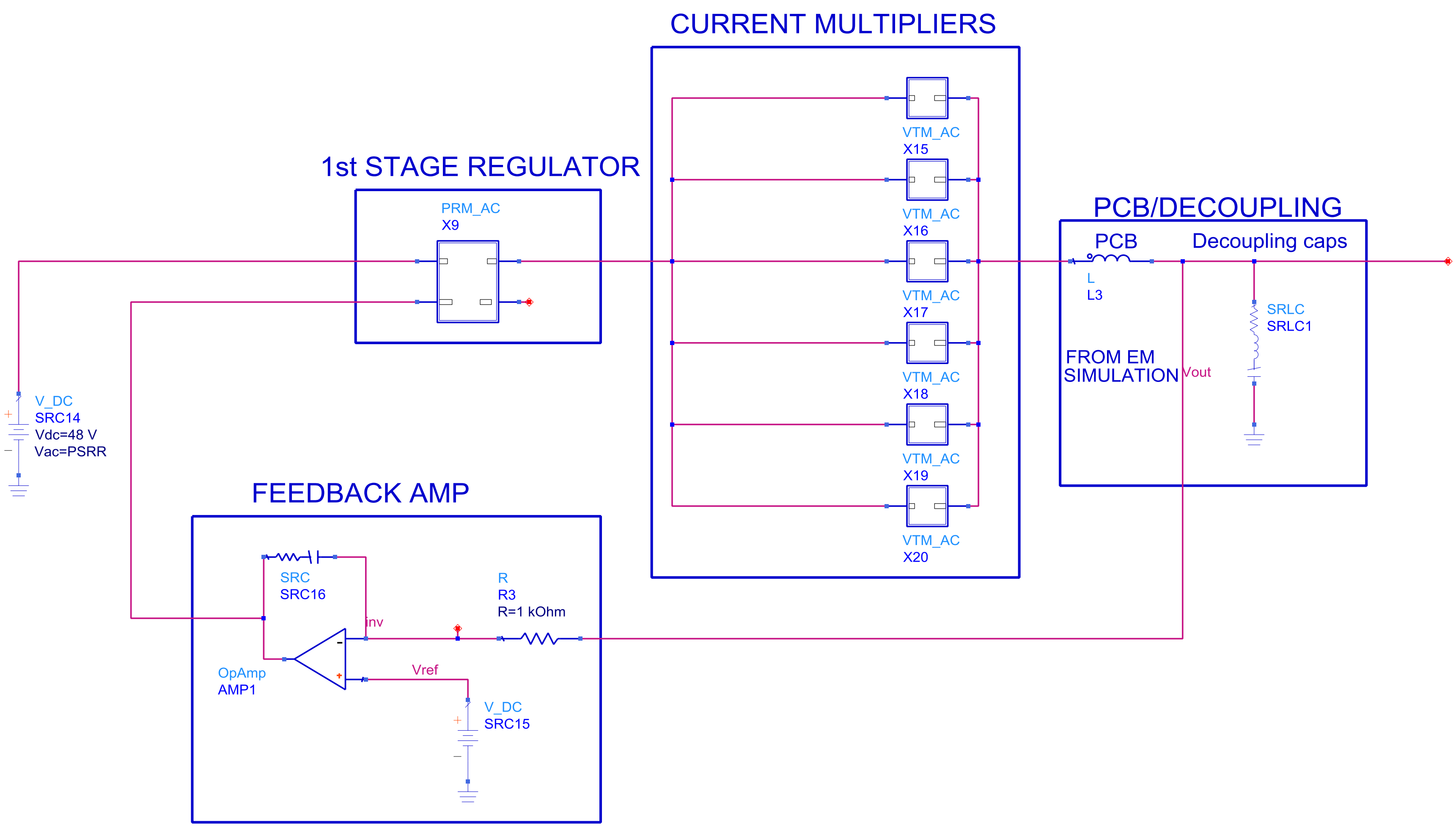
October 17-19 2018
Santa Clara Convention Center
Santa Clara, CA

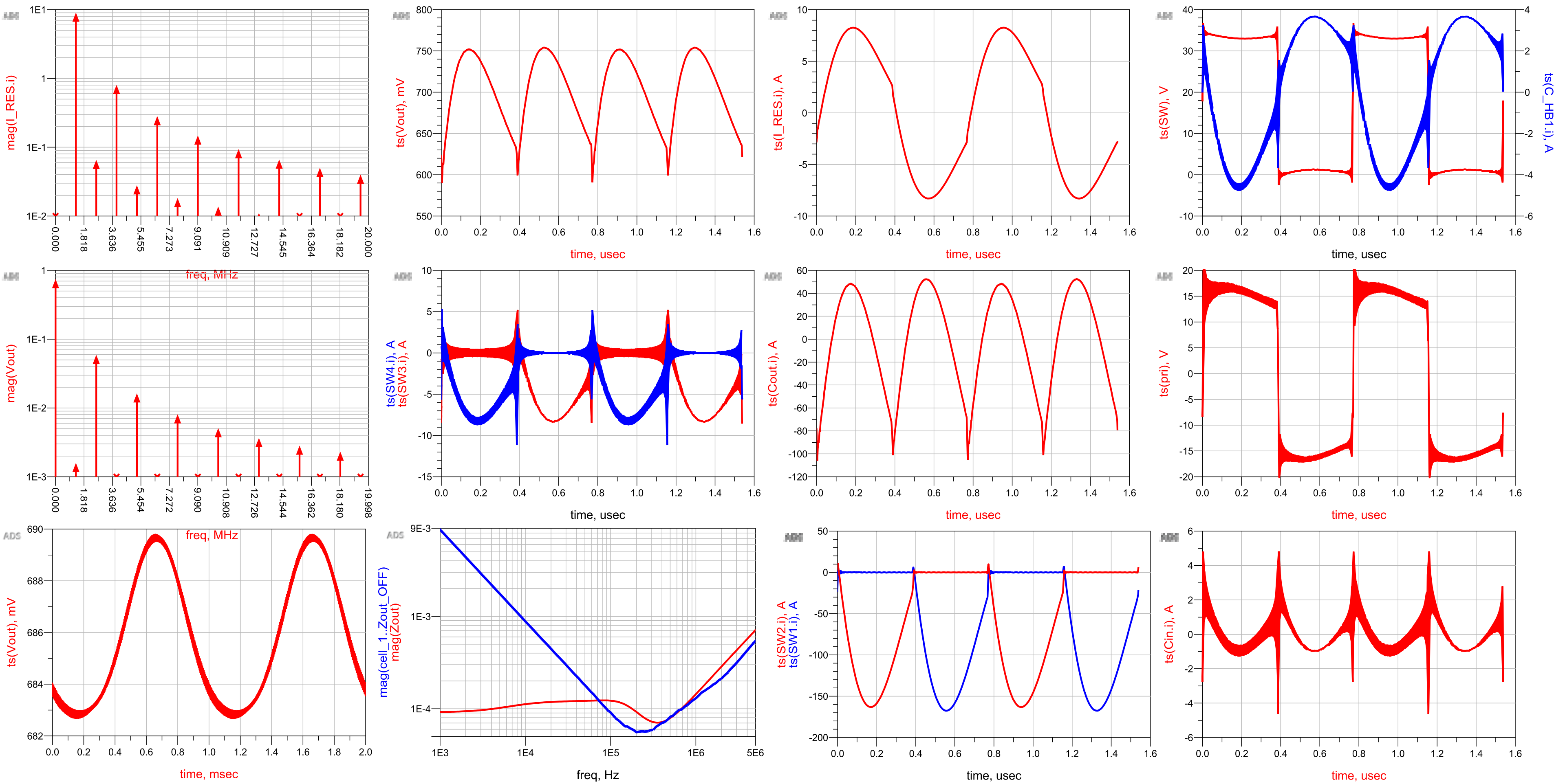


www.tinyurl.com/pi-videos

Multi-phase DC-DC Converter State Space Hybrid Model - TPS40140

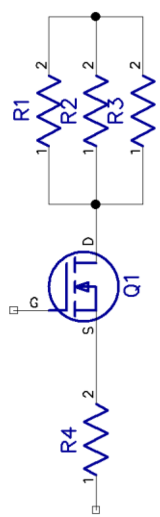



CURRENT MULTIPLIERS
VTM_AC
X15
VTM_AC
X16
VTM_AC
X17
VTM_AC
X18
VTM_AC
X19
VTM_AC
X20
1st STAGE REGULATOR
PRM_AC
X9
PCB/DECOUPLING
PCB
Decoupling caps
L
L3
SRLC
SRLC1
FROM EM
SIMULATION
Vout
V_DC
SRC14
Vdc=48 V
Vac=PSRR
FEEDBACK AMP
SRC
SRC16
inv
R
R3
R=1 kOhm
OpAmp
AMP1
Vref
V_DC
SRC15

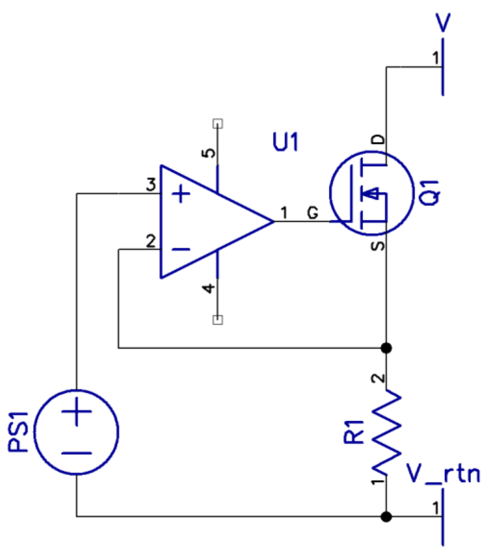

mag(I_RES.i)
freq, MHz
0.000
1.818
3.636
5.455
7.273
9.091
10.909
12.727
14.545
16.364
18.182
20.000
ts(Vout), mV
time, usec
ts(I_RES.i), A
time, usec
ts(SW), V
ts(C_HB1.i), A
time, usec
mag(Vout)
freq, MHz
ts(SW4.i), A
ts(SW3.i), A
time, usec
ts(Cout.i), A
time, usec
ts(pri), V
time, usec
ts(Vout), mV
time, msec
mag(cell_1..Zout_OFF)
mag(Zout)
freq, Hz
ts(SW2.i), A
ts(SW1.i), A
time, usec
ts(Cin.i), A
time, usec

Three (and a half) Load Testing Solutions

Slammer



Current Sink



In-socket current sink

SLAMMER	
PROS	CONS
LOWEST COST	HIGHEST INDUCTANCE
NO STABILITY ISSUE	SLOWEST
	INTERCONNECTS

CURRENT SINK	
PROS	CONS
GENERAL SOLUTION	INTERCONNECTS
MODERATE COST	STABILITY
	HIGHER INDUCTANCE
	SLOWER SPEED

IN SOCKET CURRENT SINK	
PROS	CONS
LOWER INDUCTANCE	INTERPOSERS
HIGHER SPEED	LIMITED SPEED
PROGRAMMABILITY	COST
	COOLING

DUT SOFTWARE	
PROS	CONS
LOWEST INDUCTANCE	RISKS DUT
MIN HARDWARE	CODE DESIGN COST
HIGHEST SPEED	Indirect current
PROGRAMMABILITY	

Is it Necessary??

It Depends!!

Thanks for Attending this Session!

In this session I shared

- How to create an impedance budget
- The two common design architectures
- Measurement limitations and tips to overcome them
- The biggest challenge to transient testing
- Many additional resources

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