EDI CON 2018
Electronic Design Innovation Conference & Exhibition
October 17-19 2018
Santa Clara Convention Center
Santa Clara, CA

VRM Modeling: A Strategy to Survive the Collision of Three Worlds

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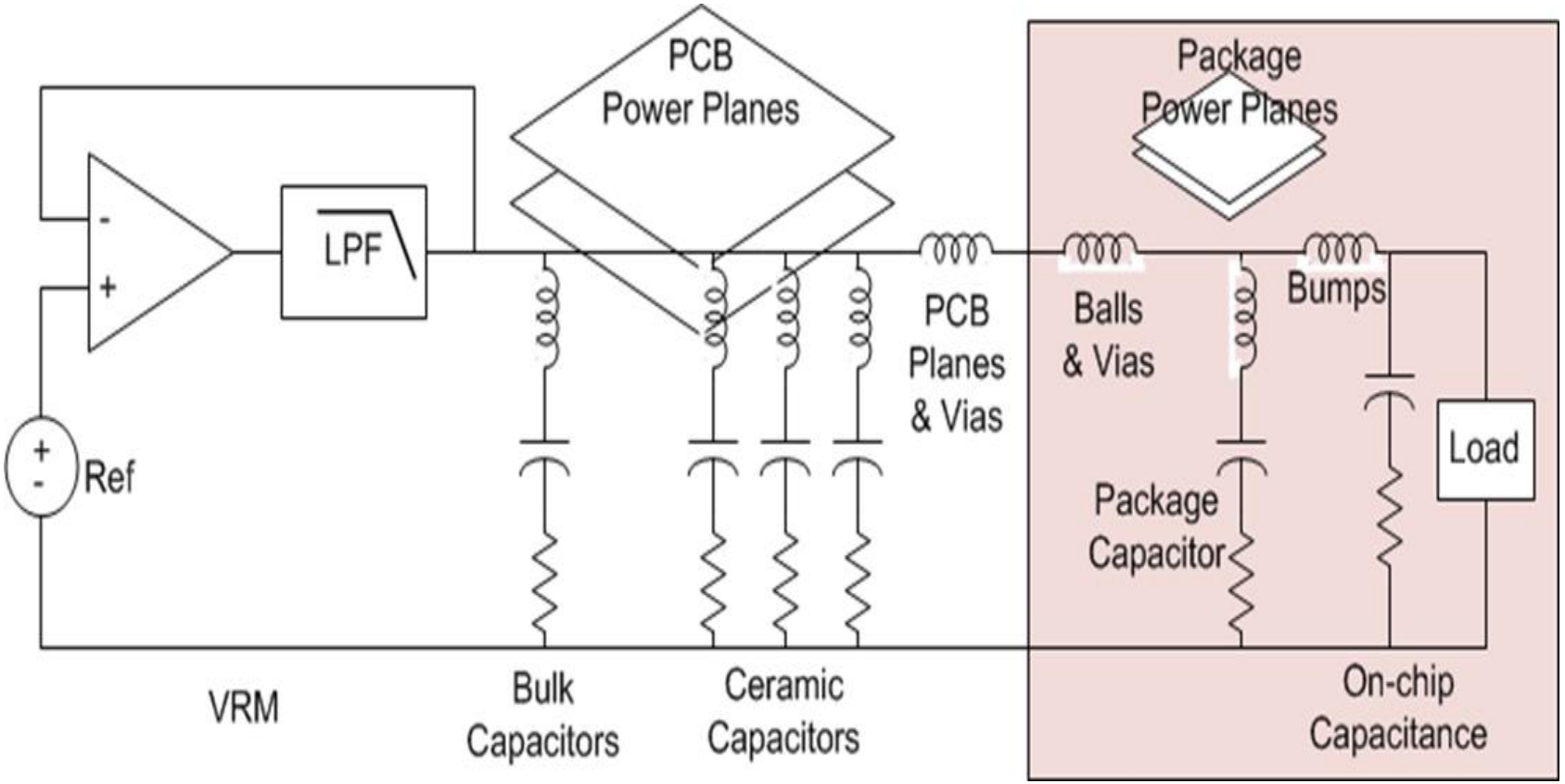
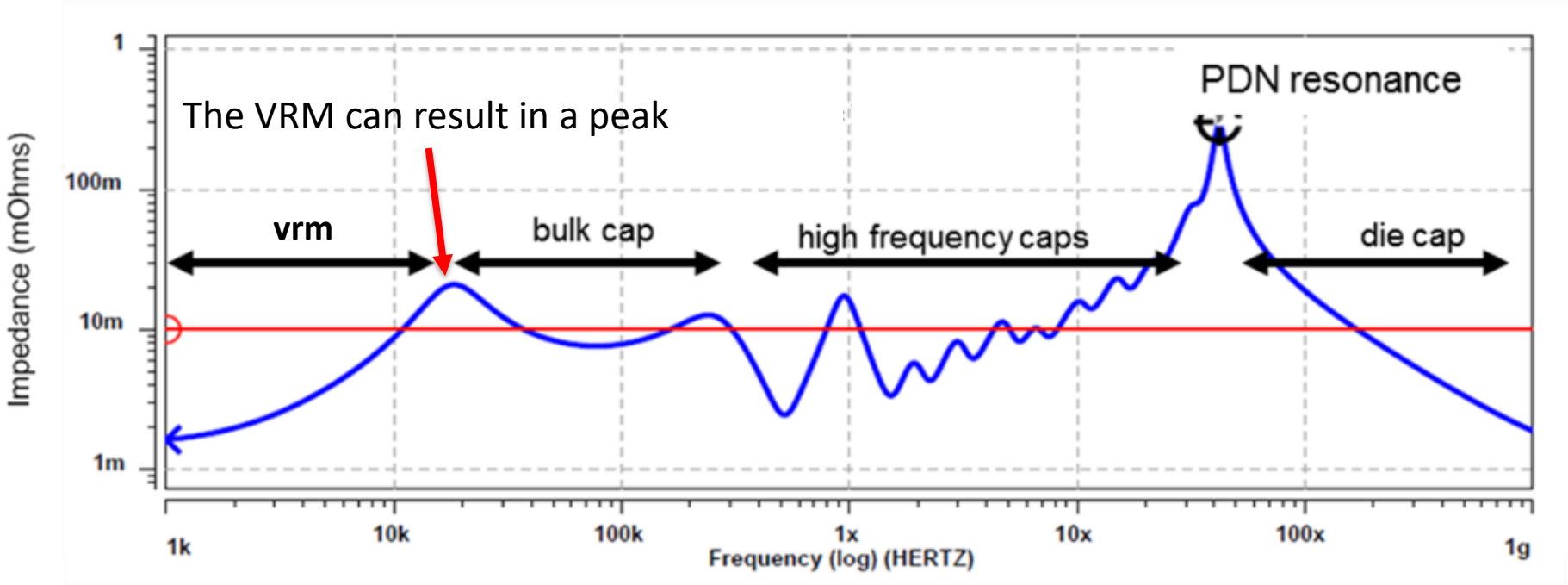
Larry Smith, PDNPowerIntegrity.com

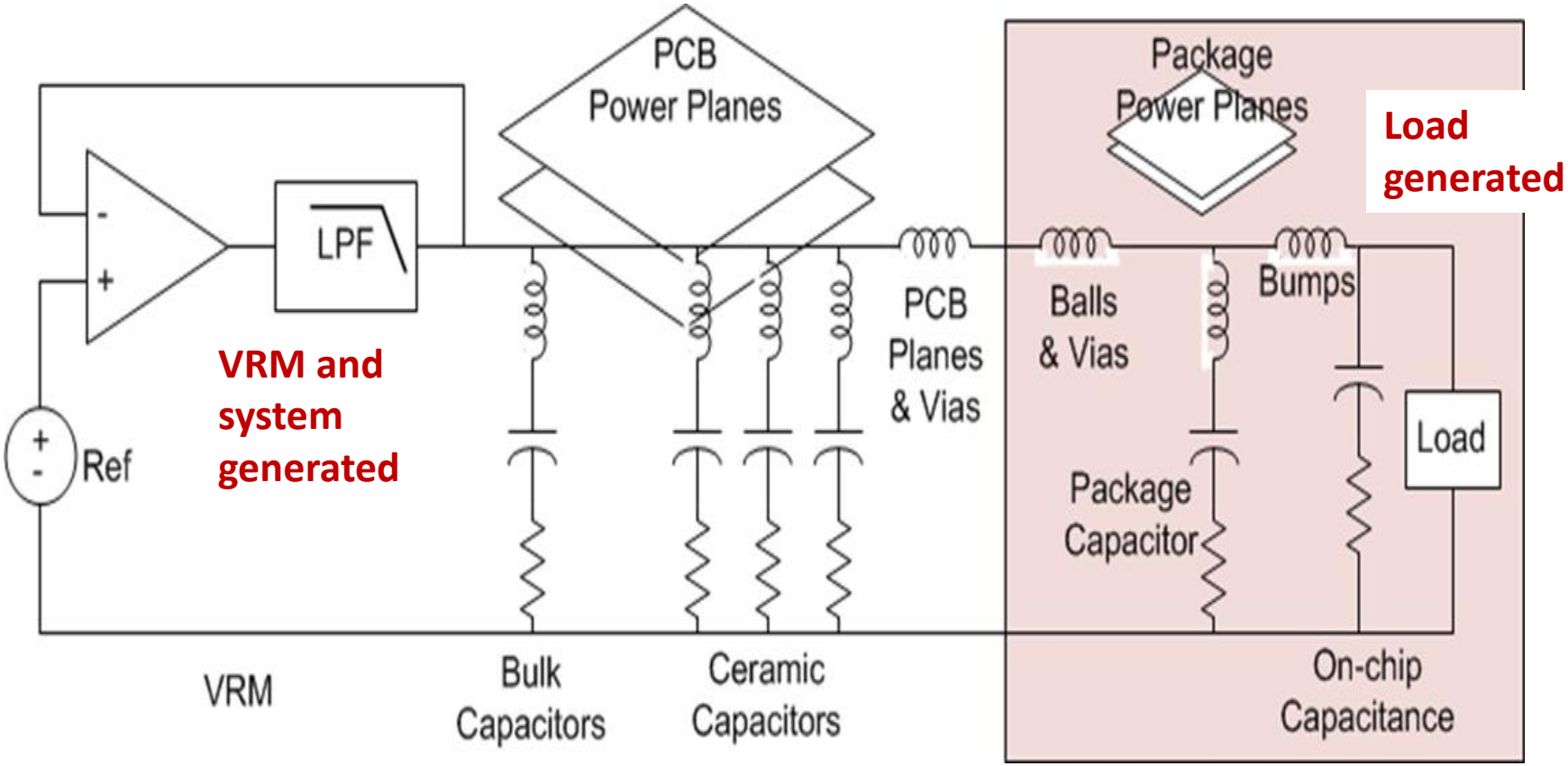
The Typical PDN

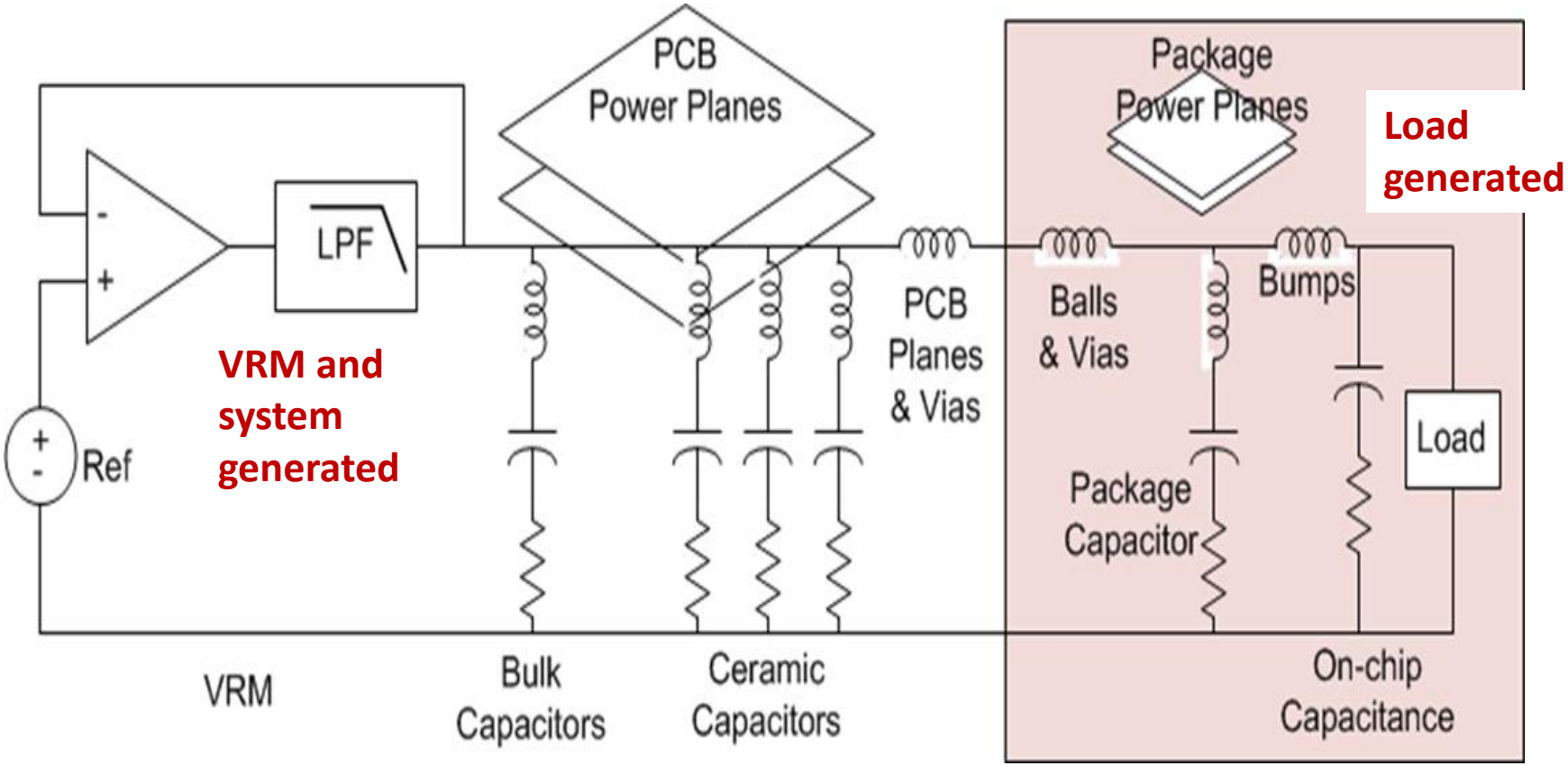


And a Look at Impedance



The VRM Contributions



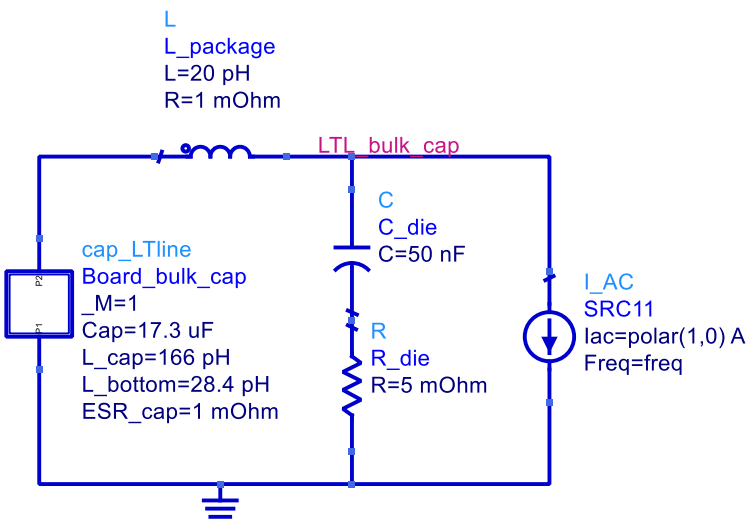

PCB
Power Planes
Package
Power Planes
Load
generated
LPF
VRM and
system
generated
Ref
PCB
Planes
& Vias
Balls
& Vias
Bumps
Load
Package
Capacitor
VRM
Bulk
Capacitors
Ceramic
Capacitors
On-chip
Capacitance

Representing the VRM

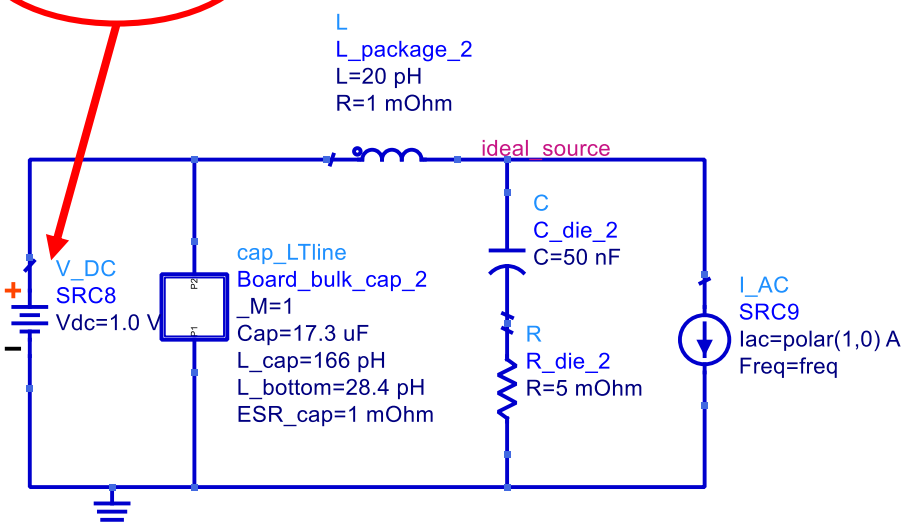
1. DC Voltage Source
2. R-L network
3. R-L-R-L network
4. High accuracy model

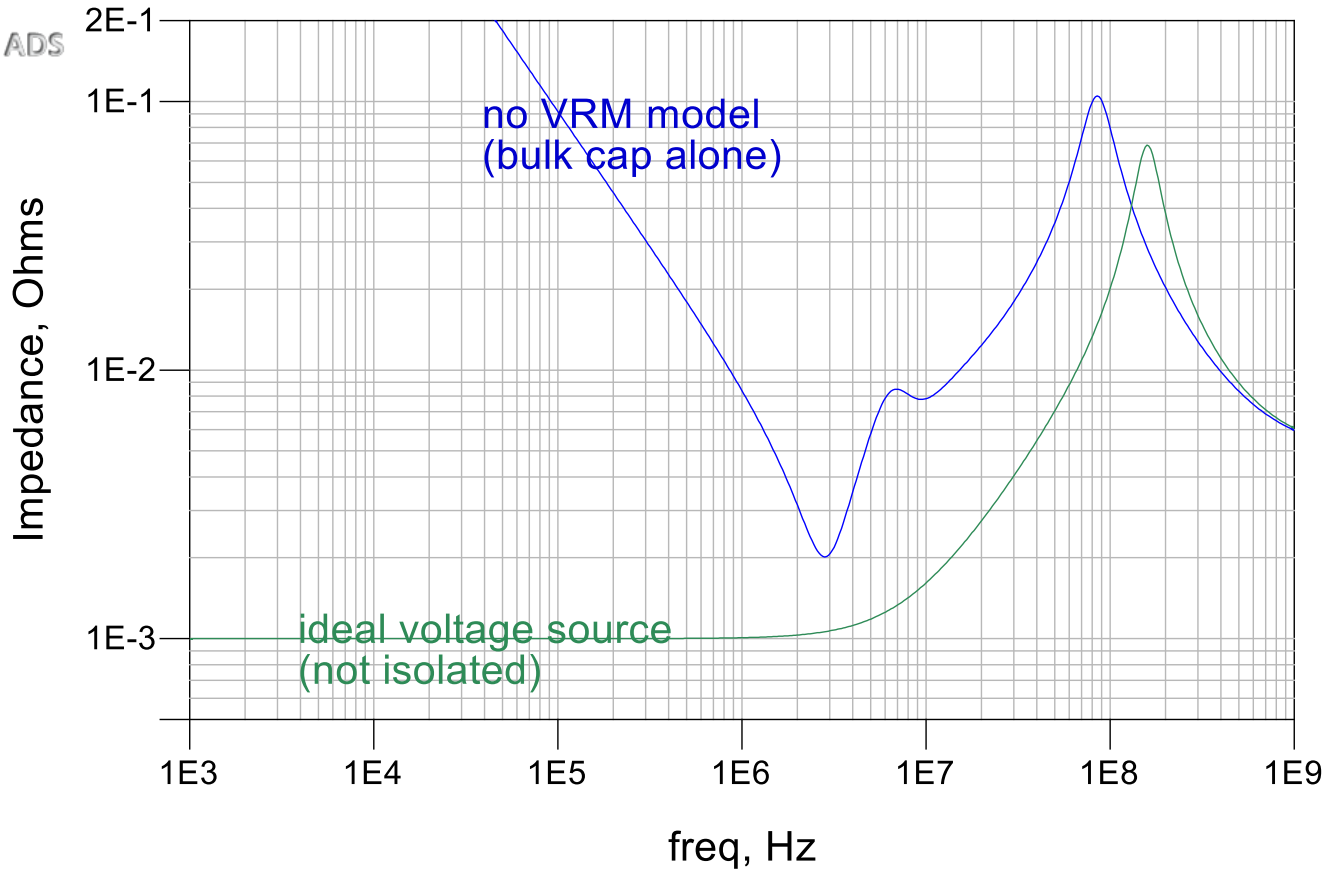
DC Voltage Source

PDN Bulk and Die Caps



IDEAL VRM + PDN Bulk and Die Caps

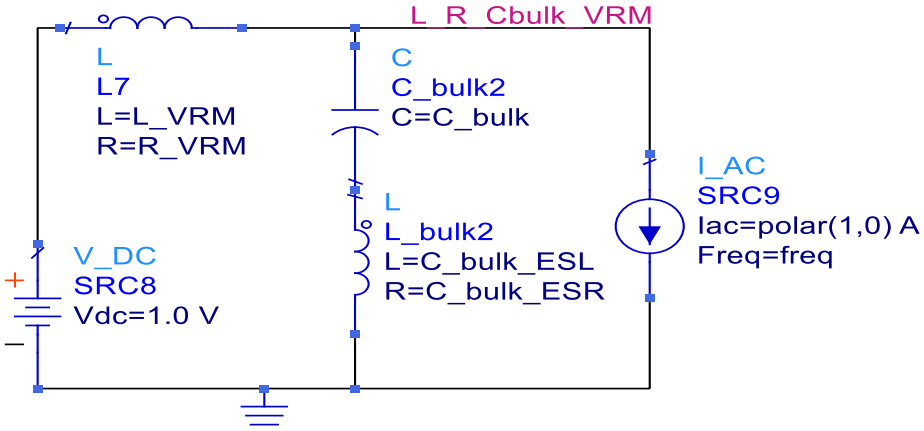


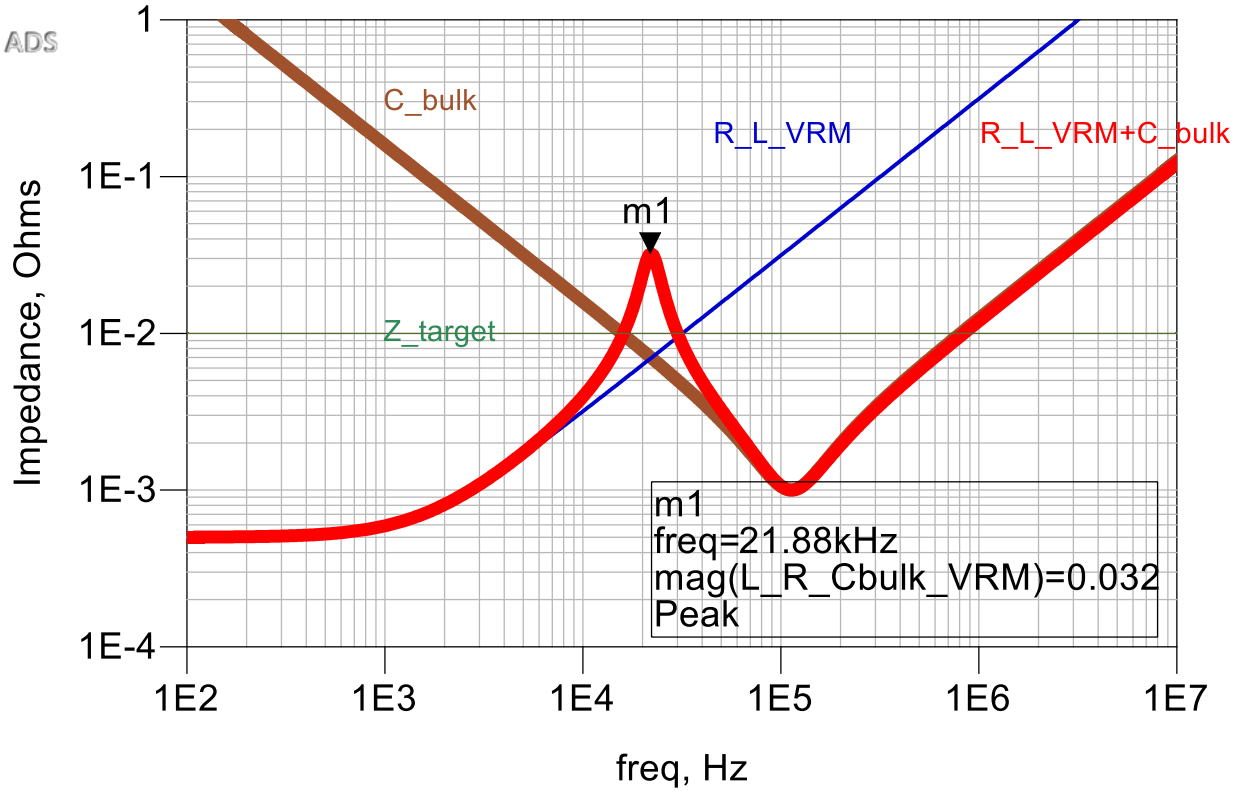

ADS
2E-1
1E-1
1E-2
1E-3
Impedance, Ohms
no VRM model
(bulk cap alone)
ideal voltage source
(not isolated)
1E3
1E4
1E5
1E6
1E7
1E8
1E9
freq, Hz

R-L Network

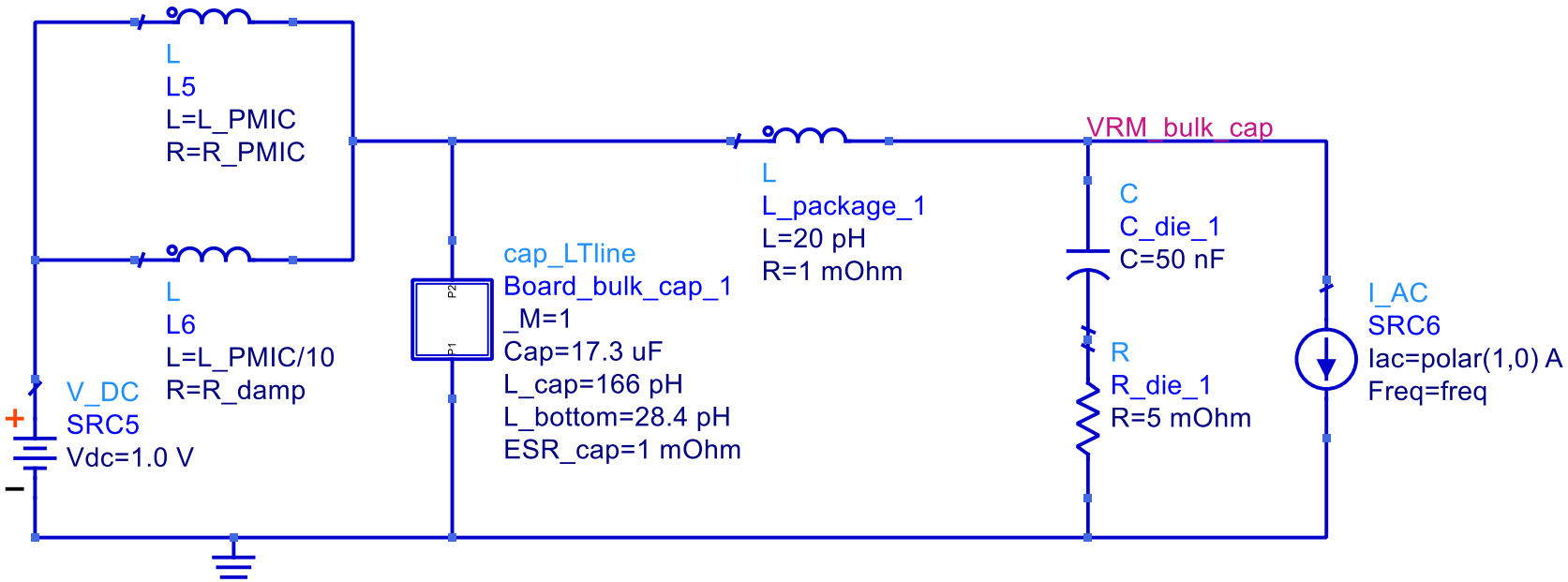
Flat Impedance VRM Representation

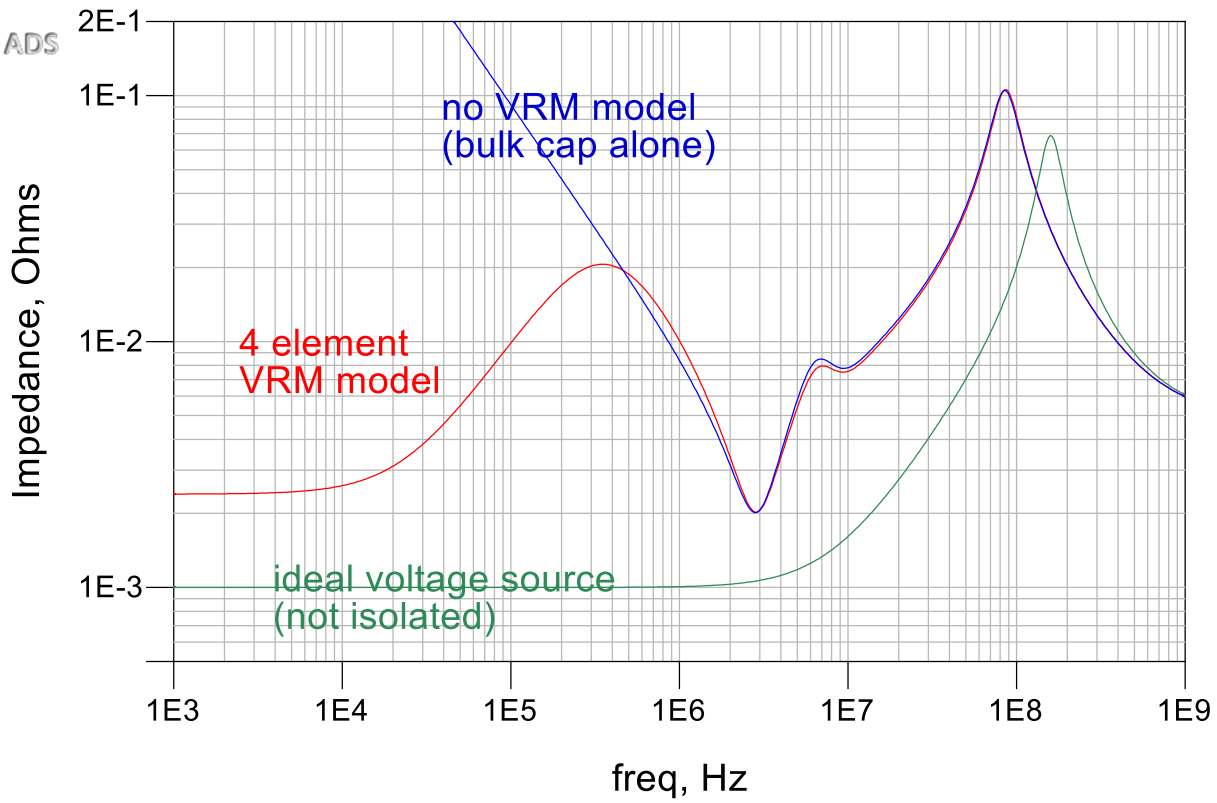
Var Eqn
VAR
VAR1
L_VRM=50 nH
R_VRM=0.5 mOhm
R_damp=20 mOhm
C_bulk=1000 uF
C_bulk_ESR=1 mOhm
C_bulk_ESL=2 nH



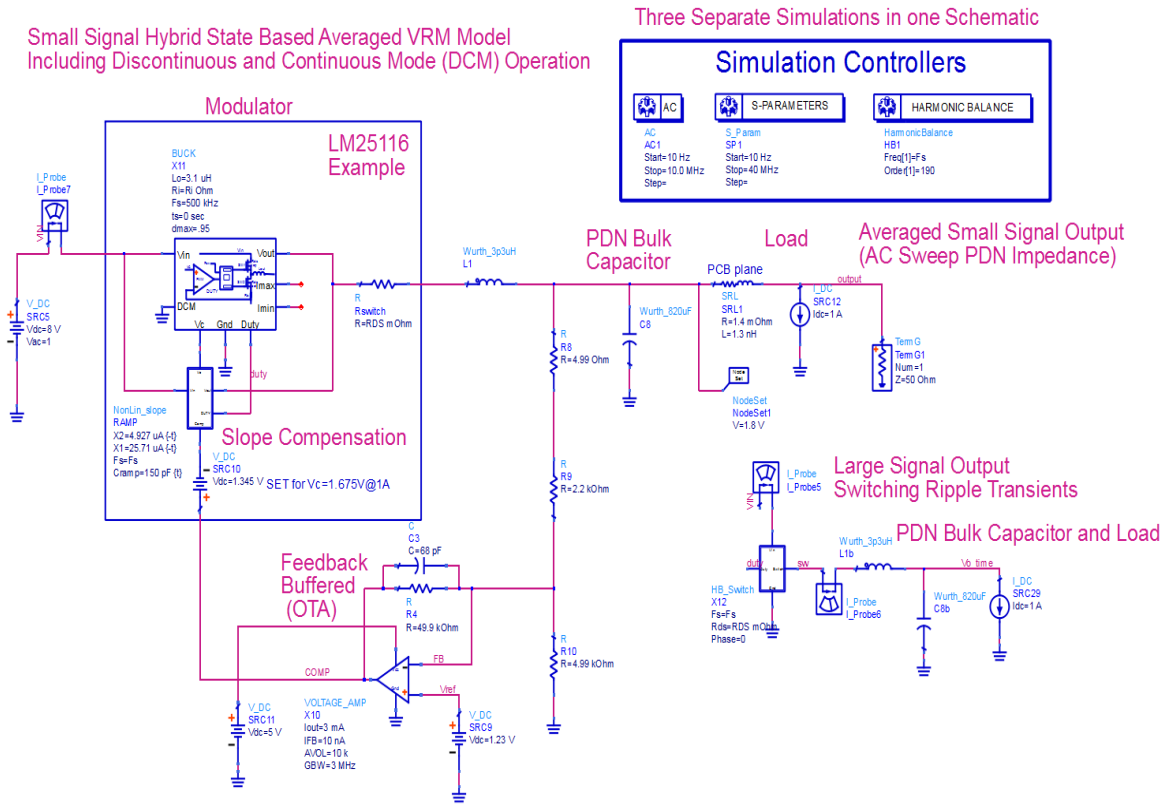

ADS
1
1E-1
1E-2
1E-3
1E-4
Impedance, Ohms
C_bulk
R_L_VRM
R_L_VRM+C_bulk
m1
Z_target
m1
freq=21.88kHz
mag(L_R_Cbulk_VRM)=0.032
Peak
1E2
1E3
1E4
1E5
1E6
1E7
freq, Hz

R-L-R-L Network

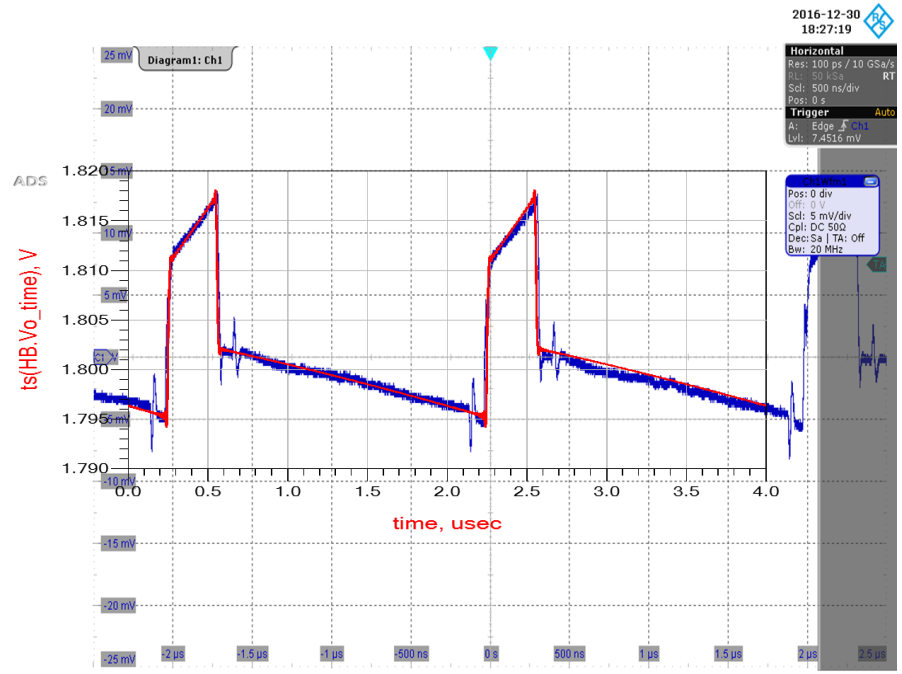


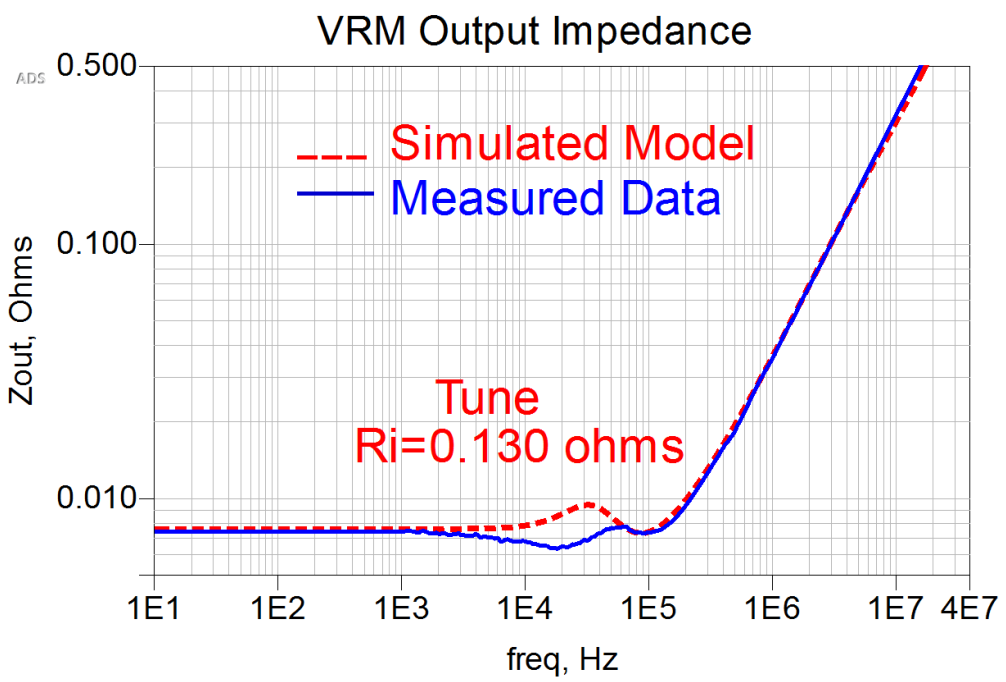

ADS
2E-1
1E-1
1E-2
1E-3
Impedance, Ohms
no VRM model
(bulk cap alone)
4 element
VRM model
ideal voltage source
(not isolated)
1E3
1E4
1E5
1E6
1E7
1E8
1E9
freq, Hz

High Accuracy Model



Gets Both Right





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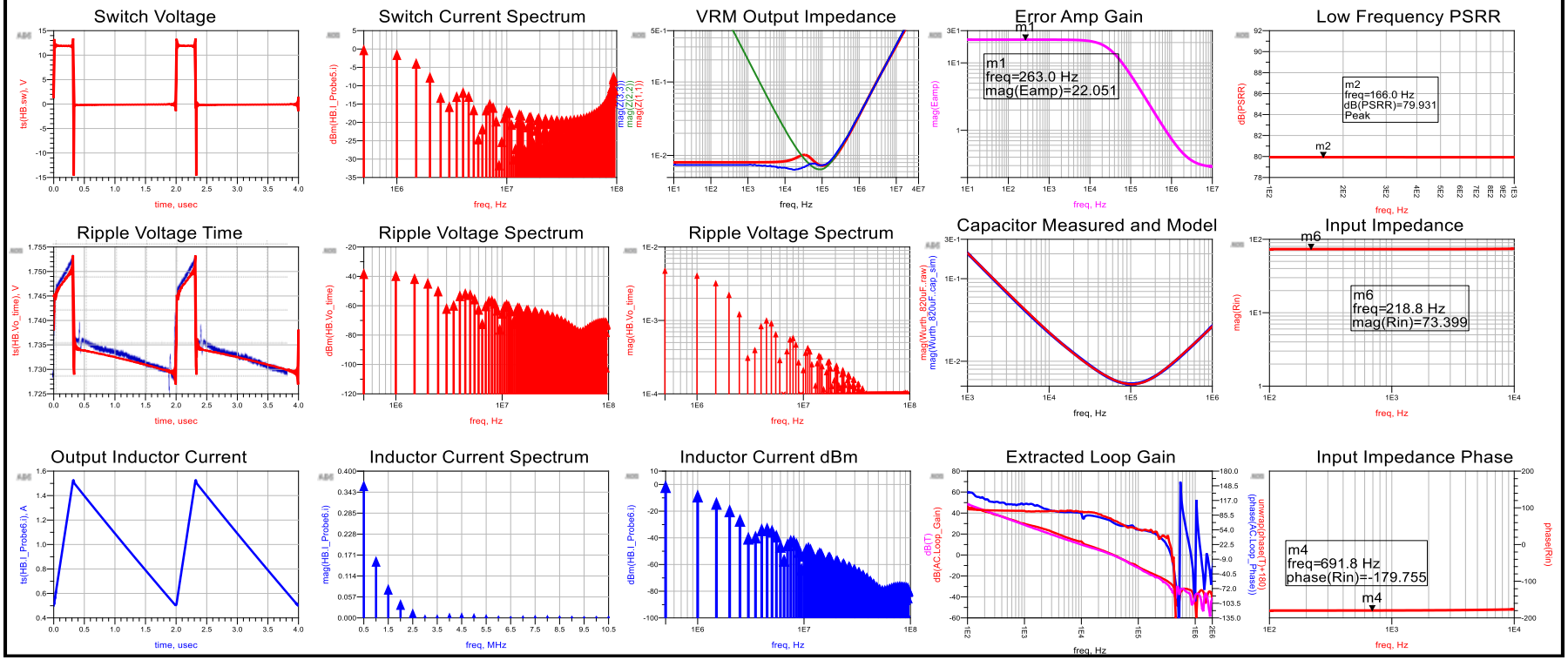
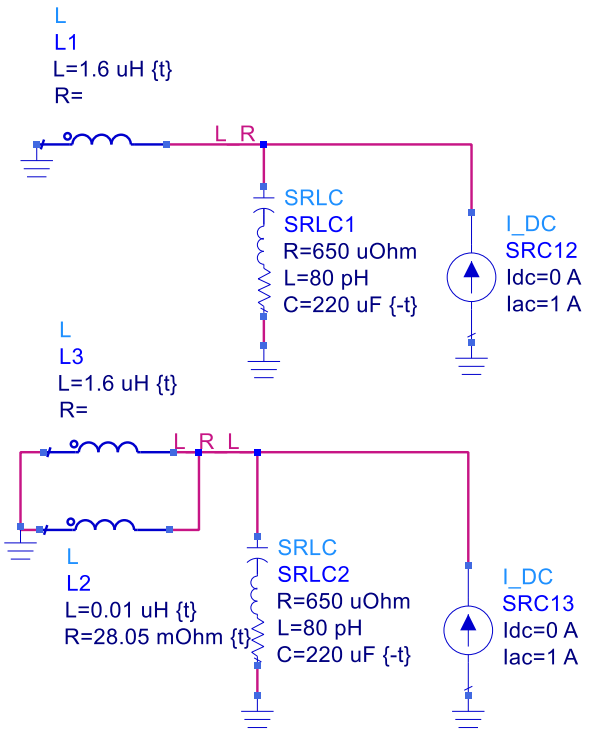
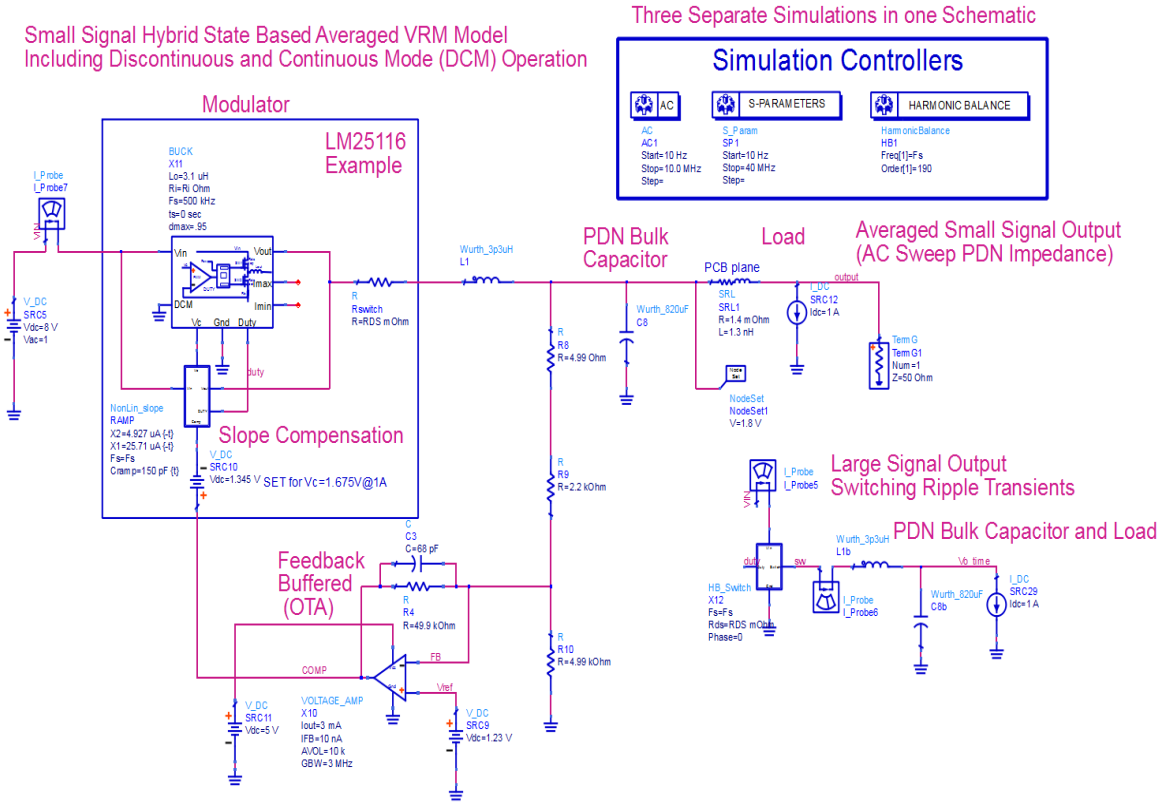
State Space Hybrid Model - LM25116

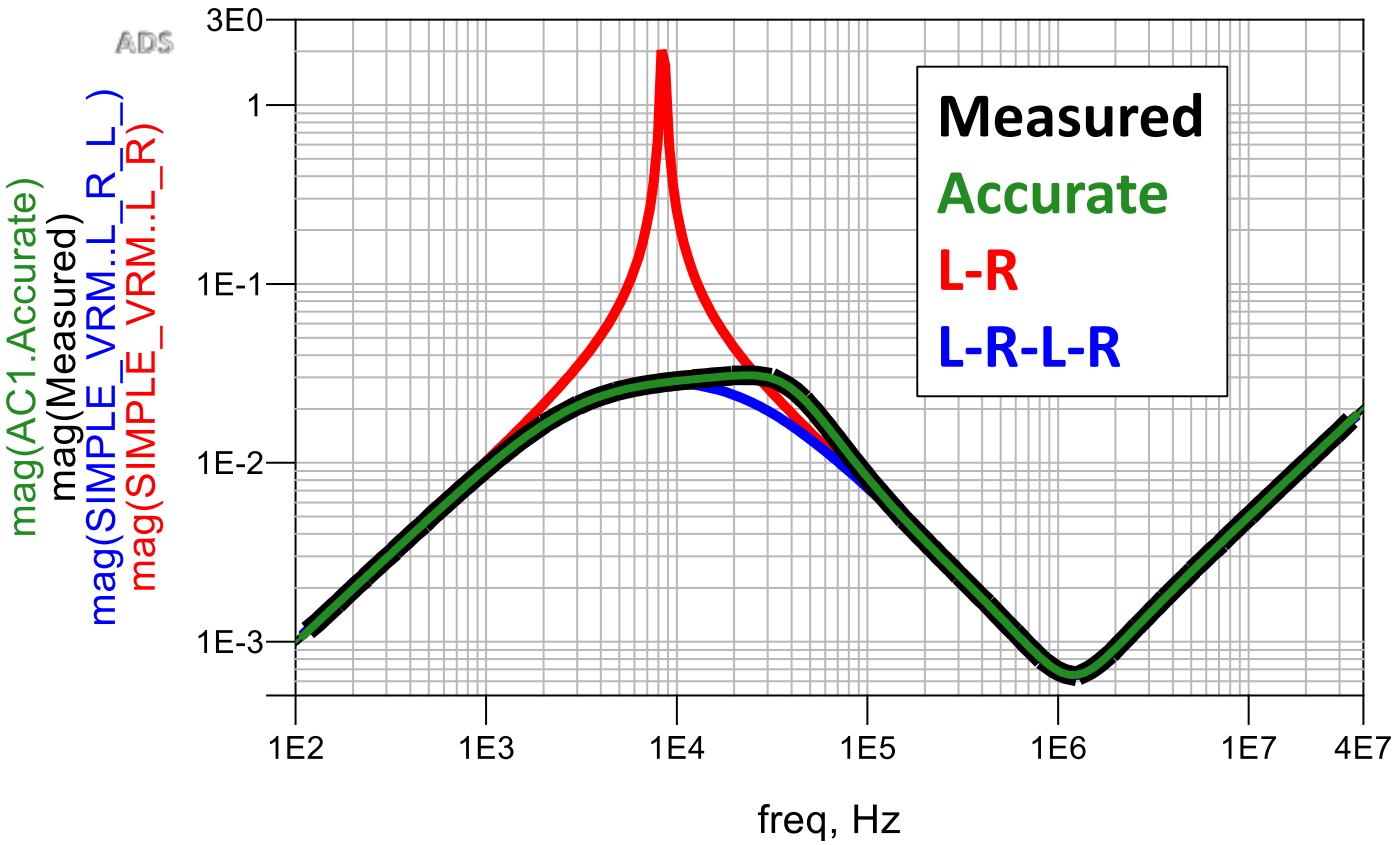


Accurate, L-R and L-R-L-R





Model Comparison



Supported Characteristics

	V Source	L-R	L-R-L-R	Accurate
PDN Impedance	INCORRECT RESULT	NOT WELL	REASONABLY	Y
Switching ripple	N	N	N	Y
PSRR/Transients	N	N	N	Y
Negative resistance	N	N	N	Y
Input switching current	N	N	N	Y
Control loop stability	N	N	N	Y
Turn on overshoot	N	N	N	Y
Remote sense	N	N	N	Y

Conclusions

1. Omitting the VRM model completely can eliminate one or more impedance peaks that contribute to PDN noise as well as eliminating the self-generated noise contribution of the VRM
2. Replacing the VRM with a voltage source shorts the PDN generating in incorrect results
3. A simple, R-L model provides basic impedance characteristics that can show the PDN impedance peaks, though in low fidelity. Self-generated noise is ignored
4. A pair of R-L models provides a more accurate representation of VRM related impedance peaks, while still ignoring self generated noise
5. A highly accurate, state space based model is more difficult to create but provides accurate representations of both the impedance peaks and the VRM self generated noise. Other VRM characteristics are also included, such as control loop stability, input source transients and other switching related noise effects.

Thanks for Attending Our Session!

Maintain your Integrity - Power Responsibly

REFERENCES

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2. V. Sriboonlue, L. Smith, J. Mohamed, J. Shin, and T. Michalka, "Novel Parallel Resonance Peak Measurement and Lossy Transmission Line Modeling of 2-T and 3-T MLCC capacitors for PDN Application."
3. H. Barnes, J. Carrel, and S. Sandler, "Power Integrity for 32 Gb/s SERDES Transceivers," in *DesignCon*, 2018.
4. L. Smith and E. Bogatin, *Principles of Power Integrity for PDN Design*. Prentice Hall, 2017.
5. S. Sandler, *Measurement based VRM modeling*, 2017 IEEE 21st Workshop on Signal and Power Integrity (SPI) DOI:10.1109/SaPiW.2017.7944009, June 8, 2017, Baveno Italy.
6. S. Sun, A. Corp, L. D. Smith, and P. Boyle, "On-Chip PDN Noise Characterization and Modeling," in *Santa Clara, CA, DesignCon*, 2010, no. 408, pp. 1–21.