

COM for PAM4 Link Analysis – what you need to know

Geoff Zhang, Min Huang, Hongtao Zhang
SerDes Technology Group, Xilinx Inc.

Abstract

COM (Channel Operating Margin) was initially adopted in the IEEE802.3bj standard. The intent is to qualify a high speed serial channel in the context of a specification. The analysis is expected to be fast and efficient, utilizing transmitter and receiver specification parameters. This is in contrast to time-domain bit-by-bit simulations that require both high quality device models and a long running time.

This paper focuses on the following six areas, with the emphasis on PAM4 signaling:

- (1) COM sampling time determination and its impact on channel margin
- (2) DFE tap coefficient impact on link error propagation and FEC CG
- (3) Jitter treatment and its impact on the accuracy in predicting COM
- (4) TX output signal level separation mismatch and how it is treated
- (5) CTLE implementation discussion and its implications for COM
- (6) COM margin computation and COM pass/fail criteria discussions

The first goal of the paper is to provide the very basics for the beginners of COM. The second goal is to bring adequate attention to the COM community so that the computed results for PAM4 channels can be better interpreted and link margin assessment decisions can be more properly made without being too optimistic or too pessimistic for PAM4 systems in which FEC is mandatory.

Authors Biography

Geoff Zhang received his Ph.D. in 1997 in microwave engineering and signal processing from Iowa State University, Ames, Iowa. He joined Xilinx Inc. in June, 2013. Geoff is currently Distinguished Engineer and Supervisor, in transceiver architecture and modeling under SerDes Technology Group. Prior to joining Xilinx he has employment experiences with HiSilicon, Huawei Technologies, LSI, Agere Systems, Lucent Technologies, and Texas Instruments. His current interest is in transceiver architecture modeling and system level end-to-end simulation, both electrical and optical.

Min Huang received her Master in 2013 in electrical engineering from University of California, Los Angeles. Min joined Xilinx Inc. since 2015 in transceiver architecture and modeling team under SerDes Technology Group. Prior to that, she was working on SerDes architecture at LSI. Her current interest is high speed IO architecture modeling and system level simulations.

Hongtao Zhang received his Ph.D. degree in Electrical and Computer Engineering from University of California, San Diego in 2006. He joined Xilinx in 2013 and is now a Senior Staff Design Engineer, working on SerDes architecture development and circuit design. From 2010 to 2013, he was with SerDes design team at Oracle Corporation, where he worked on circuit design and architecture modeling. Prior to that, he worked on SerDes characterization at Texas Instruments, Dallas. His current interests are SerDes architecture development and system level modeling, high speed mixed-signal circuit design and optimization.

The basic equalization schemes include a TX FFE and RX CTLE and DFE. RX side FFE for 112G is being discussed. The CDR sampling algorithm assumes the Mueller-Muller baud-rate phase detector. Assumptions of system jitter and noise are also made for the analysis. The best equalization that optimizes the signal SNR at the data slicer is obtained by sweeping-mode computations that, on the one hand, tries to minimize residual ISI and reflection effect, while, on the other, attempts to restrict the overall noise seen at the data slicer. Computations are based on end-to-end single bit response (SBR) and are performed statistically. Note that the DFE block should be removed from Figure 1.

A target BER, called detection error ratio, DER_0 , is an input parameter. The obtained signal SNR at the data slicer is compared against the required SNR to achieve the desired DER_0 . The difference is the COM margin, or simply COM. COM is usually set to 3dB, which is justified as implementation details have not been accounted for in the discussed computation.

3. PAM4 in Brief

In NRZ signaling one bit is a symbol, which has two values forming one eye. This is captured on the left side of Figure 2. For PAM4, two bits are grouped and mapped to one symbol; 2-bits has 4 unique combinations, thus 4 distinct levels and 3 vertical eyes. The mapping of two bits to a PAM4 symbol can be through Linear coding or Gray coding; the latter is standardized. More details can be found in PAM4 tutorials [3] and [4].

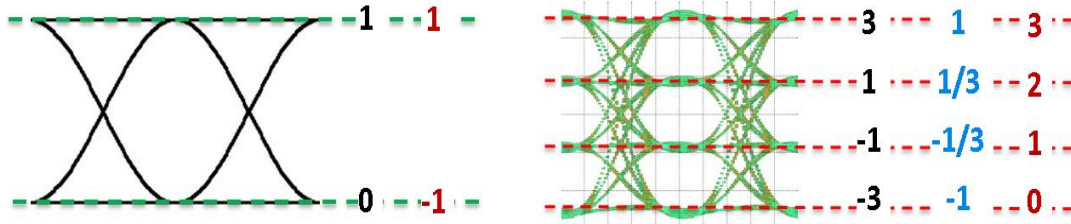


Figure 2. Comparing NRZ and PAM4 signaling.

Figure 3 shows the signal power spectral density (PSD) for NRZ and PAM4. It is seen that the Nyquist frequency for PAM4 is half of that of NRZ. Thus, PAM4 requires only half the bandwidth of that of NRZ. This is straightforward since one symbol duration for PAM4 is twice as long as that of NRZ. However, comparing with NRZ, except the bandwidth requirement relax, PAM4 is a lot more demanding and the resultant system is full of challenges. Thus, analysis and simulation accuracy matter even more.

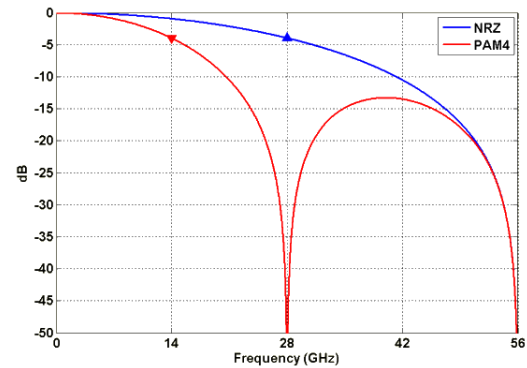


Figure 3. PSD for NRZ and PAM4.

An important concept, PAR (Peak to Average Ratio), is reviewed in this section as it is used in COM quite a lot. PAR is the ratio of peak signal power over the average signal power. Using the term L in COM for the number of signal levels, 2 for NRZ and 4 for PAM4, the average signal power is given in Eq. (1). This is the very same equation as (93A-29) for σ_x^2 in [1].

$$\sigma_x^2 = P_{avg} = \frac{2}{L} \cdot \sum_{k=1,3,\dots,L-1} \left(\frac{k}{L-1} \right)^2 = \begin{cases} 1, & \text{for NRZ} \\ \frac{5}{9}, & \text{for PAM4} \end{cases} \quad \text{Eq. (1)}$$

But why is this concept important? Figure 4 shows that the PAM4 eye height is 1/3 of that of NRZ, since practically, for the same signal amplitude, the peak signal is the same for any signal modulation. Consequently, the signal loss for PAM4 is $20 \cdot \log_{10}(1/3) = \sim -9.5\text{dB}$. However, the SNR loss is $20 \cdot \log_{10}(((1/3))/\sigma_x) = \sim 7\text{dB}$. The implication is then (a) if the degradation is dominated by noise, SNR loss from NRZ to PAM4 is close to 9.5dB; (b) if impairment is dominated by residual ISI, reflections, and crosstalk (assuming PAM4 is also the source of aggressors), the SNR loss is only about 7dB.

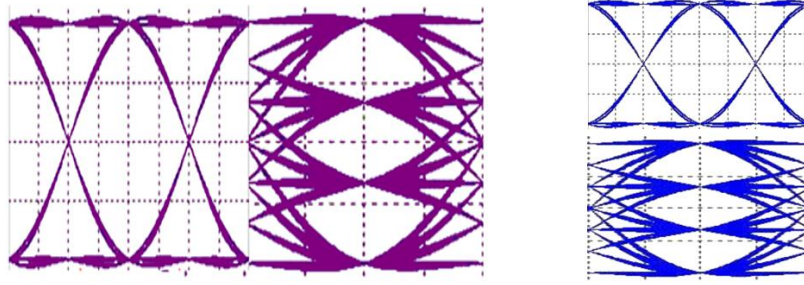


Figure 4. NRZ and PAM4 eye diagram comparison.

An example running COM for the same setup and same baud rate between NRZ and PAM4 shows the COM difference is 8.36dB, falling between 7dB and 9.5dB (Figure 5). In reality, as impairments and non-idealities are more detrimental to PAM4, the SNR difference could be much more than 9.5dB.

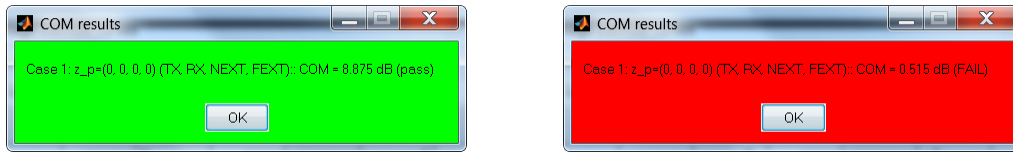


Figure 5. COM example between NRZ and PAM4 for the same baud rate.

4. Data Sampling Time in COM

The sampling time, t_s , is determined by (93A–25) in [1]. The sampling time is illustrated in Figure 6 copied from [6]. In the equation, $b(1)$ is the DFE tap-1 coefficient. If there are multiple values of t_s that satisfy the equation, then the first value prior to the peak of $h^{(0)}(t_s)$ is selected. The superscript $^{(0)}$ implies the THRU channel. Note that $h^{(0)}(t_s + T_b)$ is the SBR before DFE $b(1)$ is applied.

$$h^{(0)}(t_s - T_b) = h^{(0)}(t_s + T_b) - h^{(0)}(t_s)b(1) \quad (93A-25)$$

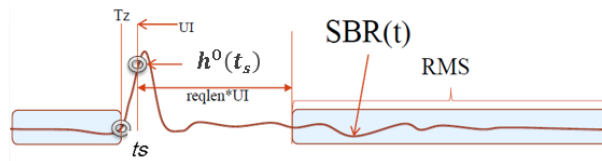


Figure 6. COM sampling phase emulating Mueller-Muller Baud-Rate Phase Detector.

As long as $b(1)$ is not excessively large (default to no bigger than 0.7), $h^{(0)}(t_s - T_b) = 0$. It is noted that although the choice of t_s reduces the impact of pre-cursor ISI, it is usually at the expense of moving the sampling phase left, and sometimes way left, of the SBR peak, thus increasing $b(1)$, due to both reduced $h^{(0)}(t_s)$ and increased $h^{(0)}(t_s + T_b)$. The consequence is discussed more thoroughly in Section 9.

5. DFE Tap Coefficients

The DFE tap coefficients, $b(n)$, are computed based on Equation (93A-26). $b(n) = 0$ if N_b is set to 0, i.e., no DFE is applied. The DFE is very ideal with infinite tap coefficient resolution. Thus, post-cursor ISI's are subtracted out completely if $b(n)$ is within the limits. Jitter impact on DFE feedback is approximately covered using the approach in Section 6.

$$b(n) = \left\{ \begin{array}{ll} -b_{\max}(n) & h^{(0)}(t_s + nT_b)/h^{(0)}(t_s) < -b_{\max}(n) \\ b_{\max}(n) & h^{(0)}(t_s + nT_b)/h^{(0)}(t_s) > b_{\max}(n) \\ h^{(0)}(t_s + nT_b)/h^{(0)}(t_s) & \text{otherwise} \end{array} \right\} \quad (93A-26)$$

DFE tap value range is defined. The default values for different standards are different. For example, in [12] Clause 21: CEI-56G-LR-PAM4 Long Reach Interface, COM parameters for DFE are defined (Table21-1) as replotted in Table 1.

Table 1. COM parameter for DFE specified in CEI-56G-LR-PAM4.

Parameter	Symbol	Value
Decision feedback equalizer (DFE) length	N_b	12
Normalized DFE coefficient magnitude limit for $n = 2$ to N_b	$b_{\max}(1)$ $b_{\max}(2-N_b)$	0.7 0.2

An illustration of DFE application to post-cursor removal from [9] is duplicated in Figure 7. In the example, it is seen that $b(1)$ is almost as large as $h^0(t_s)$. This is practically okay for the NRZ case if DER_0 is very small, for instance, $1E-15$. However, for 56G and 112G PAM4 most standards specify the raw BER between $1e-6$ to $1e-4$. The impact on real channel performance might be huge. This is discussed in Section 9.

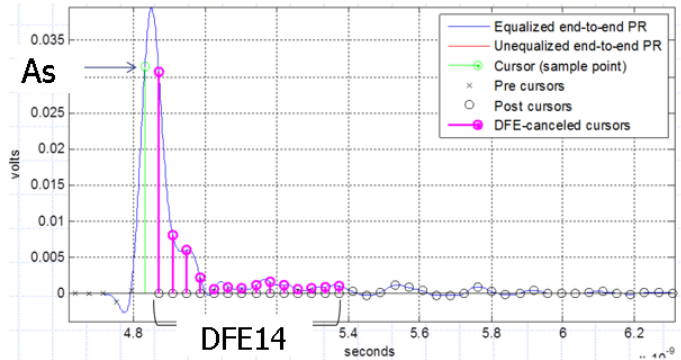


Figure 7. SBR before and after a 14-tap DFE.

6. Treatment of Jitter in COM

In COM jitter impact is converted to signal amplitude error before SNR is computed. The equalized SBR slope for the THRU path, $h_f(n)$, is described in Equation (93A-28) in [1]. The variance of the amplitude error due to timing jitter is computed per (93A-32). Figure 8 can assist the understanding of (93A-28).

$$h_f(n) = \frac{h^{(0)}(t_s + (n + 1/M)T_b) - h^{(0)}(t_s + (n - 1/M)T_b)}{2/M} \quad (93A-28)$$

$$\sigma_J^2 = (A_{DD}^2 + \sigma_{RJ}^2) \sigma_X^2 \sum_n h_f^2(n) \quad (93A-32)$$

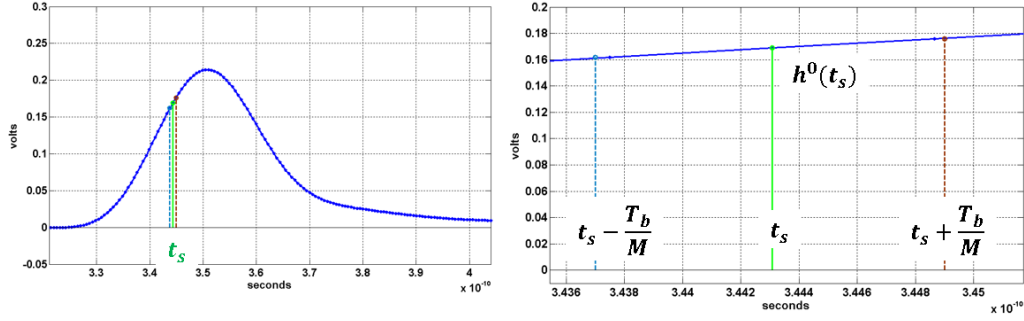


Figure 8. Signal slope based on SBR defined in (93A-28).

In (93A-32), A_{DD} represents Dual-Dirac jitter, thus its variance is the same as its peak value. A_{DD} is power-summed with the random jitter. The use of σ_x is due to the fact that the average signal strength needs to be scaled. However, when R_{LM} is smaller than 1, typically the middle eye is larger than the outer eyes, implying the scaling factor σ_x should be slightly larger than 0.7454. Thus, Equation (93A-32) could underestimate the jitter impact.

Now, what if t_s is around the peak of the SBR? In this case, $h_j(0) \approx 0$ and the jitter effect is nullified. We could improve Equation (93A-28) by making the jitter contribution more accurately assessed by considering the variance on each side of t_s and then taking the mean of the two.

7. TX Output Level Separation Mismatch, R_{LM}

PAM4 signal has one parameter for the TX called the level separation mismatch ratio, R_{LM} . This does not apply to NRZ. Its computation via Eq. (2) can easily be understood from Figure 9. R_{LM} is typically specified no smaller than 0.95. However, how the four levels are distributed is not specified.

$$S_{min} = \frac{\min(V_D - V_C, V_C - V_B, V_B - V_A)}{2}, \quad R_{LM} = \frac{6 \cdot S_{min}}{V_D - V_A} \quad \text{Eq. (2)}$$

The available signal A_s for NRZ is well illustrated in [9] and reproduced in Figure 10. COM treats NRZ and PAM4 with a unified approach. For PAM4 ($L = 3$) the available signal is the scaled version of $A_s = h^0(t_s)/3$. Thus, the available signal A_s expressed in Eq. (3) implies that the smallest eye is used. This is slightly on the pessimistic side since all three eyes contribute to system errors.

$$A_s = R_{LM} \cdot h^{(0)}(t_s)/(L - 1) \quad \text{Eq. (3)}$$

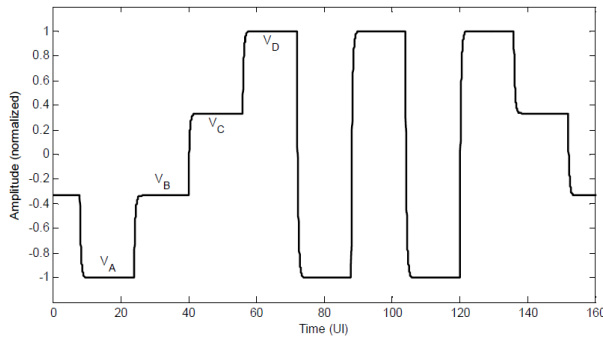


Figure 9. R_{LM} measurement.

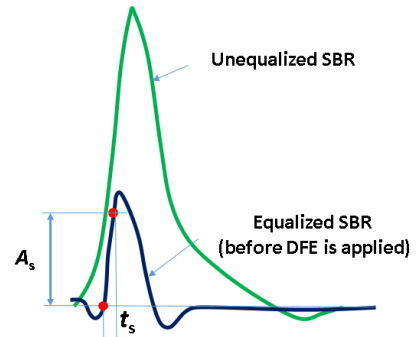


Figure 10. Available signal A_s .

8. CTLE in COM

There are two stages of CLTE specified in COM for CEI-56G-LR-PAM4. Details can be found in Table21-1 in [12], reproduced in Table 2. The two CTLE transfer functions can be mathematically expressed in Eq. (4) and (5). Note that for CTLE2, a second pole and a scaling factor, both f_{p2} , are added in this paper, as shown in Eq. (5).

$$H_{CTLE}(f) = f_{p2} \cdot \frac{j \cdot f + f_z \cdot 10^{\frac{G_{DC}}{20}}}{(j \cdot f + f_{p1}) \cdot (j \cdot f + f_{p2})} \quad \text{Eq. (4)}$$

$$H_{CTLE2}(f) = f_{p2} \cdot \frac{j \cdot f + f_{LF} \cdot 10^{\frac{G_{DC2}}{20}}}{(j \cdot f + f_{LF}) \cdot (j \cdot f + f_{p2})} \quad \text{Eq. (5)}$$

Table 2. COM CTLE parameters for CEI-56G-LR-PAM4.

Parameter	Symbol	Value	Units
Continuous time filter, DC gain	g_{DC}		
Minimum value		-20	dB
Maximum value		0	dB
Step size		1	dB
Continuous time filter, DC gain2	g_{DC2}		
Minimum value		-6	dB
Maximum value		0	dB
Step size		1	dB
Continuous time filter, scaled zero frequency	f_z	$f_b/2.5$	GHz
Continuous time filter, pole frequencies	f_{p1} f_{p2}	$f_b/2.5$ f_b	GHz GHz
Continuous time filter, low frequency pole/scaled zero	f_{LF}	$f_b/40$	GHz

The magnitude transfer functions for the two CTLE's are plotted in Figure 11. The HF peaking frequency is just above the Nyquist, while the LF peaking frequency is about 1/3 of the Nyquist.

It is seen that for the HF stage, the peaking could be as much as 17dB. This is practically very challenging to design in one stage. Thus, it is suggested to put more high frequency poles to represent the parasitic loading.

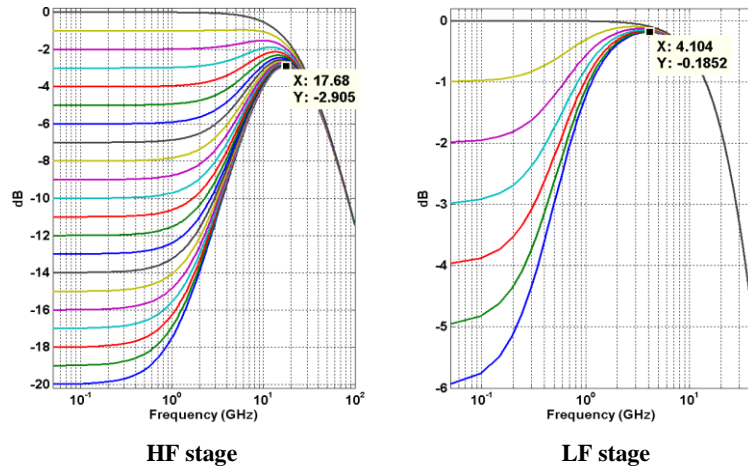


Figure 11. COM CTLE magnitude TF example.

9. COM Margin

In order to speed up the computation, FOM is firstly computed to decide the optimal equalization settings, (93A-36). Once the optimal settings are obtained, COM is computed. Note that the best FOM does not always lead to the largest COM, so the use of FOM is a trade-off between accuracy and efficiency.

$$FOM = 10 \log_{10} \left(\frac{A_s^2}{\sigma_{TX}^2 + \sigma_{ISI}^2 + \sigma_J^2 + \sigma_{XT}^2 + \sigma_N^2} \right) \quad (93A-36)$$

The five terms in the denominator in (93A-36) are briefly explained below:

- (1) The noise output from the TX, (93A-30). For the given SNR_{TX} , the larger the TX signal (A_v), the larger the noise. The simplified scaling with $[h^0(t_s)]^2$ does not include frequency dependency effect.

$$\sigma_{TX}^2 = [h^{(0)}(t_s)]^2 10^{-SNR_{TX}/10} \quad (93A-30)$$

- (2) Residual ISI, (93A-31). The factor σ_x is used. When R_{LM} is less than 1, it is a little optimistic.

$$\sigma_{ISI}^2 = \sigma_X^2 \sum_n h_{ISI}^2(n) \quad (93A-31)$$

- (3) The variance of the amplitude error due to timing jitter. This was discussed above in Section 6.
- (4) The variance of the amplitude for the combination of all crosstalk paths, (93A-33) and (93A-34). The choice is that FEXT channels are reshaped by both TX FFE and CTLE, while the NEXT are only modified by the CTLE. Other blocks affecting the crosstalk strength can be figured out in Figure 1.

$$[\sigma_m^{(k)}]^2 = \sigma_X^2 \sum_n [h^{(k)}((m/M+n)T_b)]^2 \quad (93A-33)$$

$$\sigma_{XT}^2 = \sum_{k=1}^{K-1} [\sigma_i^{(k)}]^2 \quad (93A-34)$$

- (5) The variance of the noise at the output of the receive equalizer, (93A-35).

$$\sigma_N^2 = \eta_0 \int_0^\infty |H_r(f)H_{ctf}(f)|^2 df \quad (93A-35)$$

The combination of values (t_s , TX FFE coefficients, CTLE settings, and DFE coefficients) that maximized the FOM is recorded to compute COM in Eq. (6). Now, the denominator in (93A-36) is replaced by using interference PDFs at the given DER_0 to compute the noise amplitude at DER_0 , A_{ni} . The total distribution via convolutions is used for the CDF integration.

$$COM = 20 \cdot \log_{10}(A_s/A_{ni}) \quad \text{Eq. (6)}$$

It should be pointed out that, since NRZ and PAM4 both use “a single eye” concept, the conversion formulation in COM from DER_0 to SNR might not be accurate for PAM4. Assuming PAM4 adopts Gray coding as is called for in standards, BER can be approximately treated as half of SER. Thus, the relationship between BER and SNR can be derived as Eq. (7). $k = 1/2$ for NRZ and $k = 3/8$ for PAM4. Consequently, A_{ni} in Eq.(6) should be modified accordingly in the current COM code.

$$BER = k \cdot \text{erfc}\left(\frac{h_0/\sigma_{total}}{\sqrt{2}}\right) \quad \text{Eq. (7)}$$

10. DFE Error Propagation Impact

Figure 12 shows a 1-tap DFE model for studying error propagation. Multiple-tap DFE can be analyzed in the same manner, but the problem becomes much more complicated. The signal y_k before the slicer can be expressed as shown in Eq. (8), where a_{k-1} is the previously transmitted symbol. \hat{a}_{k-1} is the detected symbol. If a_{k-1} and \hat{a}_{k-1} differ, a symbol error occurs. The feedback term is now wrong and the ISI correction is also wrong. This could potentially cause the signal at the slicer to be incorrectly detected for the next symbol, thus the occurrence of error propagation (EP).

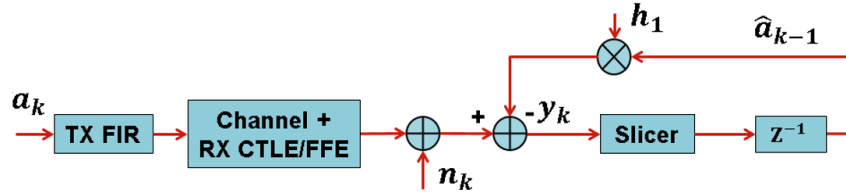


Figure 12. 1-tap DFE model for error propagation studies.

$$y_k = a_k + h_1 \cdot (a_{k-1} - \hat{a}_{k-1}) + n_k + \text{residual ISI} \quad \text{Eq. (8)}$$

If we assume that ISI is completely removed by the equalizer, the EP probability for a single tap DFE can be computed. This is shown on the left in Figure 13. The average burst symbol error length, L_{avg} , can be derived as shown in Eq. (9), which is also plotted on the right side of the figure. It is seen that for a single tap DFE architecture, the worst case P_{EP} is 0.75 and L_{avg} is 4. For multi-tap DFE architecture with large tap coefficients and certain channel loss and reflection profiles, the error propagation could be much more severe such that the FEC loses its correction capability.

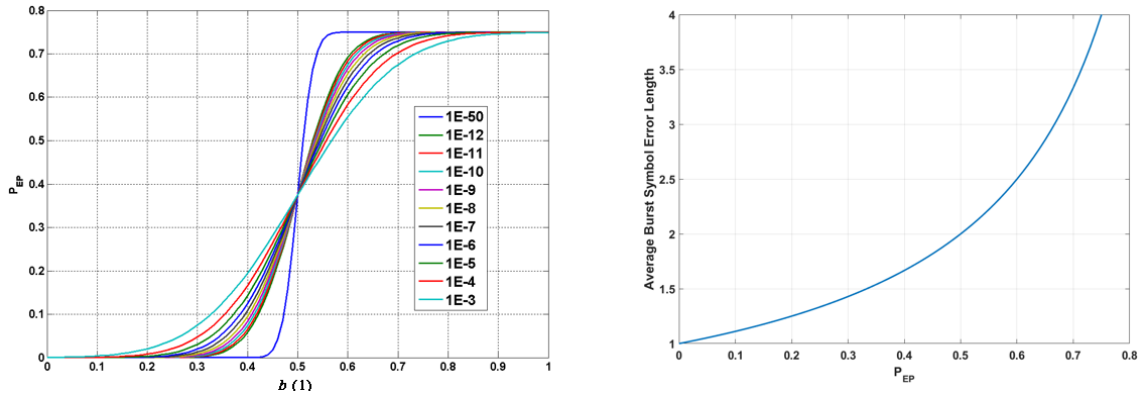


Figure 13. EP probability for 1-tap DFE for PAM4 under different BER levels.

$$L_{avg} = \frac{1}{1-P_{EP}} \quad \text{Eq. (9)}$$

However, since DFE is applied to the SBR before COM is computed, EP does not exist and is not part of the COM margin. An example is shown in Figure 14 with a 12-tap DFE, which is the default setting in CEI-56G-LR-PAM4. The system is analyzed and obtained that the SER without DFE EP is 1.0324e-6. The details of DFE EP effect will wait until the next section. It should be emphasized that the DFE tap coefficients chosen as examples are well within the limits specified in COM in CEI-56G-LR-PAM4.

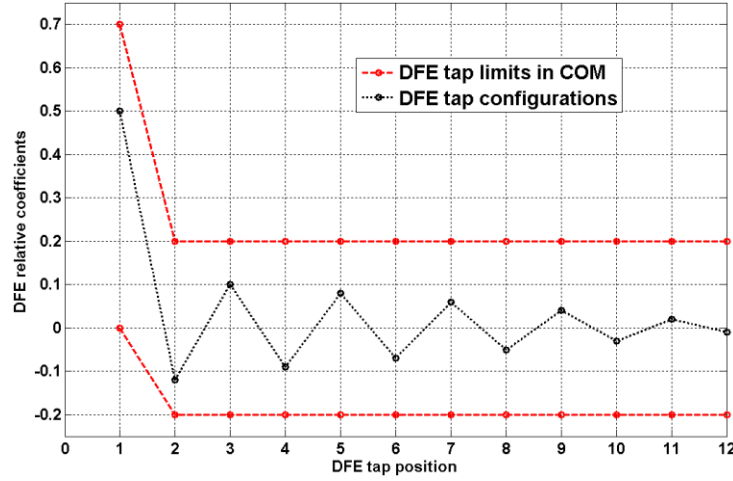


Figure 14. Two DFE coefficient settings.

The burst error length can be literally defined as a block of symbols in which every symbol is wrong. However, burst error length is more appropriately defined as a block of errors, in which the first symbol error is preceded by at least N_b error-free symbols, as well as followed by at least N_b error-free symbols. N_b is often referred to as the guard band. This is illustrated in Figure 15. “1” indicates an erred symbol and “0” a correct symbol. Naturally, for a 1-tap DFE burst PAM4 symbol errors must be consecutive.

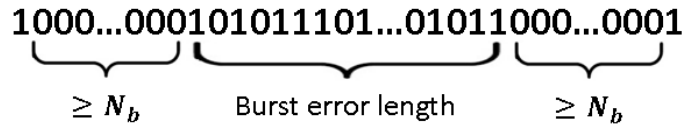


Figure 15. Burst error length definition.

11. FEC Fundamentals

Forward Error Correction (FEC) is widely used to help correct link errors so that the resultant BER meets the application requirement. Only the Reed-Solomon FEC (RS KP4 FEC) adopted in IEEE P802.3bj and P802.3bs and a bunch other standards for PAM4 is used to illustrate FEC correction capability.

FEC encoding introduces redundancy into a frame of bits, called the codeword: A block of k data symbols becomes a codeword of n symbols, (n, k) . The FEC decoding finds the decoded codeword that is closest to the received codeword.

The FEC coding gain (CG) is defined as the reduction in the required SNR that can be accommodated while still achieving the desired BER. An illustration of CG is shown in Figure 16, where AWGN noise is assumed [11]. Under typical operating conditions, measurements from system houses showed that KP4 FEC can achieve up to 8 dB in CG. The exact CG value is a function of BER and error signature.

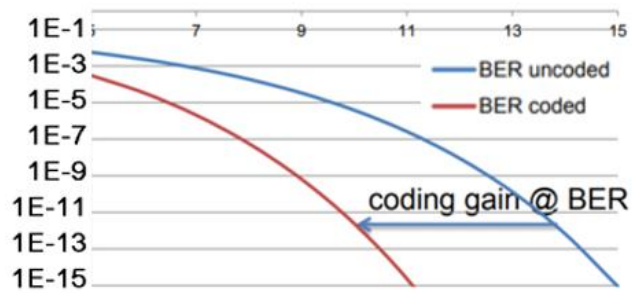


Figure 16. Illustration of FEC coding gain.

The KP4 FEC, $RS(544, 514, T=15, M=10)$, implies that, in a codeword, 514 FEC symbols are encoded to form 544 FEC symbols. Each FEC symbol contains $M (=10)$ bits. The FEC can correct up to $T (=15)$ symbol errors within each codeword, regardless of number of bit errors. This implies that (i) at its most effective, KP4-FEC can correct as many as 150 bit errors in a codeword; (ii) In the other extreme, KP4-FEC can correct no more than 15 bit errors in 5440 bits, if 16 bit errors scatter over 16 FEC symbols.

What should be pointed out is that if the FEC symbol errors exceed the correction capability, the whole codeword is non-correctable, thus discarded. The implication is that for really bad BER plus bad error signature, the FEC output BER could be worse than the input BER.

The simulation result for a hypothetical DFE setting described in Figure 14 is given in Table 3, together with the case without DFE, hence no DFE EP, but at much higher noise, thus higher SER. It is seen that

- The SER increase after DFE is not alarmingly large; the raw BER is still better than specs.
- The “average burst error length” is larger than the “SER ratio with EP” in the DFE case.
- The $RS(544, 514)$ KP4 FEC fails completely even with limited sample size in the example.
- Error signature is more relevant than BER level itself in assessing FEC correction capability.
- Without DFE EP the FEC can correct all the errors even though SER is two orders worse.

It cannot be over emphasized that when DFE is a part of the equalization scheme and the DFE coefficients are relatively large, COM result should not be taken at its face value. Although COM does not currently support it, the user can modify the COM value by including a penalty factor with the knowledge of the DFE settings.

Table 3. KP4 FEC performance with the presence of DFE EP.

Raw SER	SER with EP	SER ratio after EP	Max burst error length	Average burst error length	Max KP4 FEC symbol errors
1.0324e-6	3.3779e-6	3.2719	81	4.2757	17 (>15)
1.0050e-4	n/a	n/a	2	2	6 (<16)

12. Summary and Future Work

COM is a great tool for qualifying a high speed serial link channels. This paper focused on the COM for PAM4 signaling. We particularly analyzed

- The potential impact from the sampling time and the DFE error propagations
- KP4 FEC is discussed to provide a basic idea of error correction
- An example of DFE EP is provided to show that even DFE tap coefficients are well within the COM limits, the FEC can become dysfunctional
- Running COM to get the SNR margin does not guarantee the system to meet the desired performance

Future work includes the following

- DFE error propagation in a PAM4 link with multiple DFE taps
- Error signature and its impact on FEC coding gain analysis
- Precoding effect in terms of burst error removal

References

- [1] IEEE P802.3bj™/D3.2, 11th April 2014, “Draft Standard for Ethernet Amendment 2: Physical Layer Specifications and Management Parameters for 100 Gbps Operation Over Backplanes and Copper Cables”, Prepared by the LAN/MAN Standards Committee of the IEEE Computer Society
- [2] Richard Mellitz, et al, “Channel Operating Margin (COM): Evolution of Channel Specifications for 25 Gbps and Beyond”, DesignCon 2013
- [3] Geoff Zhang, et al, “PAM4 Signaling for 56G Serial Link Applications – A Tutorial”, DesignCon 2016
- [4] Geoff Zhang, et al, “A Tutorial on PAM4 Signaling for 56G Serial Link Applications”, DesignCon 2017
- [5] Adam Healey, “Issues with sampling time and jitter in Annex 93A”, IEEE P802.3bj Task Force, May 2013
- [6] Richard Mellitz, et al, “Time-Domain Channel Specification: Proposal for Backplane Channel Characteristic Sections “, IEEE802.3bj, July 2012, San Diego, CA
- [7] A. Ran, November 2014, available online at http://www.ieee802.org/3/bj/public/tools/ran_com_3bj_3bm_01_1114.zip
- [8] Adam Healey, et al, “Channel Operating Margin for 56 Gbps PAM4 Chip-to-Chip and Backplane Interfaces”, DesignCon 2016
- [9] Richard Mellitz, “Various Topics for Computing Channel Operating Margin (COM) - 100 Gb/s Ethernet backplane and copper cable channel specification... A new signal integrity”, 2/22/2014
- [10] Yasuo Hidaka, “Problems of high DFE coefficients”, Fujitsu, IEEE P802.3by 25 Gb/s Ethernet Task Force, September 2, 2015
- [11] Shu Lin, et al, “A Brief Tour of FEC for Serial Link Systems”, DesignCon 2015
- [12] Implementation Agreement OIF-CEI-04.0, “Common Electrical I/O (CEI) – Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps I/O and 56G+ bps”, December 29, 2017
- [13] Yasuo Hidaka, “BER margin of COM 3dB”, Fujitsu, IEEE P802.3by 25 Gb/s Ethernet Task Force, September 9, 2015