EDI CON 2018
Electronic Design Innovation Conference & Exhibition
October 17-19 2018
Santa Clara Convention Center
Santa Clara, CA

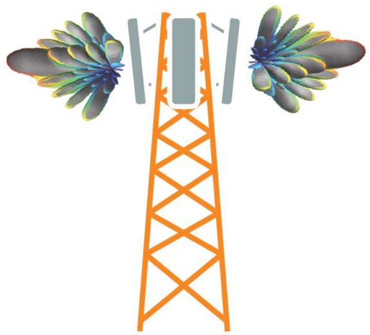
All-Silicon Active Antennas for High Performance mmWave Systems

Alastair Upton
Ian Gresham

Anokiwave, Inc.
Billerica, MA, USA

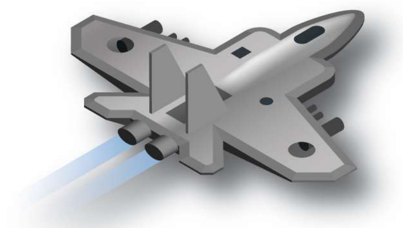
Anokiwave

Several major markets for mmWave systems and RFICs are emerging



5G

SATCOM



A/D RADAR

5G

- High power gNodeB
- Fixed wireless access
- Small cell access point
- Indoor/outdoor CPE
- Mobile devices
- Automotive, V2X

SATCOM

- Ku Band terminal
- Ka Band terminal
- Airborne arrays
- Marine terminal
- Remote area internet access

A/D RADAR

- Military communication
- X and Ku-Band radar
- mmWave radar

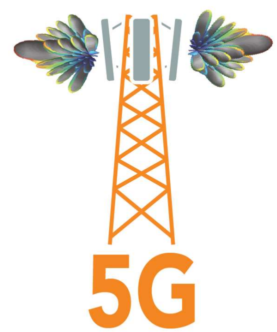
For 5G mmWave to develop the way we want, then two factors need to be addressed

Technical Factors

- Link budget (EIRP, EIS, …)
- Power dissipation
- System size* and weight
- 3GPP Standards

……………………………………

- High $\frac{EIRP\ (W)}{Pdiss\ (W)}$ ratio
- Low ACLR, EVM
- Low noise figure
- Transient performance
- On-chip telemetry



All-Silicon mmWave antennas address both factors

Economic Factors

- System development cost
- Operator's Capex
- Ongoing Opex
- Supply chain diversity

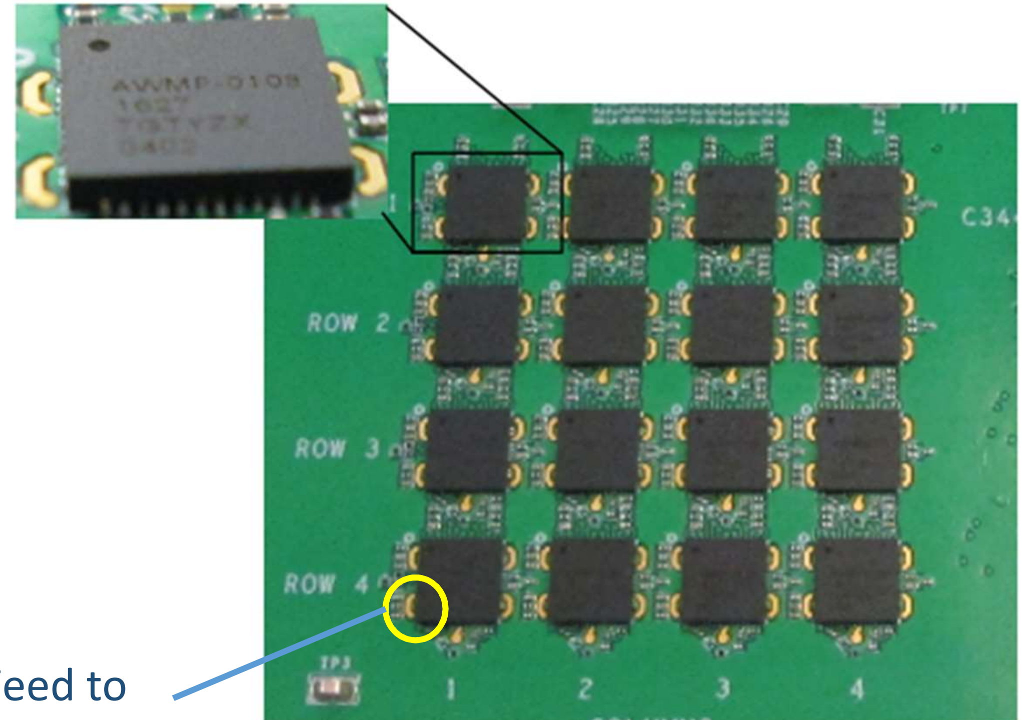
……………………………………

- Planar arrays
- Low cost silicon wafers
- Low prime power
- Minimal array calibration
- Remote monitoring
- Eco-system of array manufacturers

*Size is key issue for Regulatory Approval at local Government level

All-Silicon Array Architecture

Silicon Beamforming IC



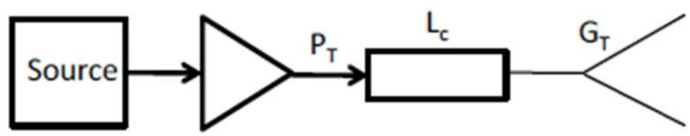
Feed to radiating element

- Batch manufacturing
- Part-to-part match/predictability
- Simplification of assembly and usage
- Robustness of performance and decay

- Pros
  - ICs reside completely within the lattice
  - Lowest possible feed loss
  - Best Tx EIRP efficiency
  - Best Rx NF
  - Full 2D scan
  - Single supply operation
  - Telemetry available
  - No array calibration
  - Lowest cost semiconductor processes in the world
- Cons
  - More ICs required
  - Lower conducted power per element than GaAs/GaN

EIRP vs. Conducted Power

The FCC defines EIRP as the sum of three logarithmic terms:



$$EIRP = P_T + G_T - L_C$$

* Path loss after signal amplification (TR switch + Transmission Line + Antenna Feed) wastes power *at the most valuable point in the system*
* Excess power dissipated in the interconnect loss is converted to thermal energy (bad) and requires a larger (more expensive) PSU than required

- Power dissipation/optimization is a holistic assessment of the entire path/system
- Active antenna efficiency/functionality needs to consider *all elements in the signal path AND control path of the sub-array* for an apples-apples comparison
- Non-signal path functions include embedded controllers and the PSU
- This function is normalized to the sub-array level to account for beam-forming architecture (hybrid/analog/digital)

EIRP should be maximized by controlling all three contributing terms:
- Maximizing conducted linear power for lowest power dissipation
- Increasing the available array gain to the maximum allowed by the application
- Minimizing the effect of system losses (which can be dramatic at mmWave)

Generating efficient, linear TX power at wide channel bandwidths is a critical challenge

- EIRP ∝ (No. Elements)^2
- Power dissipation ∝ (No. Elements)

  ∴ Larger arrays are better

  Cost and narrow beamwidth limit the size
- Efficiency is set by the **waveform**, <u>independent</u> of device technology (GaAs, GaN, SiGe, CMOS)
- 3% or -30dB EVM using 5G NR 400MHz waveform is a common requirement for OFDM 64QAM waveform
- Linear power is more important than P1dB

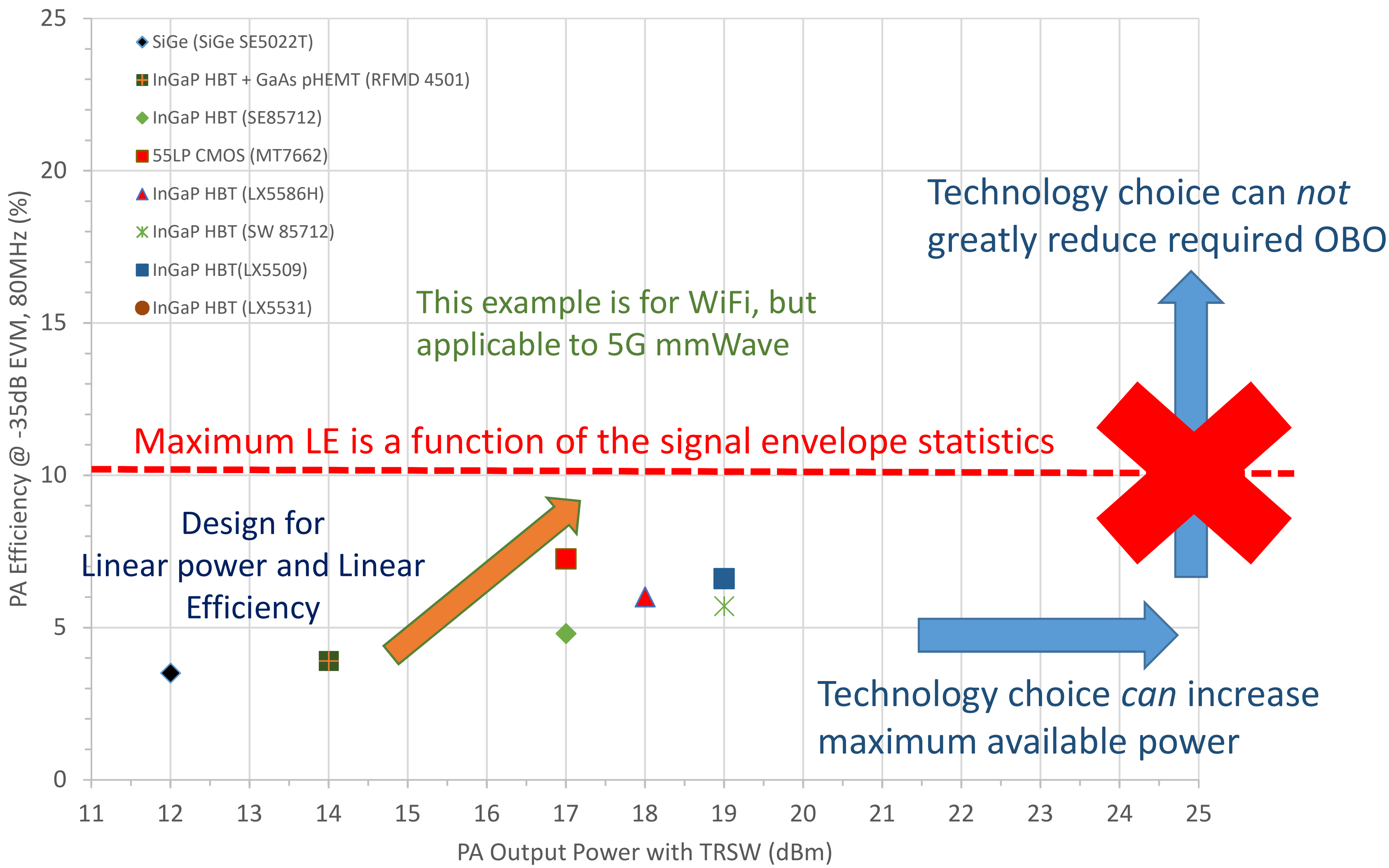
Evolution of Modern Communication Systems

	Standard	Bandwidth MHz	EVM dB	Waveform Modulation
WiFi	802.11b	20	-9	DQPSK
	802.11g/a	40	-25	OFDM
	802.11ac wave 1	80	-30	OFDM 256QAM
	802.11ac wave 2	160	-32	OFDM 256QAM
	802.11ax	160	-35	OFDM 1024QAM
Cellular	GSM	0.2	-23	GMSK-8PSK
	WCDMA	3.84	-15	QPSK
	LTE	20	-22	OFDM
	LTE-A	40	-27	OFDM
5G	5GTF	800	-30	OFDM 64QAM
	5G-NR	1400	-32	OFDM 256QAM

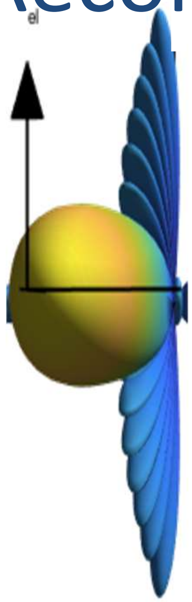
Increasing BW ↓   Decreasing EVM ↓

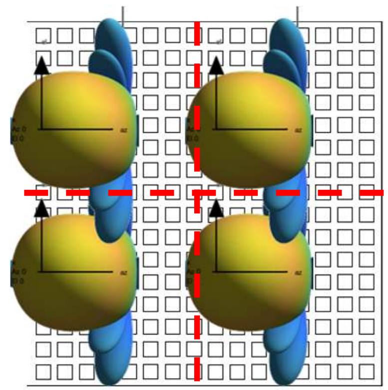
What level of output power back-off (OBO) is needed to meet the required EVM for low BER?

Circuit Efficiency for *Linear* Amplifiers



Reconfigurable 28GHz All-silicon Array





US Trade Compliant Solution (5A991.f)

Enables 4x4 MIMO

Full 2D scan for dense urban environments

- >1KW EIRP at OP1dB in 256-element mode (~ 65W P_{DISS})
- One 256 element beam or four 64 element beams
- 4x64 arrays for MU-MIMO
- Weather sealed for outside deployment
- Passive thermal management
- 26.4cm x 14.2cm x 6.9cm
- Mass: 3kg
- Embedded controller for simple UI
- Single 12V DC input

Technical Benefits of All-Silicon Arrays

Technical Factor	All-Silicon Arrays	Non-Silicon Arrays
Factory calibration	Quad architecture and ZERO-CAL™ ICs minimize calibration	Variation in process, line lengths, and temperature effects need calibration
Fast Beam Steering	Large number of beam state storage registers in CMOS	Long transient times limit Tx/Rx switching speed
Temperature Compensation	Temperature sensor and adjustment capability	Wide variations over -40 to +85°C needs calibration
Integration Level	4, 8 or 16 channels can be integrated on a single IC. On-chip SPI control	Limited integration capability. Separate SPI control IC needed

Economic Benefits of All-Silicon Arrays

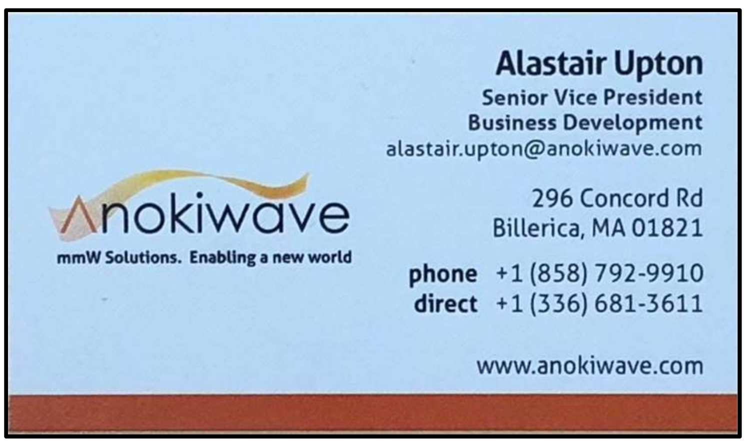
Economic Factor	All-Silicon Arrays	Non-Silicon Arrays
Several hundred million mmWave ICs per year are needed	300mm diameter CMOS wafers enable enough capacity	Limited capacity of small geometry (0.15 or 0.1um gate) compound semiconductors
Low price per radiating element in high volume	CMOS provides lowest cost semiconductor process	Difficult to meet cost targets
Low prime power and "Green" energy savings	Can dynamically turn off antenna elements for near and far users	No capability for dynamic energy savings

Summary

- mmW silicon core ICs for active antennas are commercially available now
- All-silicon, high efficiency planar arrays are in production today
  - 5G, SATCOM, A&D markets
- The momentum for increased industrialization is growing quickly
- We are beyond proof-of-concept and academic research
- Silicon provides a proven path to high volume manufacturing and the industrialization required to mass produce efficient, cost effective arrays


EDI
CON
2018
Electronic Design Innovation
Conference & Exhibition
October 17-19 2018
Santa Clara Convention Center
Santa Clara, CA

Thank You


Alastair Upton
Senior Vice President
Business Development
alastair.upton@anokiwave.com
Anokiwave
mmW Solutions. Enabling a new world
296 Concord Rd
Billerica, MA 01821
phone +1 (858) 792-9910
direct +1 (336) 681-3611
www.anokiwave.com


Ian Gresham, PhD
Technology Fellow/IEEE Fellow
ian.gresham@anokiwave.com
Anokiwave
296 Concord Road; M/S 120
Billerica, MA 01821
phone +(858) 792-9910
direct +(617) 955-6132
www.anokiwave.com