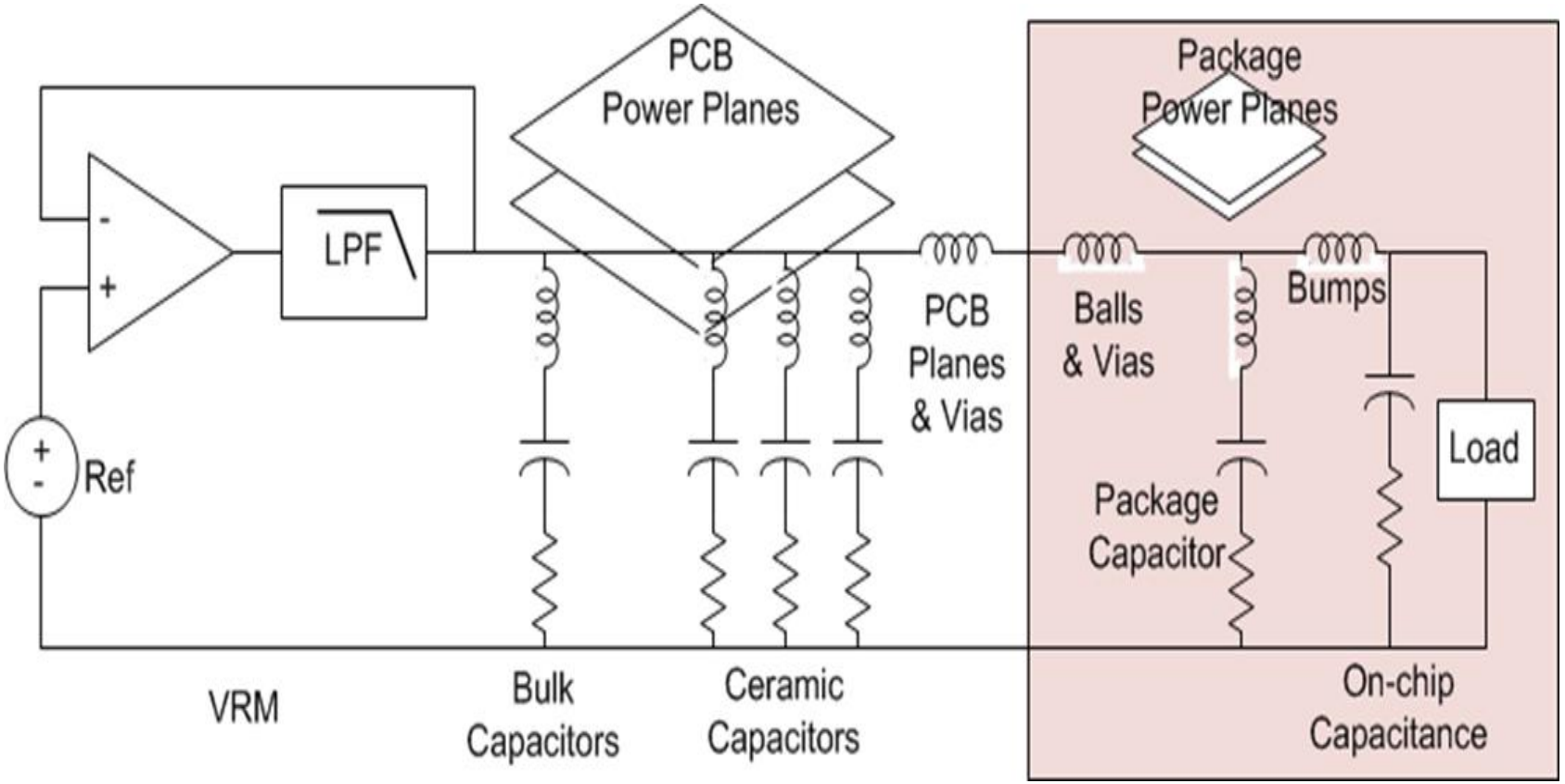
EDI CON 2018
Electronic Design Innovation Conference & Exhibition
October 17-19 2018
Santa Clara Convention Center
Santa Clara, CA

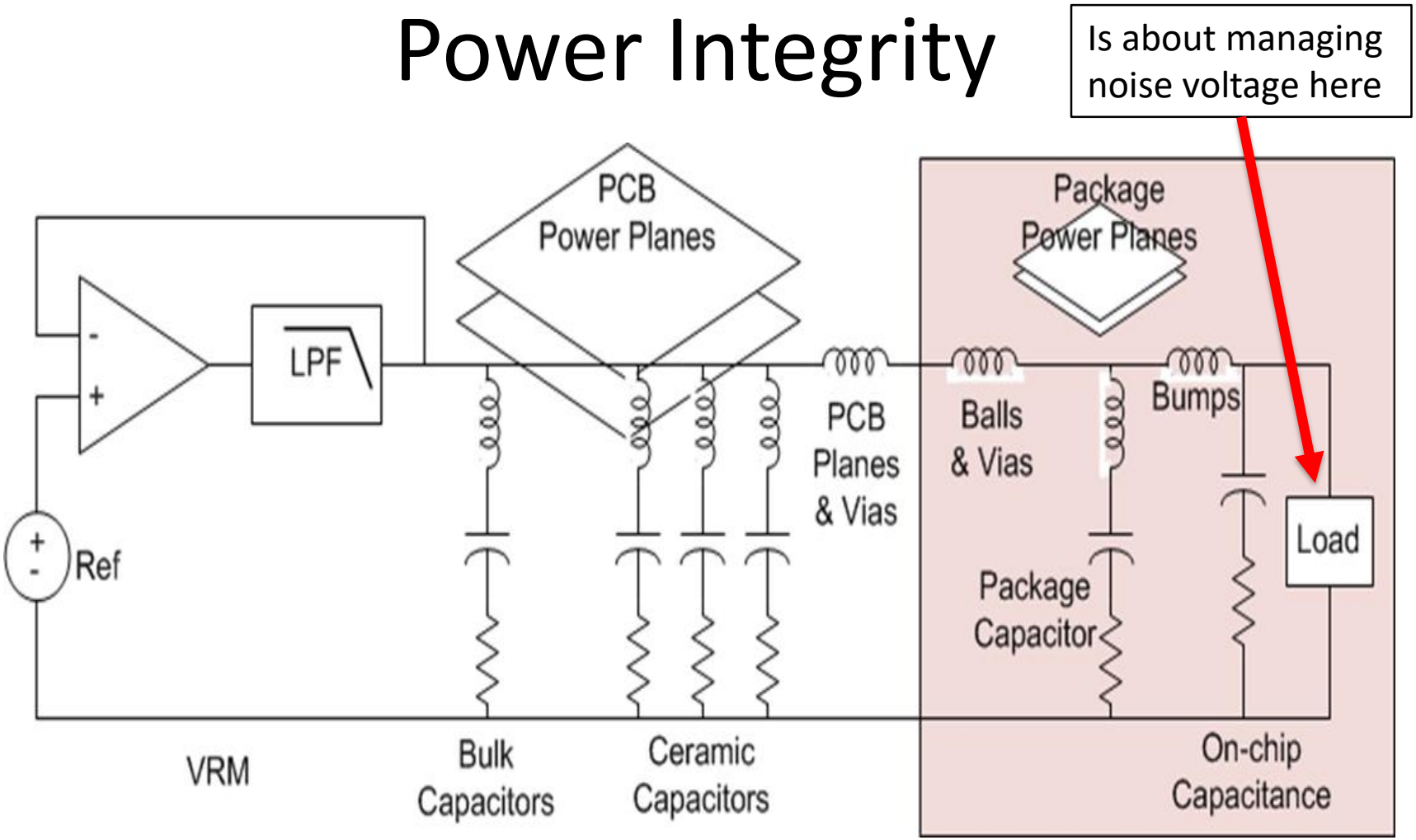
Power Distribution Network (PDN) Impedance and Target Impedance

Steve Sandler, Picotest
Eric Bogatin, Teledyne LeCroy
Larry Smith, PDNPowerIntegrity.com

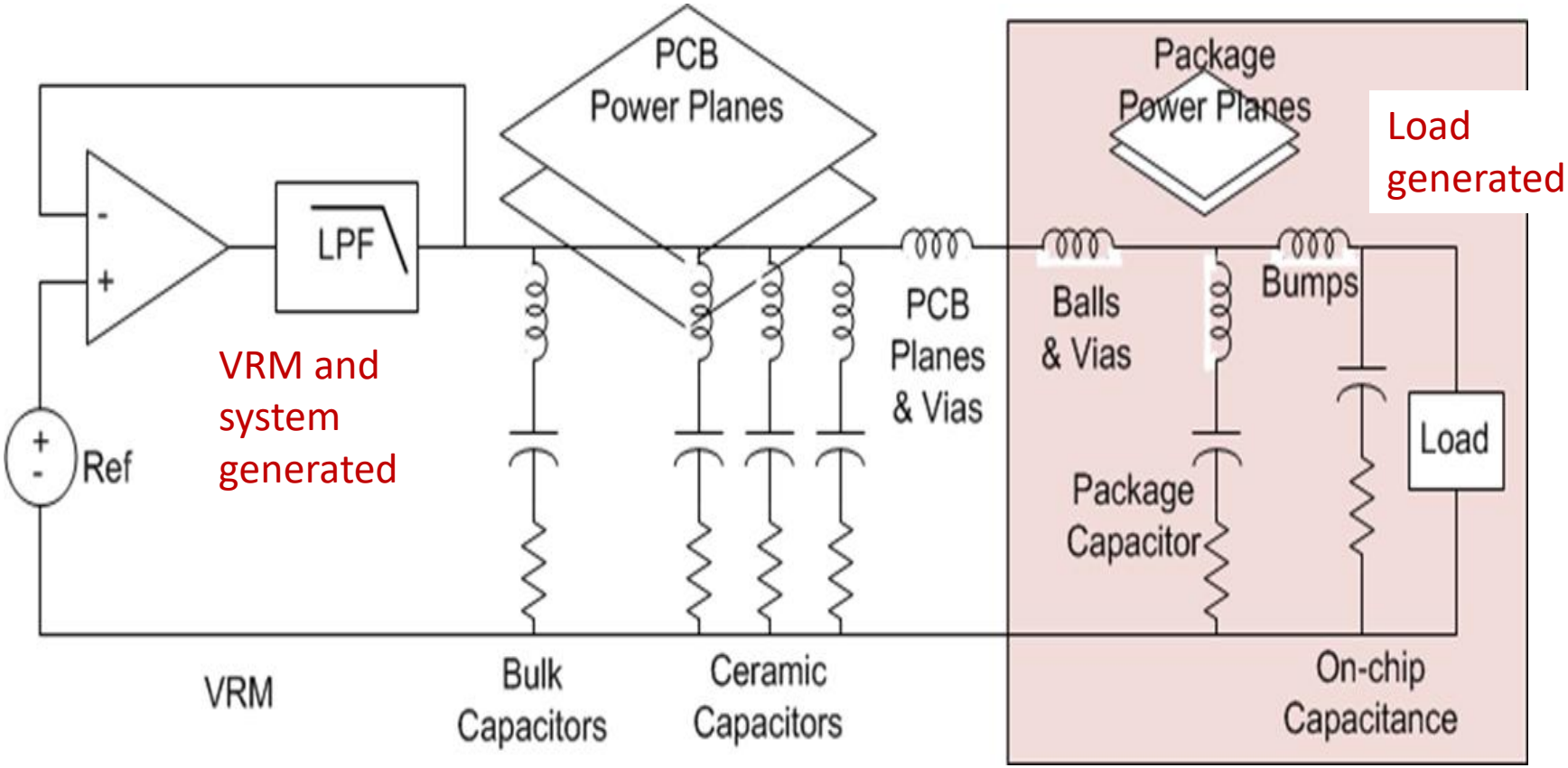
A Typical PDN



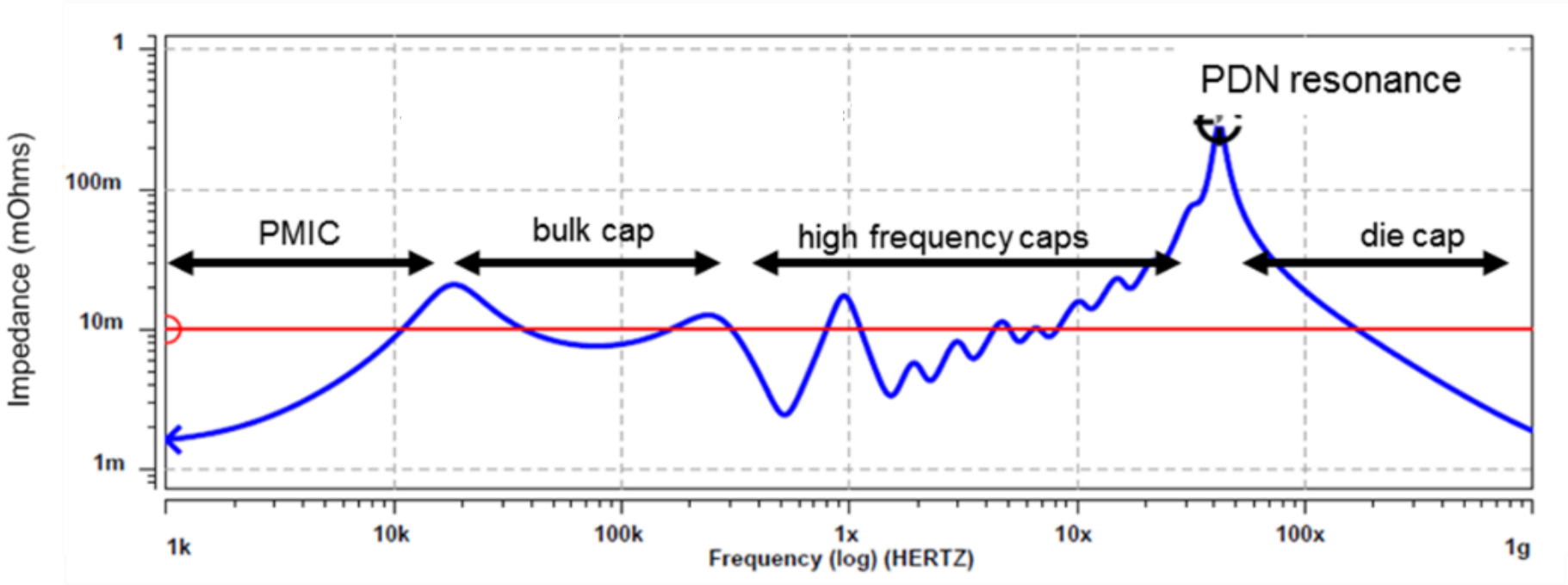
Power Integrity



Dual(ing) Noise Sources

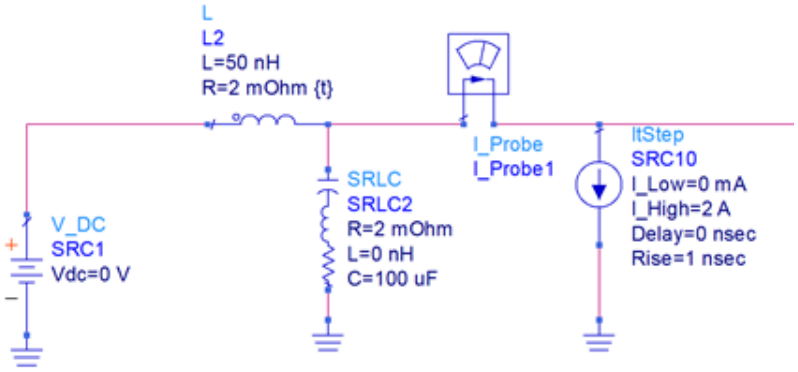


Flat Impedance is Ideal, but…



Impedance ignores the VRM generated noise

The Nature of a Peak

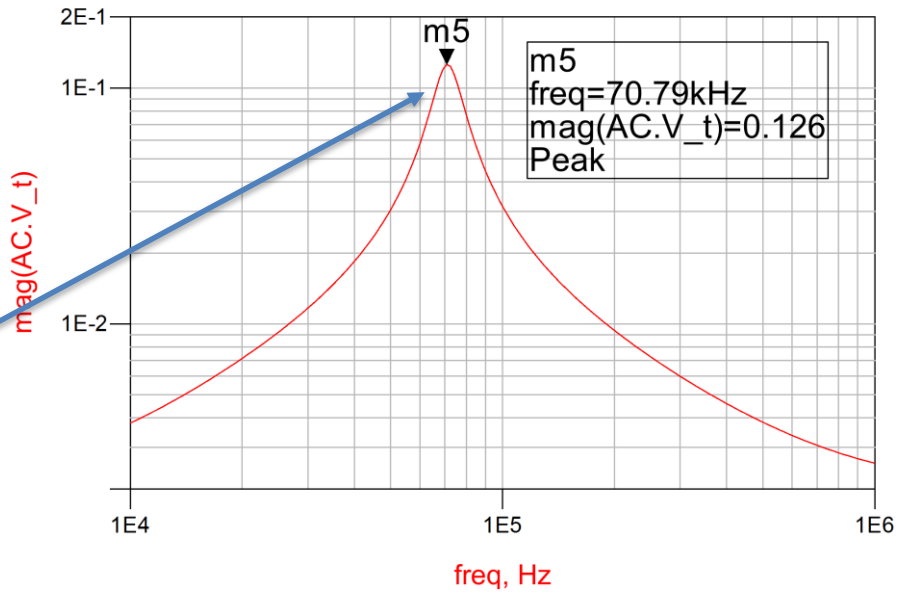


Single resonant circuit with a "target impedance" of 125mΩ is used to demonstrate the voltage response to a fixed dynamic current amplitude

$$Z_o = \sqrt{\frac{L}{C}} = \sqrt{\frac{50nH}{100uF}} = 22.4m\Omega$$

$$Q = \frac{Z_o}{R} = \frac{22.4m\Omega}{4m\Omega} = 5.6$$

$$Z_{pk} = Z_o \cdot Q = 125m\Omega$$



STEP PROFILE

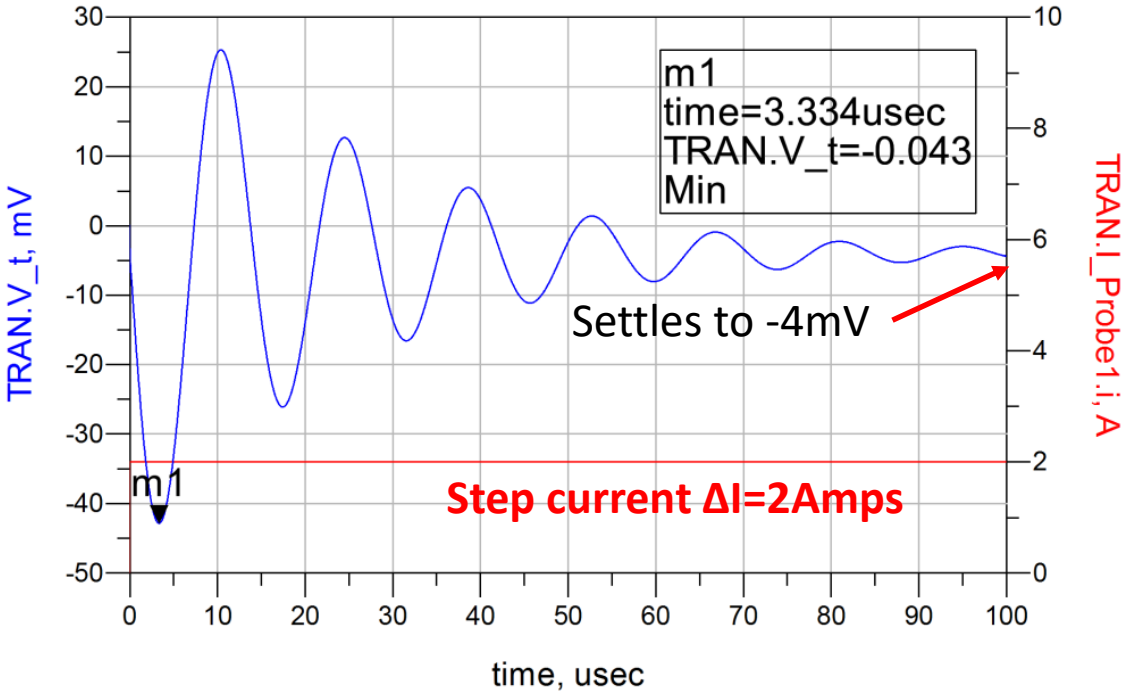
Laplace provides the time domain response

$$V(s) = \frac{1}{C} \cdot \frac{\Delta I}{\frac{1}{RC}s + \frac{1}{LC} + s^2}$$

Exponential decay

$$V(t) = \frac{\Delta I}{C \cdot \sqrt{{\omega_o}^2 - \alpha^2}} \cdot e^{-\alpha t} \cdot \sin\sqrt{({\omega_o}^2 - \alpha^2)}\, t$$

Natural Response



|ΔV| = 43mVpk

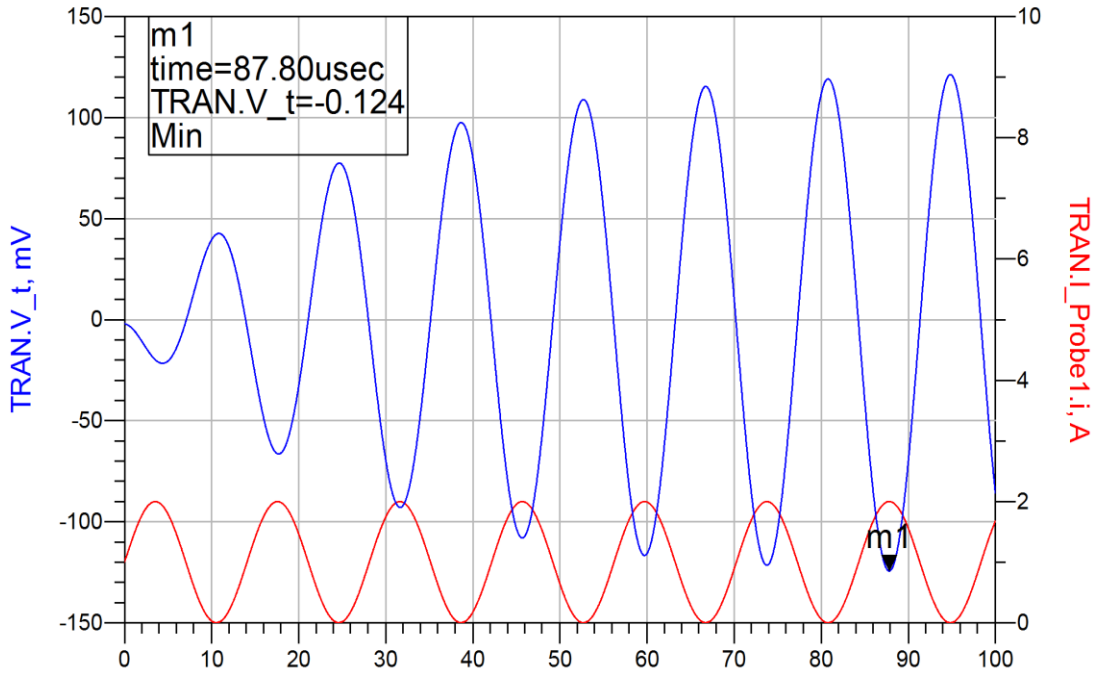
RESONANT SINE

Exponential growth

$$V(s) = \Delta I \cdot Q \cdot \sqrt{\frac{L}{C}} \cdot \left[\sin(\omega_o) \cdot t - e^{-\frac{\omega_o}{2Q}t} \cdot \sin\left(\sqrt{{\omega_o}^2 - \frac{{\omega_o}^2}{2Q}} \right) t \right]$$

Note: Q is now in the numerator

Forced Response



|ΔV|=124mVpk

Sine current ΔI=2Amps

RESONANT SQUARE

27% larger than sine excitation

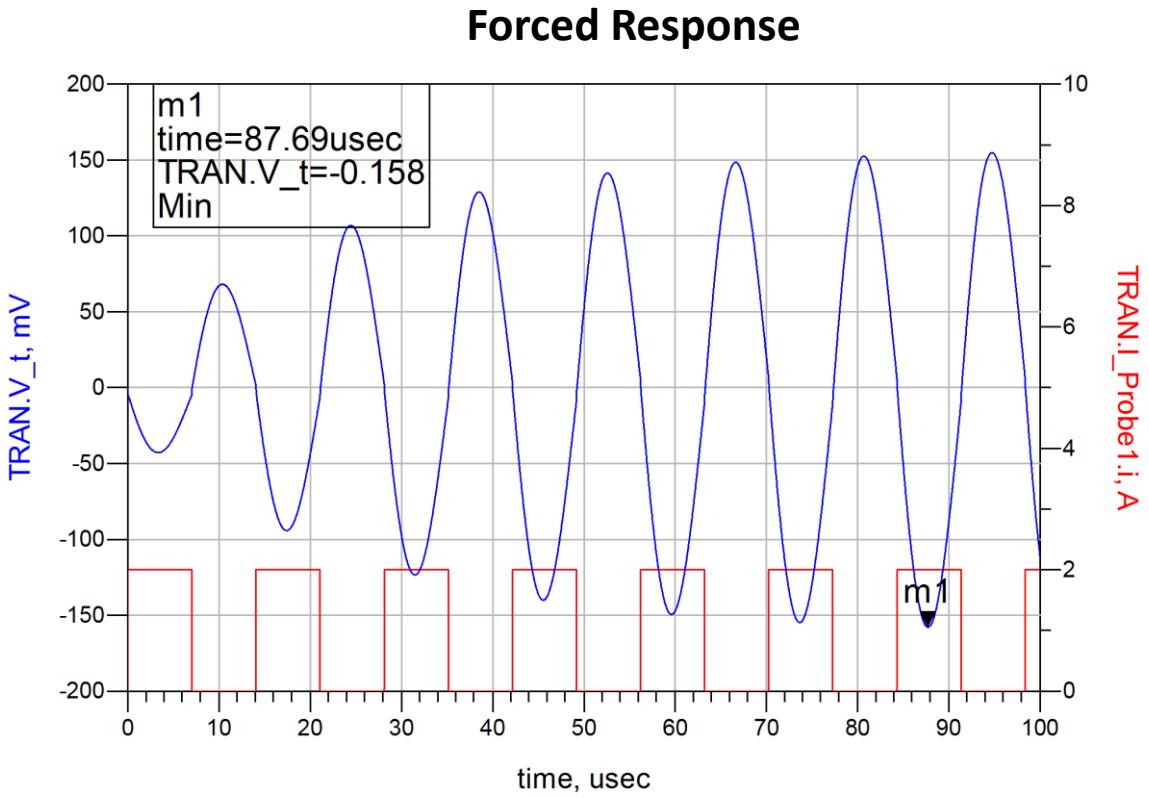
The Fourier transform of a square wave at any harmonic, n

$$\frac{2}{T}\left[\int_0^{n\pi} A\cdot sin(nt)\,dt + \int_{n\pi}^{2n\pi} A\cdot sin(nt)\,dt\right] = \frac{4}{n\pi} = \frac{1.273}{n}$$

$$\frac{4\cdot 124mV}{\pi} = 158\text{mVpk}$$

$|\Delta V|$=158mVpk

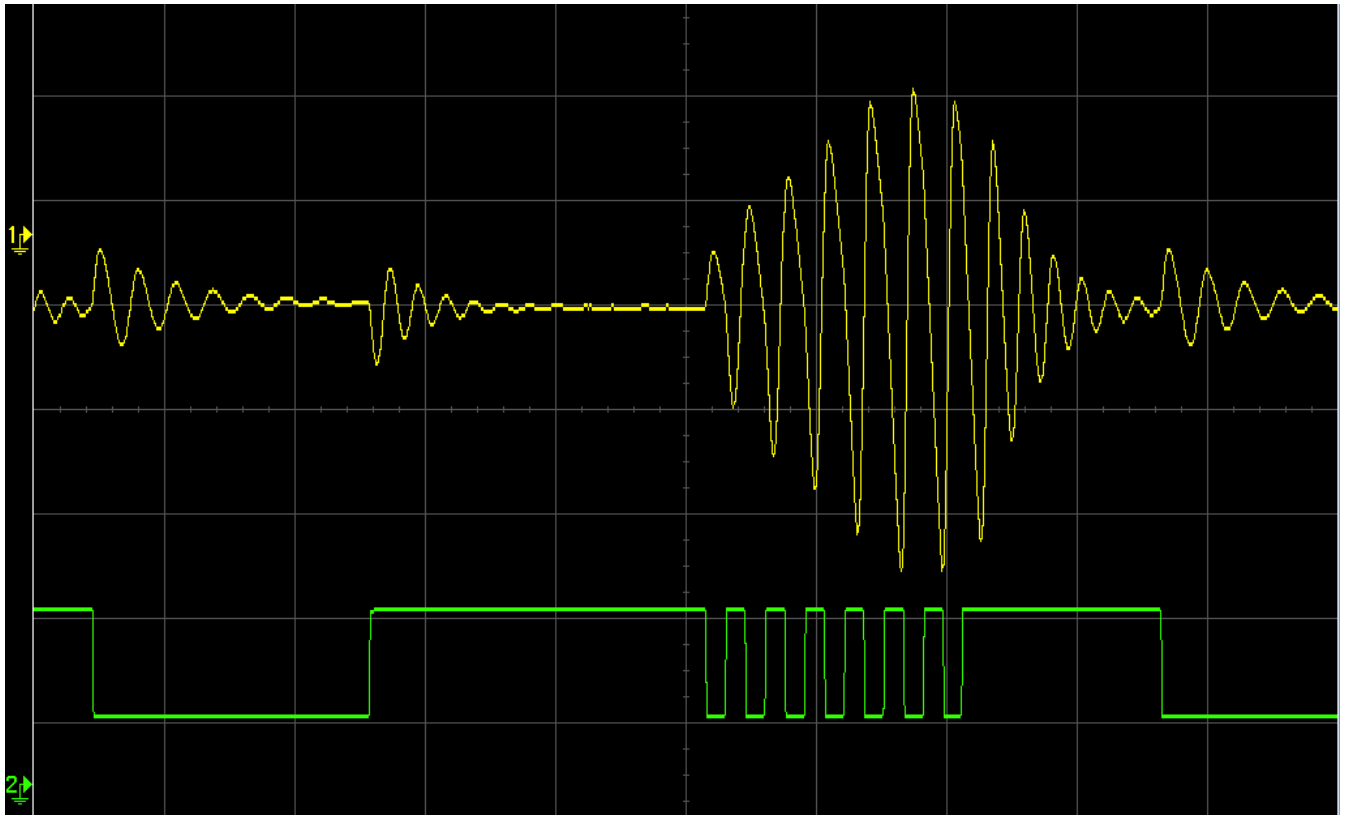
Square current ΔI=2Amps



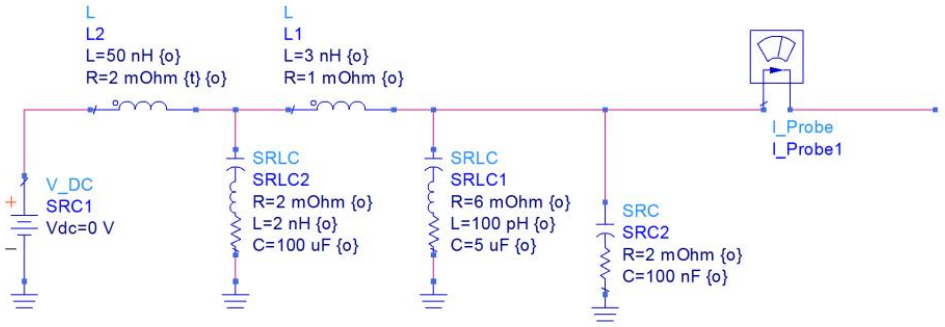
The Two response

This oscilloscope screenshot shows both the natural (step) response and the forced (resonant square wave) response at the same time.

The exponential decay, exponential growth and impact of resonant Q are all clear here.



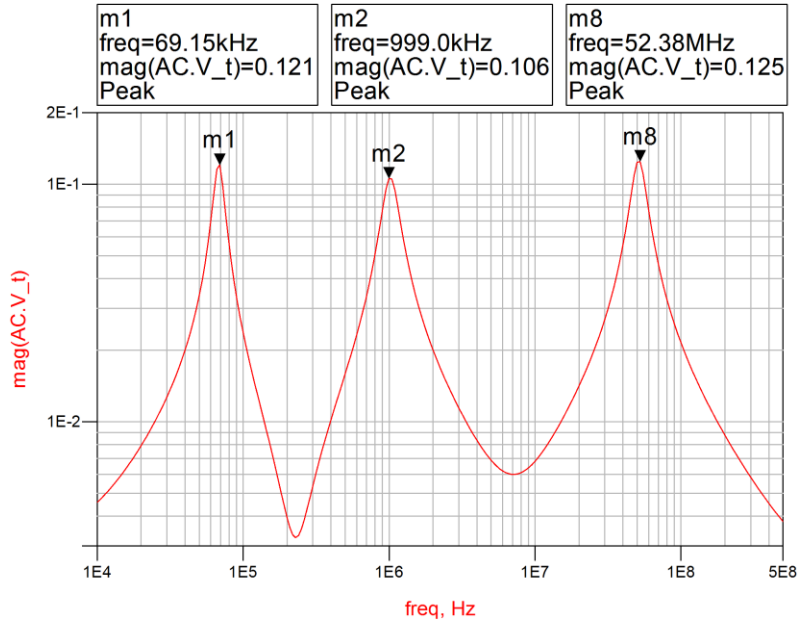
Multiple Resonances



Three resonances, each with a peak impedance of 125mΩ

What will the excursion be for a ΔI of 2A?

Most PDNs exhibit more than one resonant peak



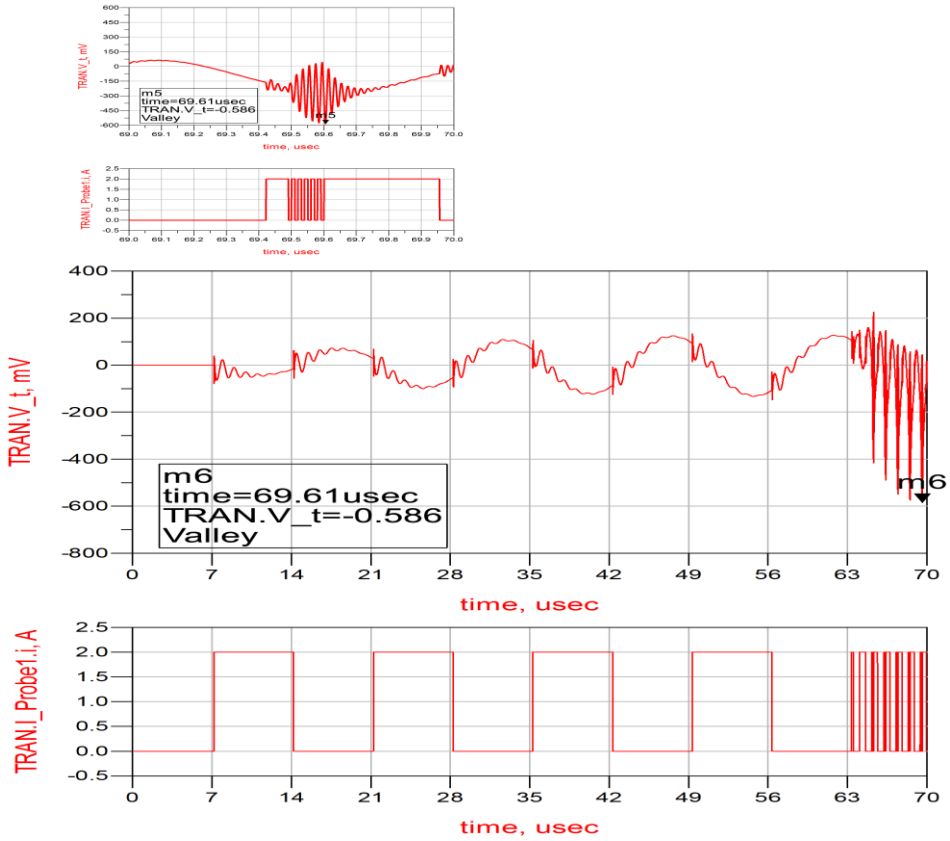
Rogue Waves

Creating a worst case current pattern results in a voltage response of 586mVpk.

The excursions were all excited and phased to sum – resulting in a Rogue wave.

This is more than 10X the response to a single 125mΩ peak step response.

$$\Delta V_{rogue} \approx \Delta I \sum_{0}^{n} Z_i)$$



Target Impedance

For a single Impedance peak

$$V_{pk-pk} = I_{pk-pk} \cdot \frac{4 \cdot Z_{pk}}{\pi}$$

Solving for an equivalent impedance

$$Z_{target} = \frac{V_{pk-pk}}{I_{pk-pk}} \cdot \frac{\pi}{4}$$

Target Impedance Bandwidth

$$Z_{BW} = \frac{0.35}{t_{edge}}$$

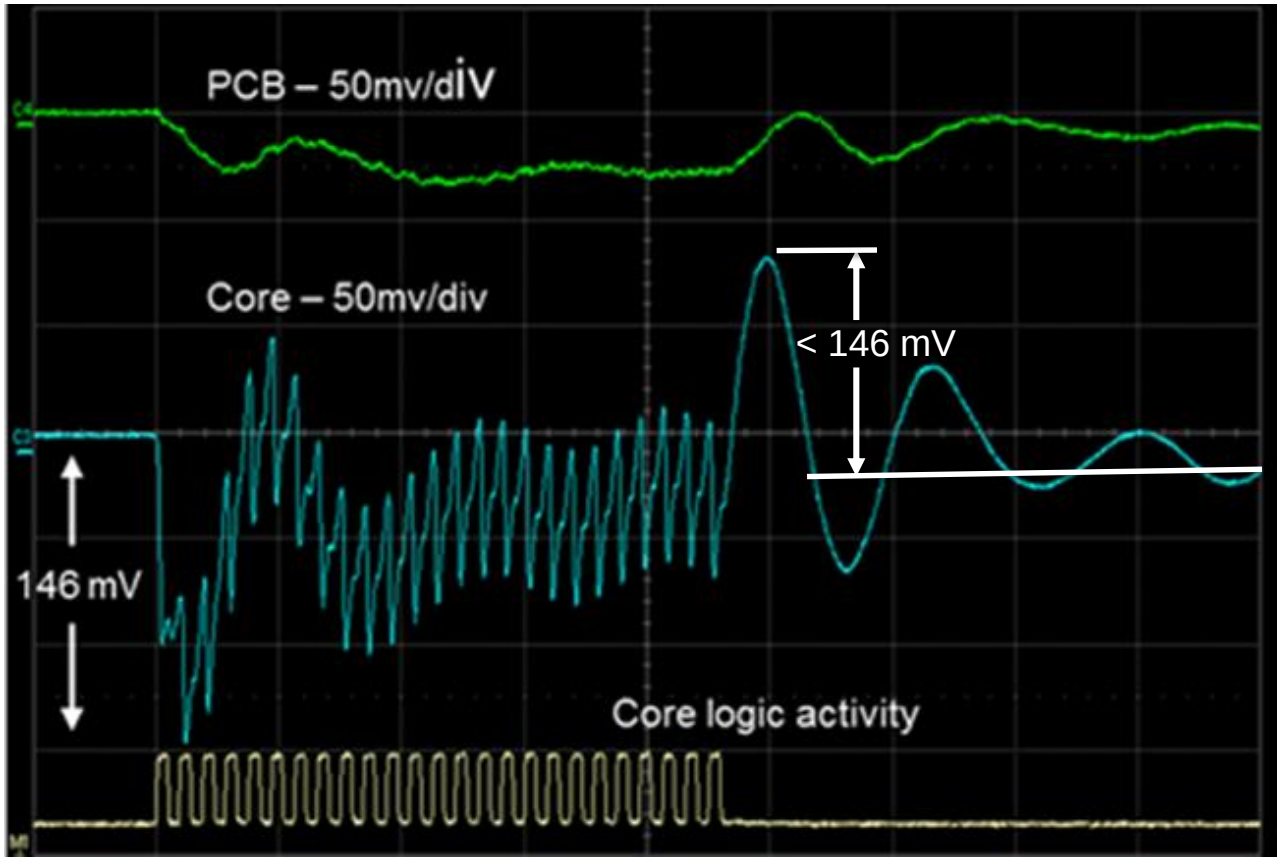
But beware of additional resonances and noise sources!

Dynamic Current is Complicated

When the core activity starts it appears as both a step and also as high frequency content

When the activity stops it appears as a step.

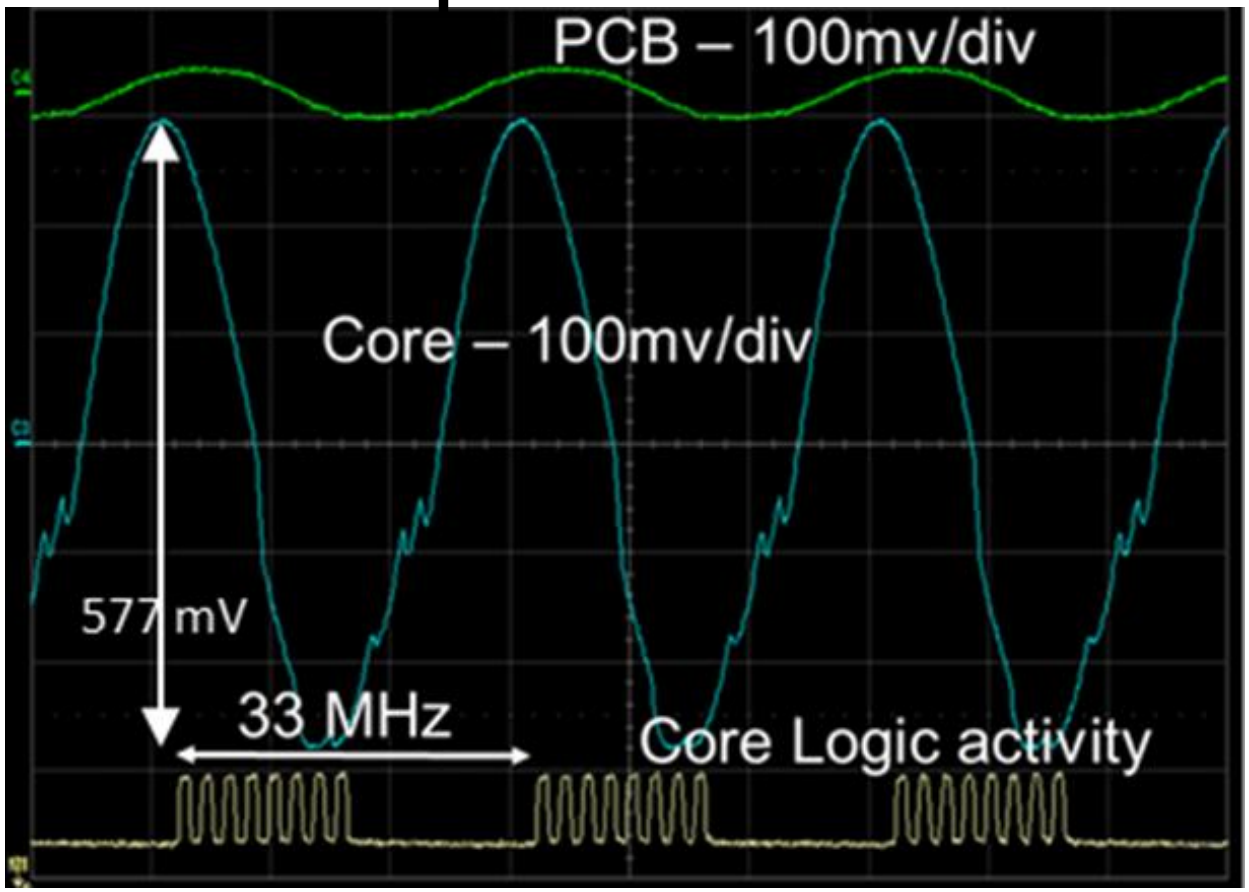
The exponential decay is clear and the response is asymmetric



Forced Response

When the core activity is at a repetition rate that matches the die resonant peak, we can see the much larger forced response.

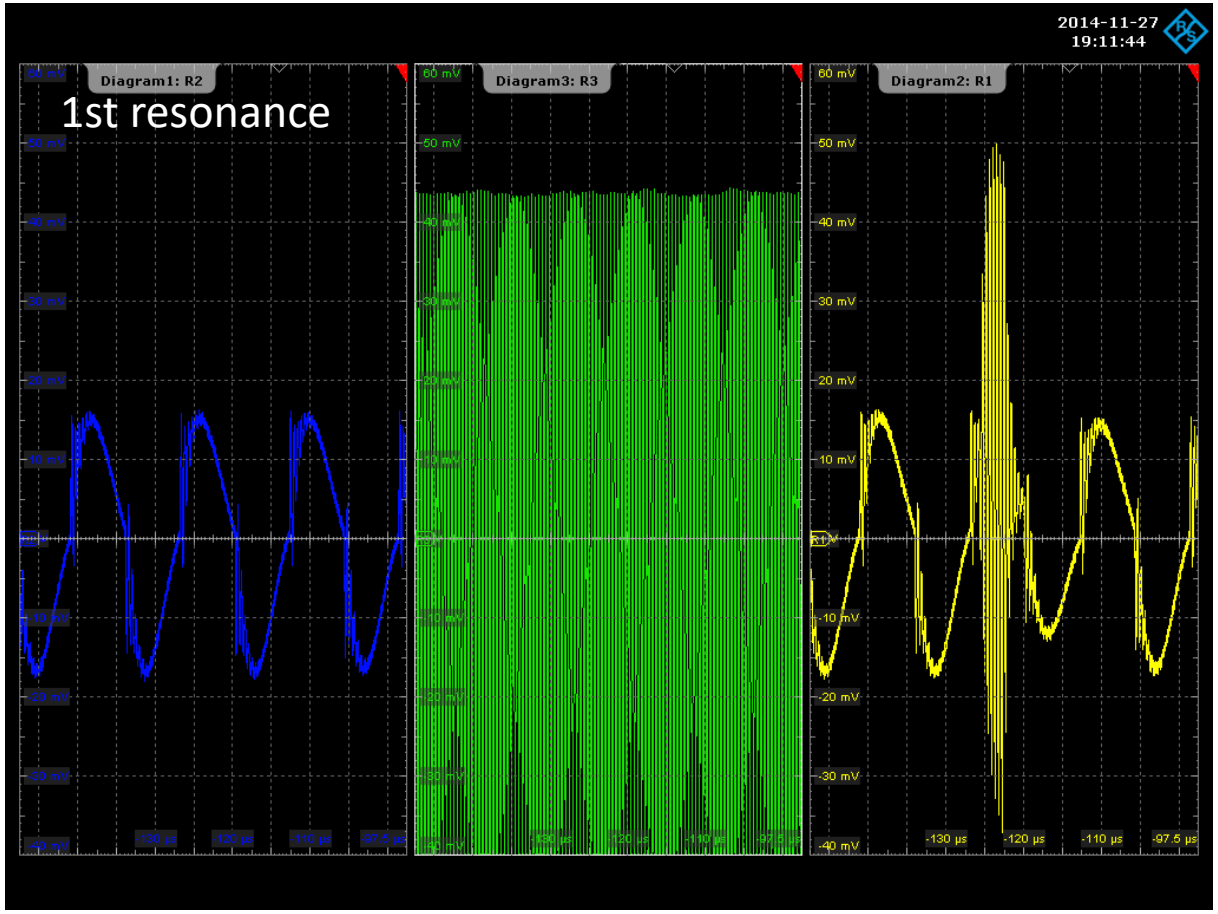
We can't see the exponential growth in this picture



Rogue Wave

Rogue waves may be rare, but do exist and are relatively simple to generate in the lab.

This oscilloscope screen shot shows a Rogue wave on the output of a DDR termination regulator.



Conclusions

1. Target impedance is a tool that helps design a robust PDN that results in acceptable noise
2. While flat impedance is ideal, careful management of the peaks can result in an acceptable design
3. Keep in mind that the VRM and system also generate noise that will appear at the die
4. Multiple sources are additive.

Thanks for Attending Our Session!

Maintain your Integrity - Power Responsibly

REFERENCES

1. Larry D. Smith, Eric Bogatin, “Principles of Power Integrity for PDN Design--Simplified: Robust and Cost Effective Design for High Speed Digital Products” (Prentice Hall Modern Semiconductor Design), ISBN-13: 978-0132735551, April 6, 2017
2. Sandler, S, “Power Integrity: Measuring, Optimizing, and Troubleshooting Power Related Parameters in Electronics Systems”, Nov 18, 2014
3. W. Cheng, A. Sarkar, S. Lin, and Z. Zheng, “Worst case switching pattern for core noise analysis,” DesignCon, 2009.
4. S. Sun, L. D. Smith, and P. Boyle, “On-chip PDN noise characterization and modeling,” DesignCon, 2010.
5. L. D. Smith, S. Sun, P. Boyle, and B. Krsnik, "System power distribution network theory and performance with various noise current stimuli including impacts on chip level timing,” in *Proc. Custom Integrated Circuits Conference*, San Jose, CA, 2009.
6. I. Novak, “Comparison of power distribution network design methods: Bypass capacitor selection based on time domain and frequency domain performances”. Manuscript for TF-MP3 “Comparison of Power Distribution Network Design Methods” at DesignCon 2006, February 6-9, 2006, Santa Clara, CA
7. C. K. Cheng “Power Distribution Network Simulation and Analysis” UCSD March, 4, 2010
8. Hu, Xiang, Peng Du, and Chung-Kuan Cheng. "Exploring the rogue wave phenomenon in 3D power distribution networks." Electrical Performance of Electronic Packaging and Systems (EPEPS), 2010 IEEE 19th Conference on. IEEE, 2010.