Signal Integrity Analysis on High-Density Silicon Interposer Package Technology for Next Generation Applications

Surender Singh and Taranjit Kukal
Cadence Design Systems, Inc. surender@cadence.com

Abstract

New semiconductor growth engines like high-performance computing (HPC) and artificial intelligence (AI) are forcing engineers to consider new advanced packaging techniques that integrate multiple integrated circuits (ICs) in a single device. In particular, 2.5D IC packaging, using a silicon interposer as a first-level of integration, offers a unique solution that provides localized high-density interconnects between two or more die, all while allowing much smaller physical interconnect geometries than traditional BGA substrates. In theory, this reduces chip-to-chip communication latency. This packaging technology has recently been targeted by these high-end computing systems that need high-memory bandwidth/low latency between the processor and memory. For these types of applications, the 2.5D IC/silicon interposer technology can provide better system performance and lower package profile, compared to the historical package-on-package (PoP) technology. However, the high data-rate and low supply voltage of these high-end computing sub-systems introduce new signal integrity (SI) and power integrity (PI) challenges.

This paper investigates the SI application of a fine-line, fine-pitch, large-size silicon interposer technology for integrating a processor and high-bandwidth memory (HBM). It starts by examining the package electrical modeling methodology used in GHz I/O device modeling in a more robust and accurate way to support high-volume manufacturing and high signal quality. This is followed by frequency and time domain analysis of package models to determine the optimized design parameters to achieve good signal performance. The contribution of each package parameter to the I/O performance is investigated using S-parameter and eye diagram techniques. The S-parameter technique is used for frequency-domain analysis while eye diagrams were used for time-domain analysis. Finally, the results seen on the silicon interposer technology are compared to traditional PoP technology.

Silicon Interposer Design Overview

To overcome the size limitation of the silicon interposer technology, and for better processor and memory integration, a new 2.5D SiP based on silicon interposer is developed as shown in Figure 1. Multiple die are integrated on a single interface layer (interposer), connected with high-density, thin interconnect [1]. The Cadence® SiP Layout tool was used design the silicon interposer. This high density of signals, coupled with silicon interposer design, requires careful design and thorough timing analysis.

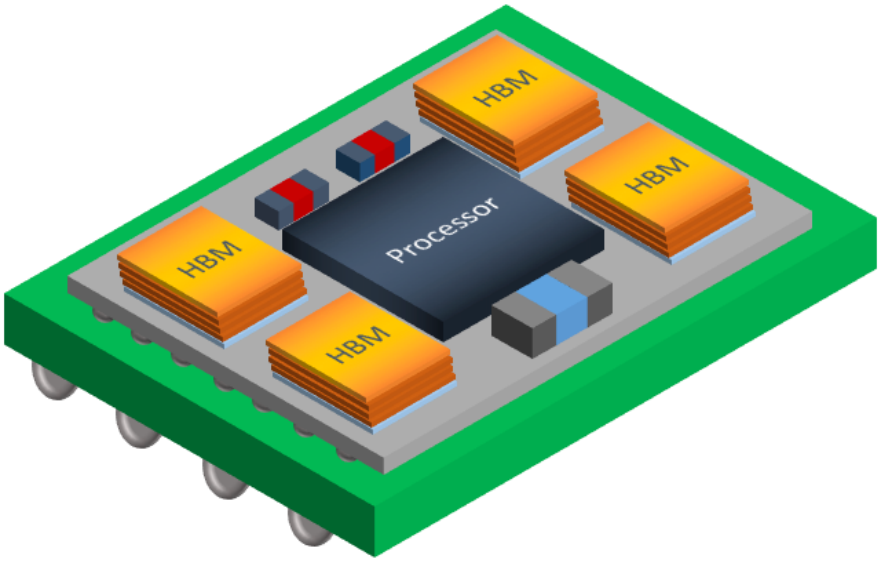

Figure1. System-level integration based on 2.5D IC/silicon interposer technology

Trace width and length are a major challenge for high-end memory-intensive applications necessitating high-speed data transmission between the processor and the large capacity memory units [2]. HBM achieves higher bandwidth while using less power in a substantially smaller form factor. Silicon interposer technology is best suited for applications where peak bandwidth, bandwidth per watt, and capacity per area are valued metrics, for applications such as Graphics Processor Units (GPUs), high-performance computing, server, networking, and client applications [3].

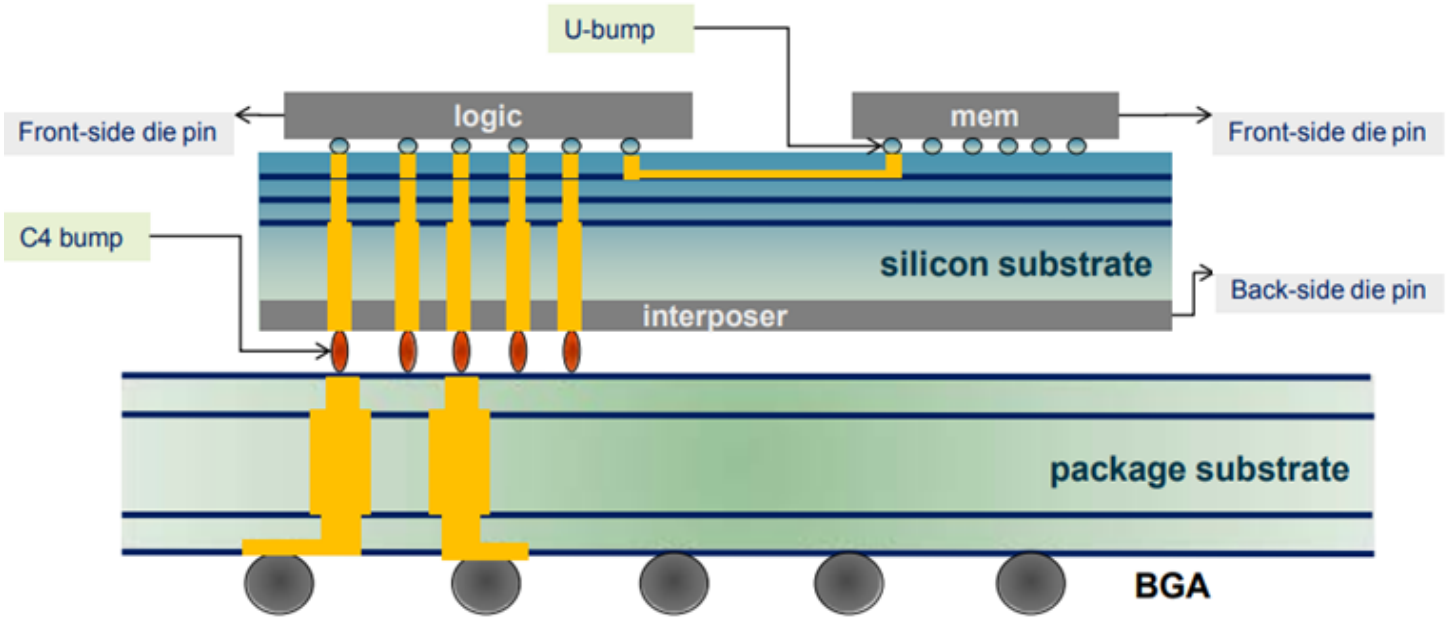

Figure 2. A side view of silicon interposer technology

Figure 2 shows the side view of Si interposer design: two die are placed side by side and connected through metal layer routing. The silicon interposer serves as an intermediate layer to establish die-to-die connections with higher density bumps. Other connections are passed through the interposer directly to the IC package substrate. For good SI performance, the system packages must perform with low-transmission loss and short-signal path to achieve the required electrical specifications. Interposer-level integration results in new electrical challenges due to the high-density interconnect routing [4]. The reduction of total power requires operation at the lowest possible voltage at the highest reliable frequency. This results in a need for decoupling inductance with capacitors located at the transistors to maintain voltage, independent of the operation being performed, and reduce ground resistance [5]. New challenges are posed as multiple requirements have to be balanced for one package, such as voltages are reduced, transistor count is increased, and analog and mixed-signal design.

Design Methodology "Silicon Interposer Technology"

Figure 3 shows a schematic cross-sectional image of a silicon interposer with logic and memory die. Two die were assembled side by side and fine copper traces were used for die-to-die connections. In the test-vehicle design, three metal layers were used for routing.

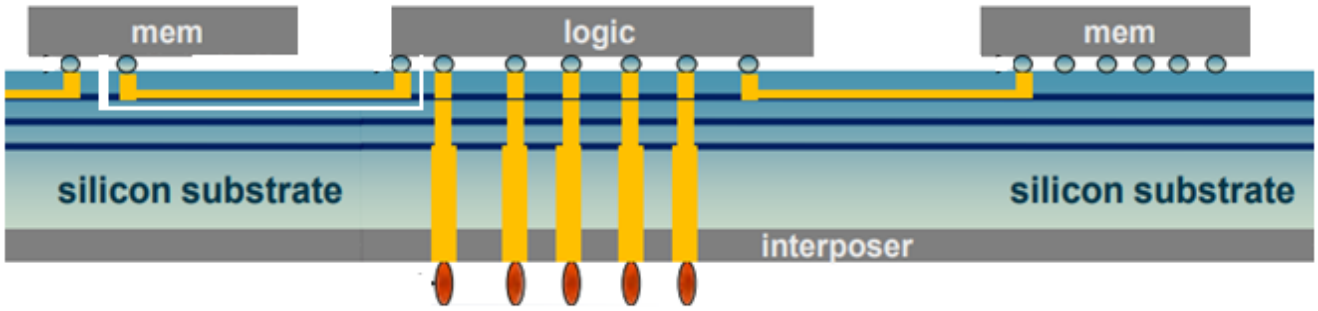

Figure 3. A schematic cross-sectional image of the silicon interposer

The entire memory system is integrated into the package using the silicon interposer as shown in Figure 4. The interposer has a size of 30mm × 25mm. A high-performance processor die measured 20mm × 24mm is attached on top of the interposer. The fully integrated memory system includes four stacks of HBM memory at 512GB/s bandwidth. Both the processor and HBM attach to the interposer using micro-bumps. The interposer is mounted on the substrate via traditional flip-chip bumps. The processor has 189,000 micro-bumps and the interposer has more than 34,000 flip-chip bumps. Four die were placed side by side with a 2.5-mm gap. Die-to-die connections were achieved with 2µm line widths. For improved performance of the layout, the processor die is split into six die with equal number of bumps, D1 to D6, as shown in Figure 4.

Design specification and overview:

- ASIC Die: Split into 6 die (each die of 28k bumps)
- No of HBM: 4 die
- Each HBM: 5 K bumps (total 20 K bumps)

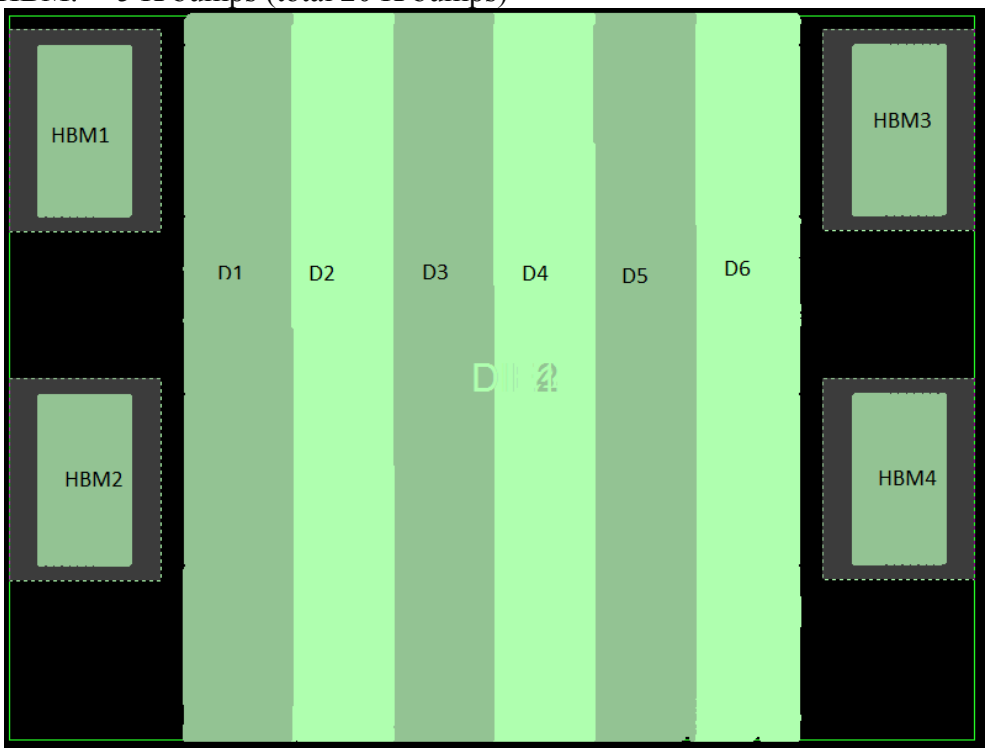

Figure 4. Silicon interposer with HBM and processor die

The reduced size of die and package dimensions and the incorporation of diverse substrate materials increases the challenges of controlling crosstalk between circuit elements [6]. For example, long signal traces that are closely spaced in a design may experience crosstalk due to the electric field interaction of data signals on adjacent traces. Over-constraining the layout with larger spacing rules or shielding requirements is not an ideal option as it can increase design size, leading to even more electrical challenges.

Copper, used for interposer-level interconnect, increases in resistivity in very small geometries due to increased edge and grain boundary scattering [7]. Inductance increases as the wire cross-section is decreased, and complex geometries are used. This increase in resistivity and inductance leads to an increase in latency for data signals and threaten power integrity.

Simulation and Results

To minimize the crosstalk on the interposer, a guard band was used between all traces as shown in Figure 5. Three metal layers were used for routing purposes. One metal layer was used for fan-out of both the die, HBM and processor, and two other layers were used for other routing purposes.

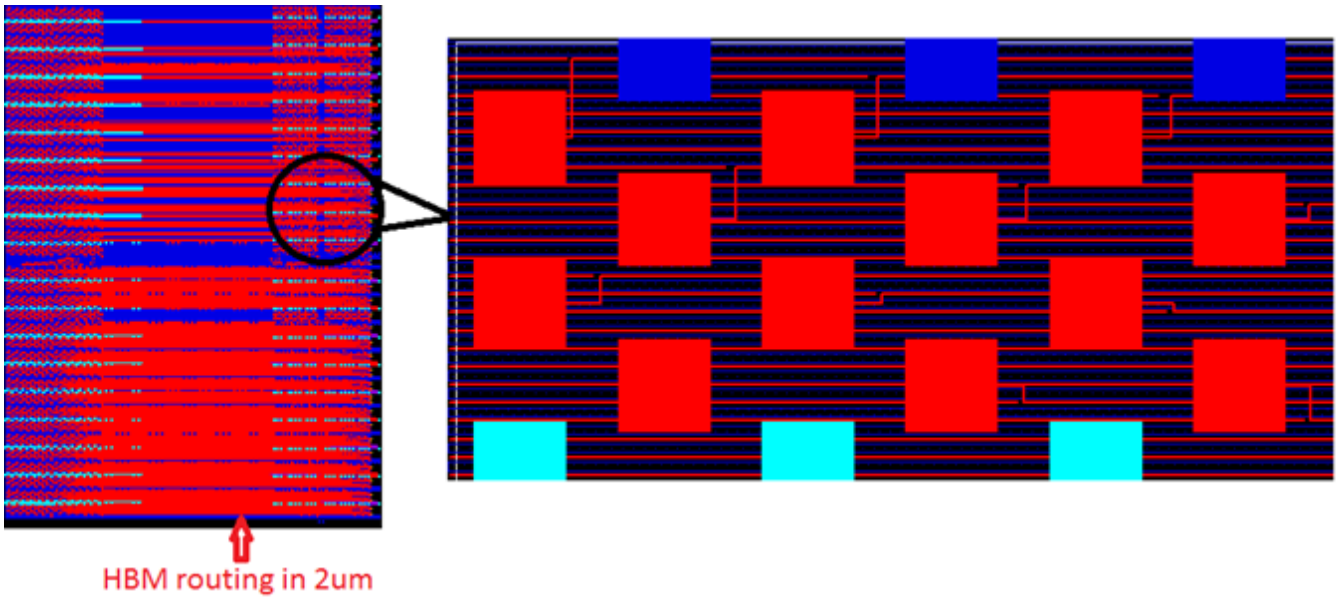

Figure 5. Silicon interposer routing between HBM and processor die

Time-domain and frequency-domain simulations have been performed to validate the 2.5D design and to check whether the performance specification of the HBM channels are met and to compare with traditional PoP design, where two BGA packages are combined vertically. The interconnect geometries used in PoP design are very different from the interconnect geometries used in silicon interposer technology.

The Cadence Sigrity™ PowerSI® 3D EM Extraction tool was used to perform the frequency-domain analysis based on S-parameter model extraction. Figure 6 (a) shows the return and insertion losses. Return and insertion losses are significant. Figure 6 (a) shows the return loss is less than –22dB, up to the fundamental for the 2800MT/s data transfer in silicon interposer design. Figure 6 (b) shows return and insertion for PoP design. An insertion loss of –1dB better at the fundamental of the 2800MT/s transfer rate in the interposer design.

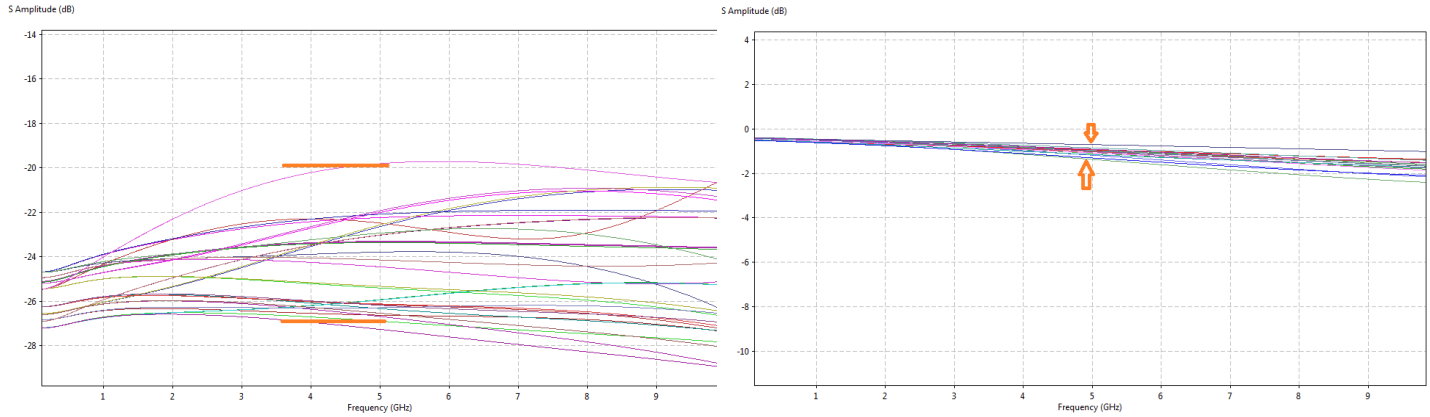

Figure 6 (a): The return loss and insertion loss in the 2.5D IC/silicon interposer design

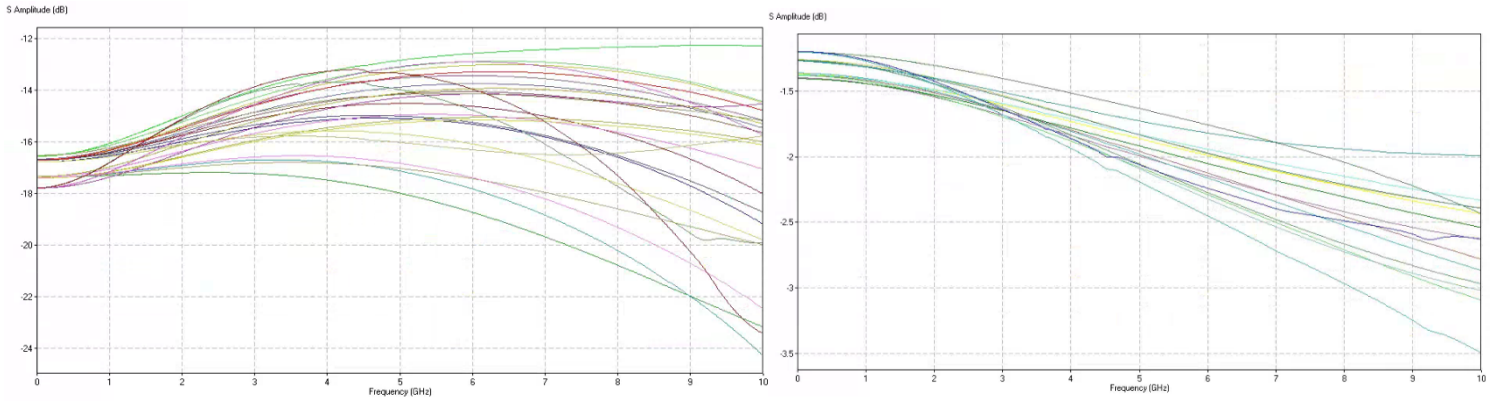

Figure 6 (b): The return loss and insertion loss in the PoP design

The silicon interposer results show better return and insertion loss performance than the traditional PoP technology. The return loss is improved by -8dB and inversion loss is improved by -1dB. Crosstalk is minimized in the interposer by using ground guard band between interconnect as demonstrated in this paper.

After the S-parameter model extraction, a testbench was setup in the Sigrity SystemSI™ tool for simulating the design, as shown in Figure 7.

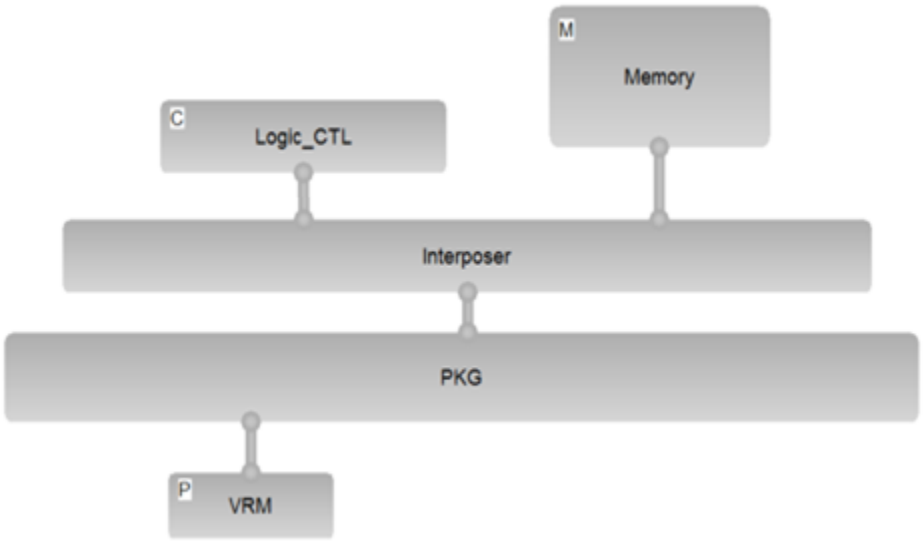

Figure 7: Simulation test bench setup for silicon interposer design.

For high-speed SI analysis, a S-parameter model is extracted at a wide frequency range of up to 10GHz. In the simulation testbench, the interposer represents the S-parameter of the processor interconnects to the HBM. To accurately simulate the IO switching behavior, IBIS device models are assigned to the processor and HBM blocks. The VRM block is assigned as the power supply to both die. Similarly, a testbench was setup for the PoP package, as shown in Figure 8.

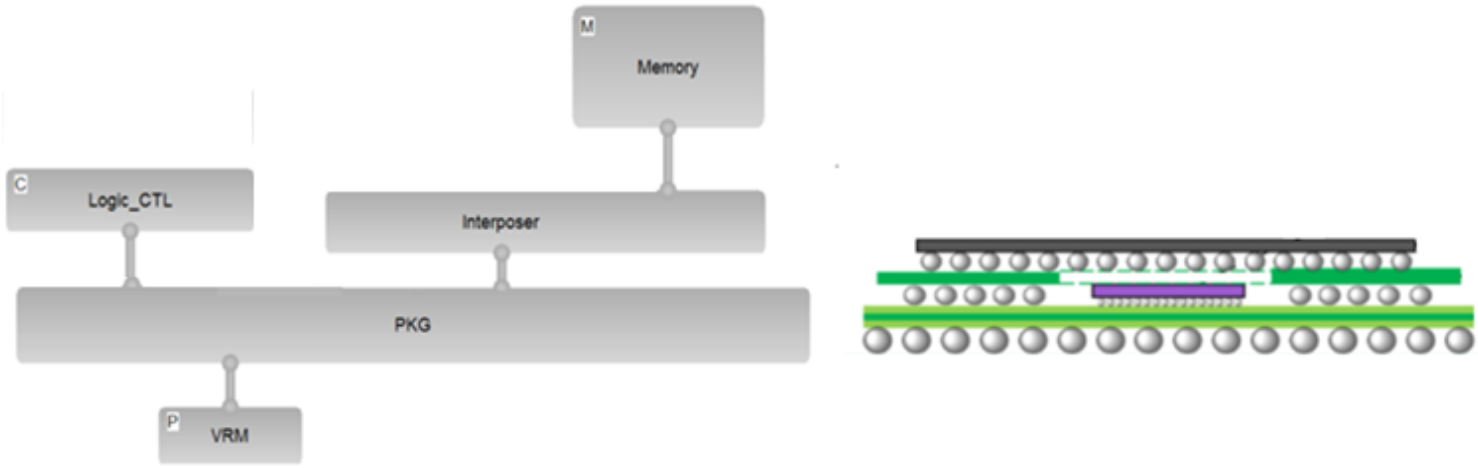

Figure 8: Simulation test bench setup for the PoP design.

For SI analysis, the S-parameter model was used by a time-domain simulator to check the eye diagram opening and jitter. For power integrity, the S-parameter can be reduced to check the input impedance profile in the frequency-domain.

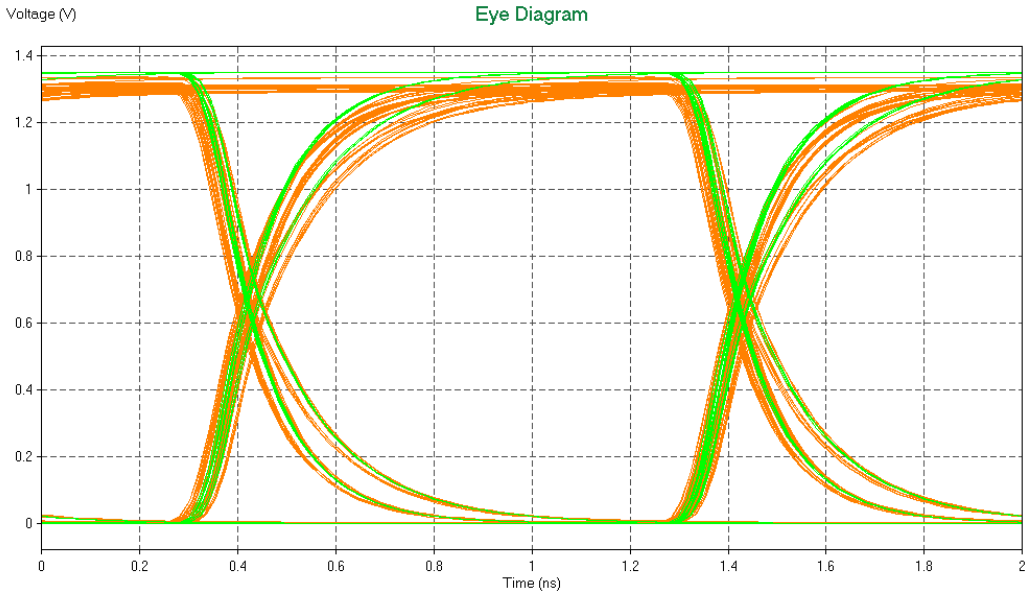

Figure 9 (a) Eye diagram for silicon interposer

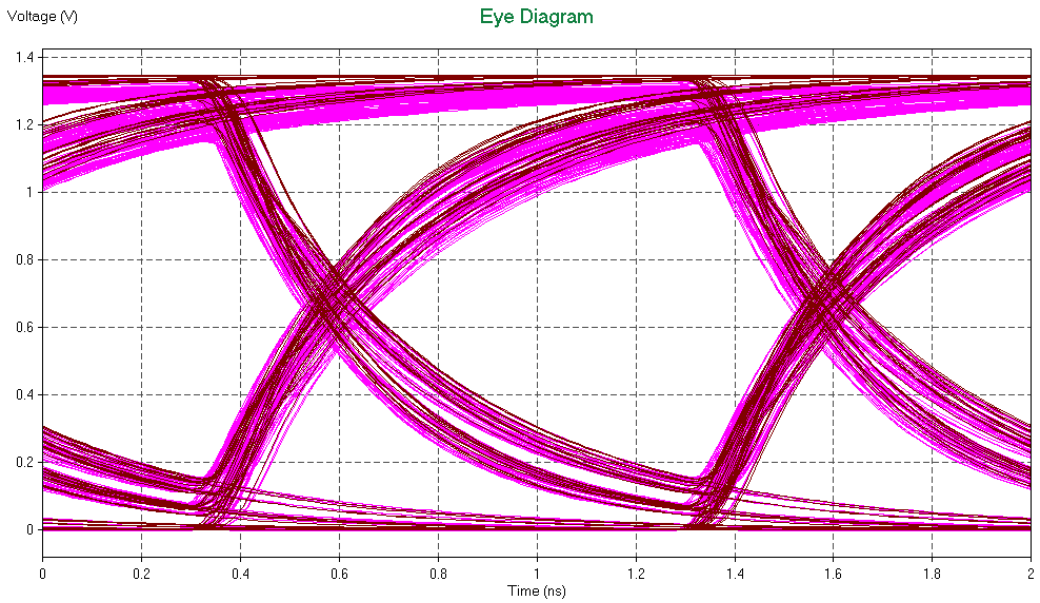

Figure 9 (b) Eye diagram for PoP

The eye height and the jitter are derived from the eye diagram, as shown in Figure 9 (a) for the interposer and, Figure 9 (b) for PoP design, respectively. The eye opening is better in silicon interposer design compared to PoP package. Jitter is also better in interposer design as compared to the PoP design. In the interposer design, interconnect length between HBM and processor die was smaller/shorter, compared to PoP design. This indicates that the SI performance is improved in silicon interposer technology.

Conclusions

In this paper, the 2.5D/silicon interposer packaging architecture was studied and compared against traditional PoP technology. Based on the smaller/shorter interconnect geometries that the silicon interposer supported, it's clear from this study, that 2.5D IC technology can provide significant electrical performance improvements over traditional PoP technology. The design included multiple flip-chip attached die to a silicon interposer, used as an intermediate layer to create high-performance die-to-die interconnect paths. This study confirms the use of silicon interposers, in a 2.5D IC configuration, as an excellent technology to achieve high-performance interconnect paths, reducing latency for die-to-die communication.

Reference:

1. W. S. Liao, *et al.*, "3D IC heterogeneous integration of GPS RF receiver, baseband, and DRAM on CoWoS with system BIST solution," in *Proc. Symposium on VLSI Circuits*, pp. C18-C19, Jun. 2013.
2. D. C.H. Yu, "New system-in-package (SiP) integration technologies," in *Proc. Custom Integrated Circuit Conference*, pp. 1-6, Sep. 2014.
3. D. Yu, "A new integration technology platform integrated fan-out wafer-level-packaging for mobile applications," in *Proc. Symposium on VLSI Technology*, pp. T46-T47, Jun. 2015.
4. M. Swaminathan and A. E. Engin, *Power Integrity Modeling and Design for Semiconductors and Systems*. Englewood Cliffs, NJ: Prentice-Hall, 2007.
5. Y. Kim, J. Cho, K. Kim, V. Sundaram, R. Tummala, J. Kim, "Signal and power integrity analysis in 2.5D integrated circuits (ICs) with glass, silicon and organic interposer," *Proc. IEEE 65th Electronic Components and Technology Conf. (ECTC)*, 2015, pp. 738–43.
6. A. Martwick and J. Drew, "Silicon interposer and TSV signaling," *IEEE 65th Electronic Components and Technology Conf. (ECTC)*, pp. 266–275, San Diego, CA, May 26–29, 2015.
7. Kei Murayama, Mitsuhiro Aizawa, Koji Hara, Masahiro, Mitsutoshi Higashi, " Warpage Control of Silicon Interposer for 2.5D Package Application", in *Proc. IEEE Electronic Components and Technol. Conf. (ECTC)*, Las vegas, Nevada, May 28–31, 2013, pp. 879–884.
8. *High-bandwidth Memory (HBM) DRAM*, JESD 235, Oct. 2013