Via Characterization and Modeling By Z-Input Impedance

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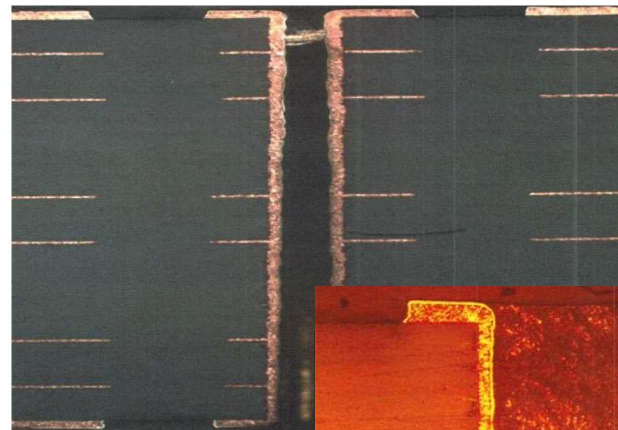
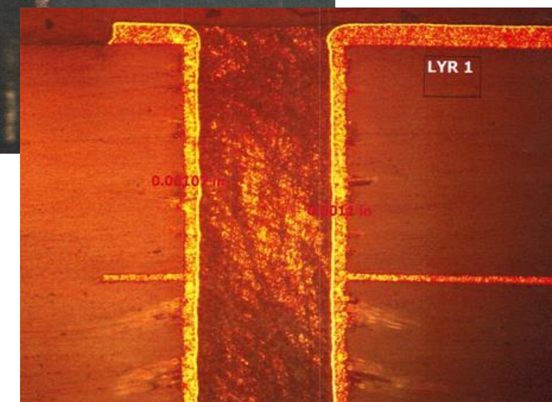
What is Via?
(Vertical Interconnect Access)

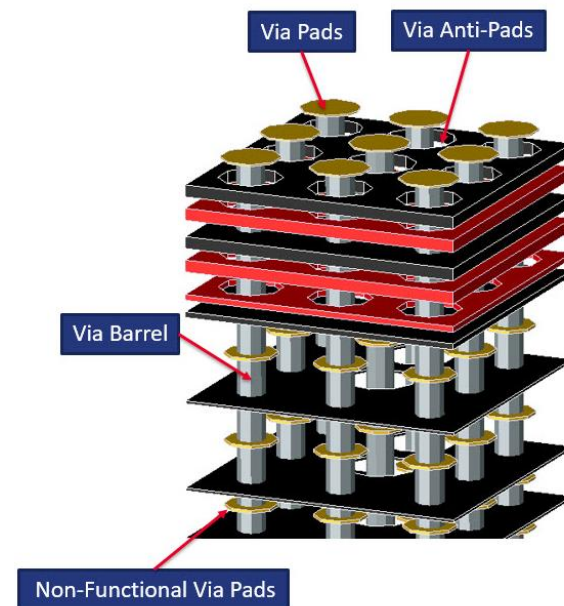
- An electrical connection between layers to propagate signals from one layer to the other
- Used only for multilayer PCB or package designs
- Produce discontinuity that affects signal and power integrity issues
- Via capacitance makes signal speed slower





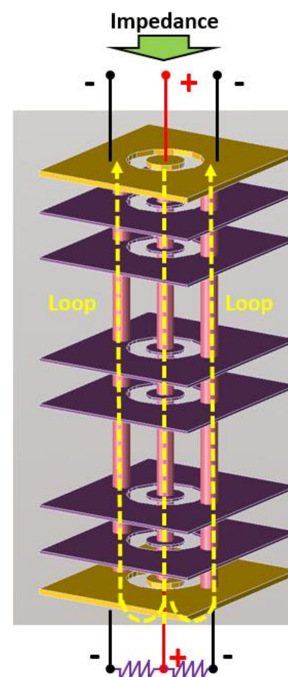
Anatomy of Via

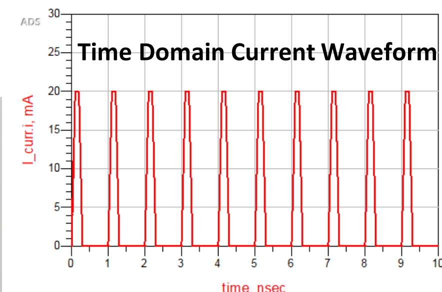
- Via Barrel
  - A through-hole that has been plated with a conductor
- Via Pads
  - Connect each end of the barrel to the components, planes, or traces
- Via Anti-pad or Clearance
  - Separate the via pad from other metal layers
- Non-Functional Via Pads (NFVP)
  - Internal or external pads that are not connected to any traces or components

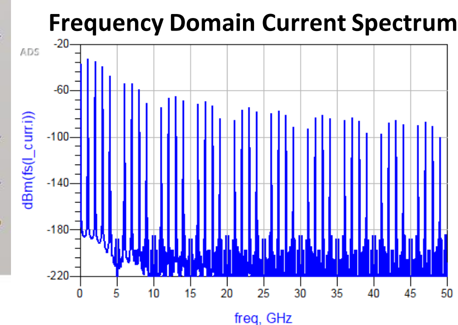


Via Impedance

- Impedance is typically the ratio of voltage divided by current between the two pins of component, physical layout, or commonly a network
- Via impedance is the impedance seen between the plus (+) and negative (-) pins from the source, and it is also the impedance of a network that makes a complete loop or circuit
- Ground return path must be a part of the via impedance calculation, otherwise the impedance value would be incorrect
- The return current flow favors the least impedance path and the return path for each frequency may have a different return path







Consideration in Using TDR

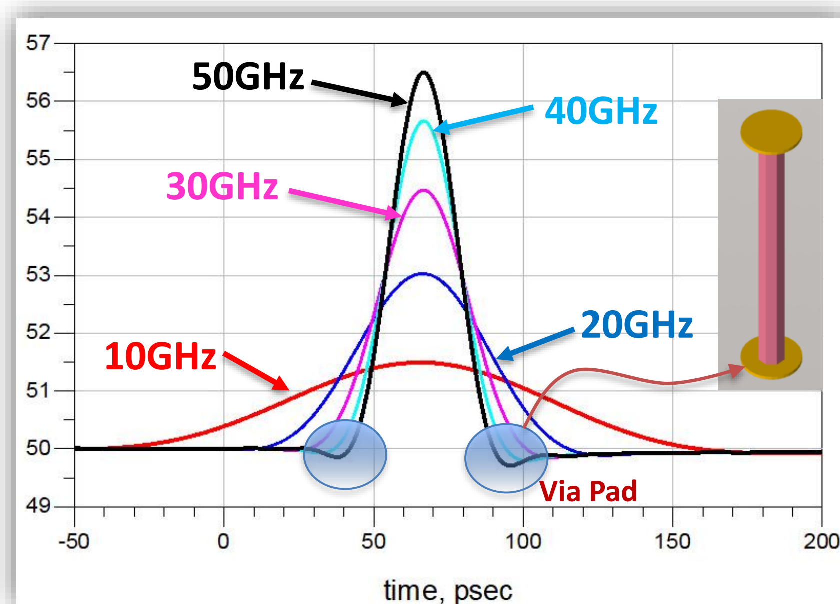
- Rise time of step signal – Minimum resolution
  - Ex: 10 ps → 30 mil minimum

$$L_{min} = \frac{T_R * C_0}{2 * \sqrt{\varepsilon_R}}$$

- Bandwidth limitation
  - Lower bandwidth data→ Can not resolve the via pad

$$BW = \frac{0.35}{TR}$$

- Impedance value read-out
  - 10GHz, 20GHz, 30GHz, 40GHz, and 50GHz bandwidth data → impedance keeps increasing

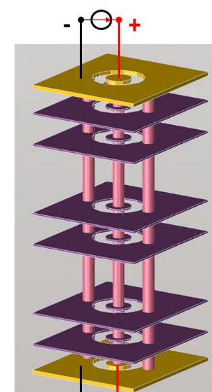


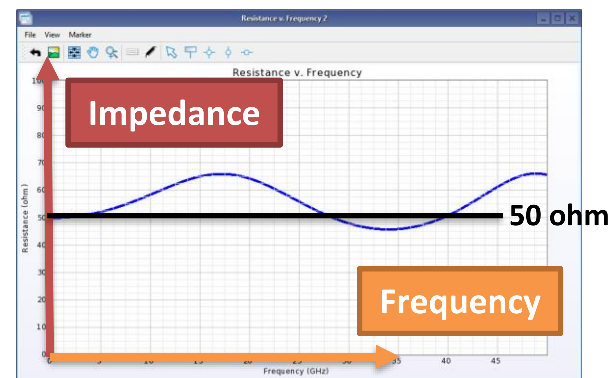
Z Input Impedance Approach

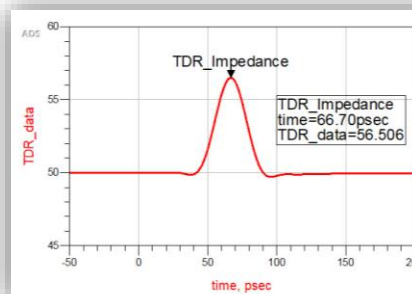
- Z-Input Impedance with the other port 50ohm terminated
  - No shorter risetime for step signal is required
  - No frequency to time conversion is required
- Frequency dependent impedance that is plotted around 50ohm
- Read out an accurate impedance value at every frequency
- TDR peak = 56ohm, Z-impedance = 46ohm ~ 66ohm, close to the average value

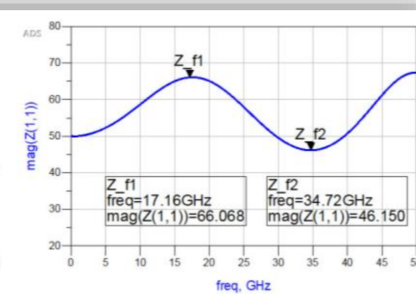
Z-Input Impedance

$$Zin = Zo\frac{1+S11}{1-S11}, Zin = 50\frac{1+S11}{1-S11}$$



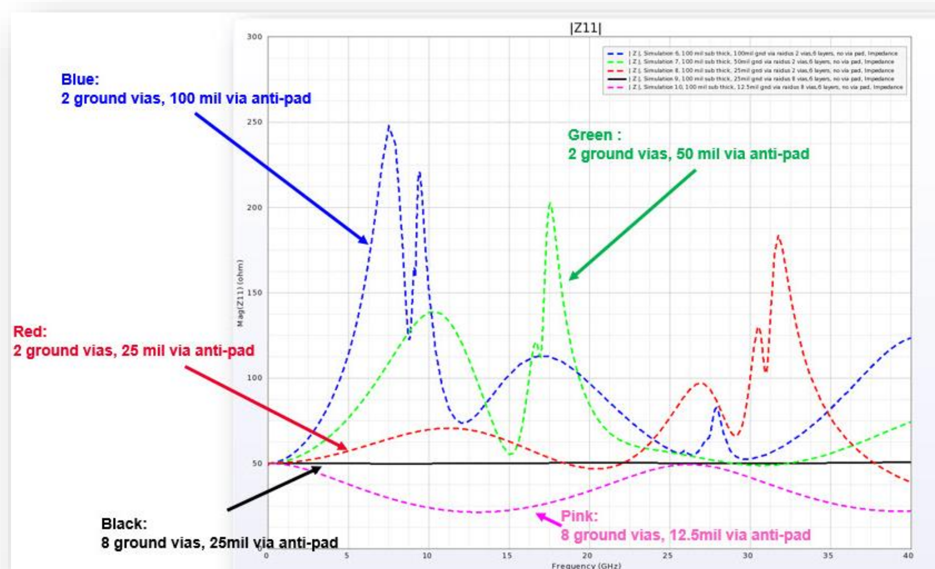






Typical Via Characteristic

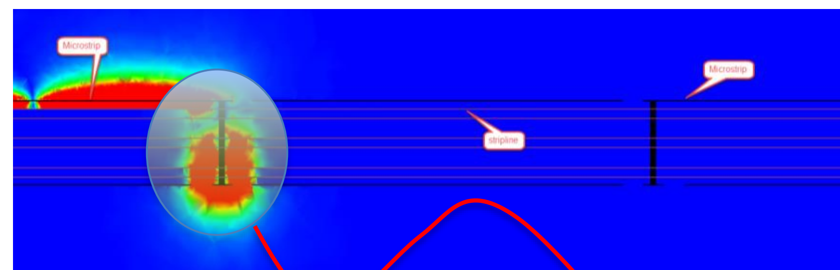
- Z-impedance Slope:
  - Positive Slope: Inductive
  - Negative Slope: Capacitive
- Typical characteristic
  - Via pad: Capacitive
    - The larger the size is the lower the slope is
  - Via anti-pad: Capacitive
    - The larger the size is the higher the slope is
  - Non-functional via pad: Capacitive
    - The more, the lower the slope is
  - Ground via
    - The more, the lower the slope is
    - The farther, the higher slope is

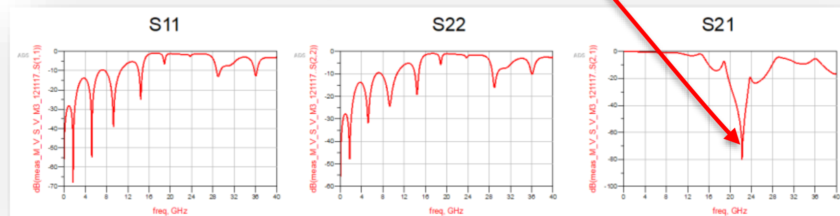


Via Stub Resonance

- Exist when signal routing goes from either microstrip to stripline or stripline to stripline without back-drilling
- Act as a series resonator or quarter wavelength open circuited stub
- Create a deep suck-out in the channel

Electric Field Trapped at the via stub



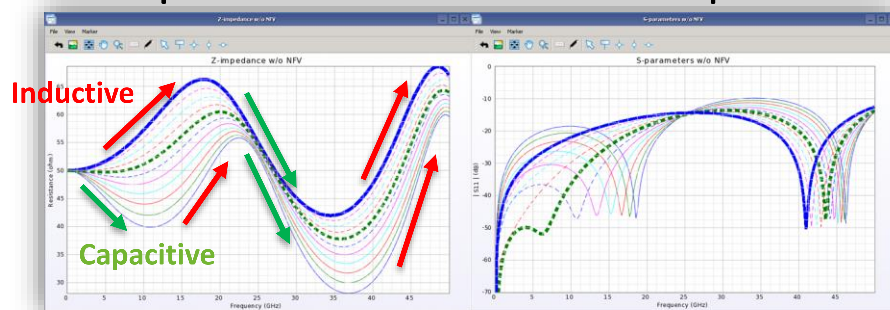


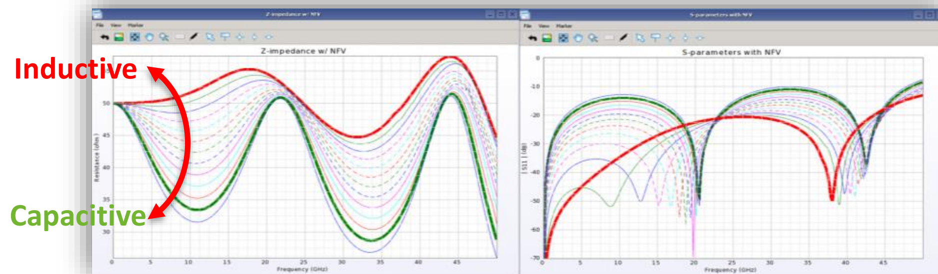
Measured S-Parameter Data

Z-Input Impedance vs. Antipad

- Only variable is the different size of anti-pad
  - For simplicity, other dimensions are fixed, for example, via barrel, via pads, ground via to anti-pad distance, 12mil diameter, 26mil diameter, and 3mil respectively
  - Fixed number of ground vias is 8
- Smaller anti-pad – Increased capacitance

Z input and S11 Without NFVP vs. Anti-pad size

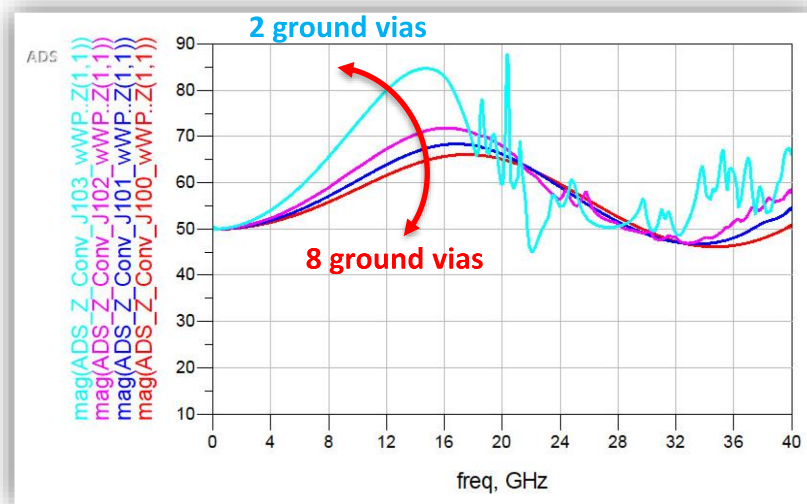




Z11 and S11 With NFVP vs. Anti-pad size

Effect on Number of Ground Vias

- Circular ground via ring can make the propagation mode to TEM
- The more ground vias, the better for the performance
- Fewer ground vias increase the inductance

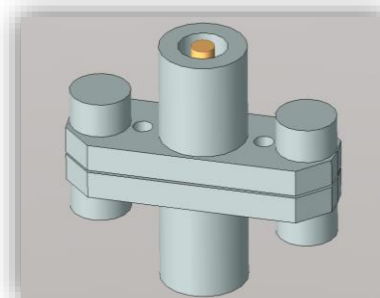


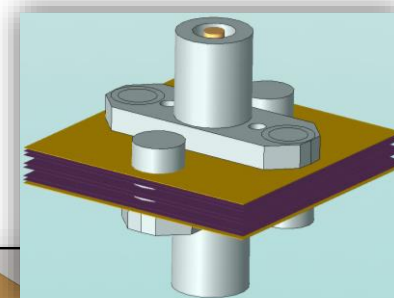
Circuit Model for Via

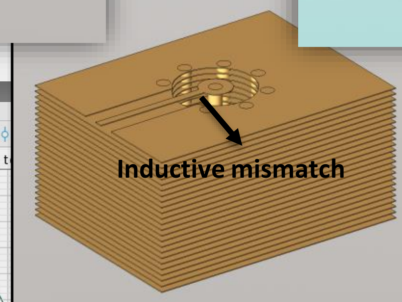
- Via Z-impedance is similar to that of low pass filter or coaxial transmission line
- The agreement between circuit model and EM model looks very good up to 20GHz and starts to deviate slightly due to the ideal model used in the circuit
- Extracted pad capacitance is 15.82fF and the modeled anti-pads is 33.5 mil compared to 23.4mil in 3D model
- This is due to the effective dimension for the ground is defined by the ground via ring not the size of anti-pads

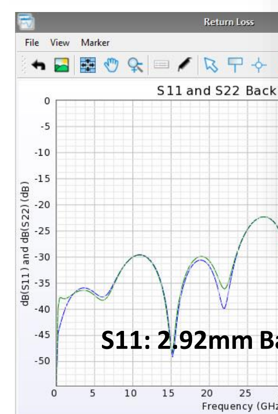
Thru Via Measurement with 2.92mm Connectors

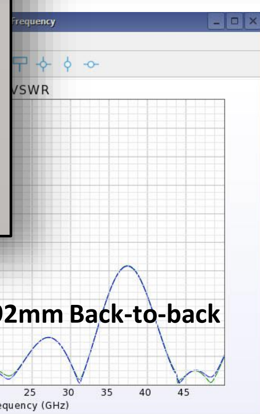
- Hard to perform via only characterization measurement without additional connecting transmission lines
- Transmission line to via adds an inductive mismatch
- Direct measurement of a via with 2.92mm connectors to the top and bottom of the via may minimize the mismatch for the via characterization (TEM propagation)
- Back-to-back 2.92mm connector performance looks very reasonable, less than -15dB return loss and 1.42 VSWR up to 50GHz







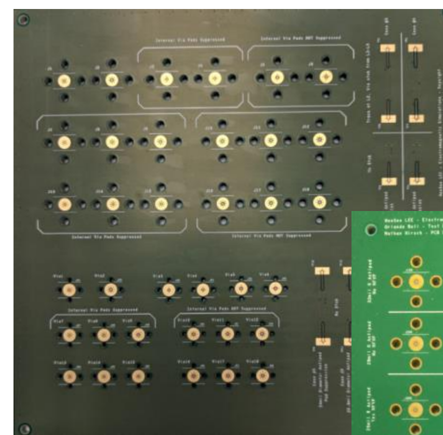




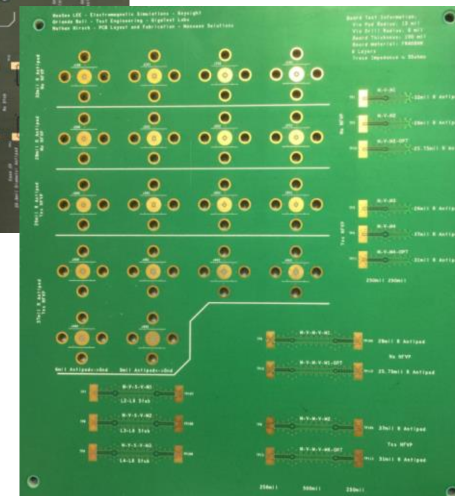
Test PCB Designs, Two Cases

- Designed two boards for measurements
- Isolated via structures
- Stripline/Microstrip via structures
- Structure variables:
  - Anti-pad
  - Via Pad
  - Non-Functional Vias Removed
  - # of Return-Path Vias

Board 1



Board 2



Common Board Specifications

- Dielectric: Isola FR408HR
  - Glass-weave/Resin dielectric
  - Chosen as a cost-effective, commonly used high-speed material
  - Dk range: 3.24 ~ 3.99*
- ½ Ounce copper
  - Outer layers have additional plating
- 12mil diameter barrels

Microstrip Cross-section

Via Cross-section

*Taken from Isola Datasheet, not measured from test board

Stack-up Design – Board 1

- Focus of first board:
  - Exaggerate length of via stub
  - Exaggerate over-all via length
- Nearly 1mil of difference in over-all thickness

	Table 1: Board 1			
	Material	Thickness (Planned)	Thickness (Actual)	Dk (@ 1GHz)
Layer 1	Copper Foil + Plating	1.40	2.20	
	FR408HR - 106(75)	5.00		3.26
	FR408HR - 2-2116	10.00	18.90	3.7
	FR408HR - 106(75)	4.94		3.26
Layer 2	Copper Foil	0.60	0.60	
	FR408HR - 7-1652	39.00	39.60	3.89
Layer 3	Copper Foil	0.60	0.60	
	FR408HR - 106(75)	4.94		3.26
	FR408HR - 2-1652	20.00	29.90	3.87
	FR408HR - 106(75)	4.94		3.26
Layer 4	Copper Foil	0.60	0.60	
	FR408HR - 7-1652	39.00	40.20	3.89
Layer 5	Copper Foil	0.60	0.60	
	FR408HR - 106(75)	4.94		3.26
	FR408HR - 2-2116	10.00	19.40	3.7
	FR408HR - 106(75)	5.00		3.26
Layer 6	Copper Foil + Plating	1.40	2.10	
	Total:	**152.96**	**154**	

Stack-up Design: Board 2

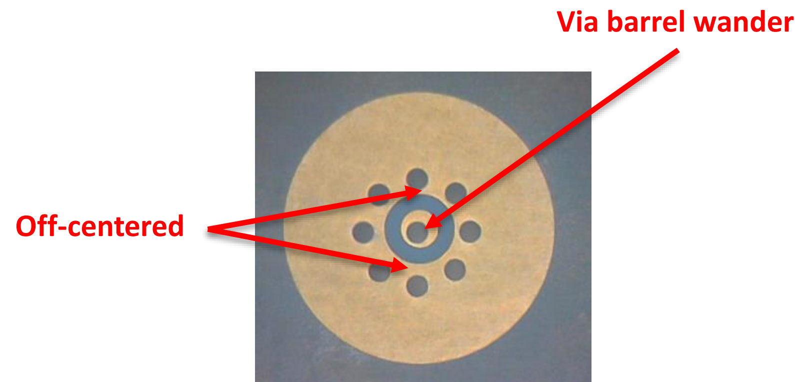
- Focus of second Board:
  - Make 50-ohm traces narrower
  - Make gaps between planes smaller
- Added two copper layers
- Shrunk dielectric thickness
- Nearly 4mil difference in board thickness

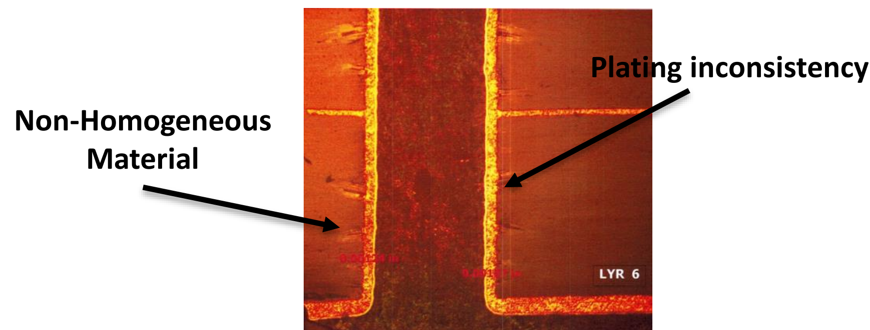
Table 2: Board 2

	Material	Thickness (Planned)	Thickness (Actual)	Dk (@ 1GHz)
Layer 1	Copper Foil + Plating	1.40	1.70	
	FR408HR - 2113(57)	8.28	7.40	3.62
Layer 2	Copper	0.60	0.60	
	FR408HR - 2-1652	10.00	10.00	3.99
Layer 3	Copper	0.60	0.60	
	FR408HR - 1080(65)	.30		3.46
	FR408HR - 2-1652	10.00	21.50	3.99
	FR408HR - 1080(65)	6.48		3.46
Layer 4	Copper	0.60	0.60	
	FR408HR - 2-1652	10.00	10.10	3.99
Layer 5	Copper	0.60	0.60	
	FR408HR - 1080(65)	6.30		3.46
	FR408HR - 2-1652	10.00	21.60	3.99
	FR408HR - 1080(65)	6.30		3.46
Layer 6	Copper	0.60	0.60	
	FR408HR - 2-1652	10.00	10.00	3.99
Layer 7	Copper	0.60	0.60	
	FR408HR - 2113(57)	8.28	7.40	3.62
Layer 8	Copper Foil + Plating	1.40	1.50	
	Total:	**98.34**	**94.80**	

Manufacturing Tolerances

- Material thickness
  - Prepreg will flow out of board during fabrication, leads to inconsistent thickness and via length mismatch
- Non-Homogeneous Material
  - Along via barrel, material density changes
- Via drill wander
  - Hole location tolerances on test board +/- 1mil, fabricator specific
- Plating inconsistencies
  - Barrel plating can vary

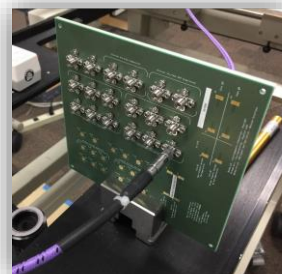




Measurement and Calibration

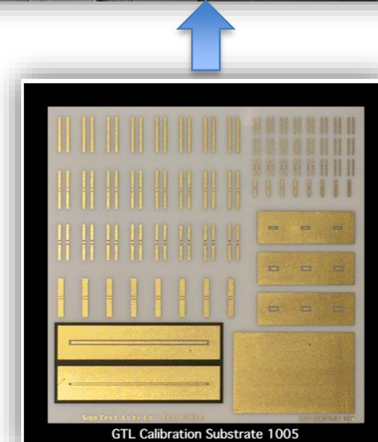
- Measurements conducted with coaxial connectors and probes
- Calibration is key for measurement accuracy
- Coaxial calibration: E-Cal module
- Probe calibration: Calibration Substrate
- Do not forget to verify the calibration

Coaxial Measurement



Probe Measurement

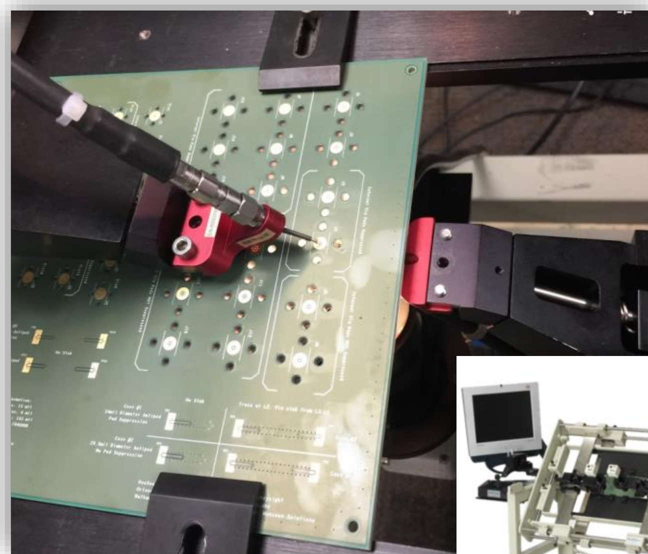
E-Cal Module



Calibration Substrate

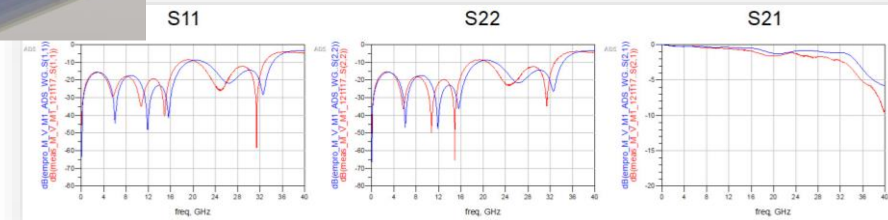
Probe Measurement for Thru Vias

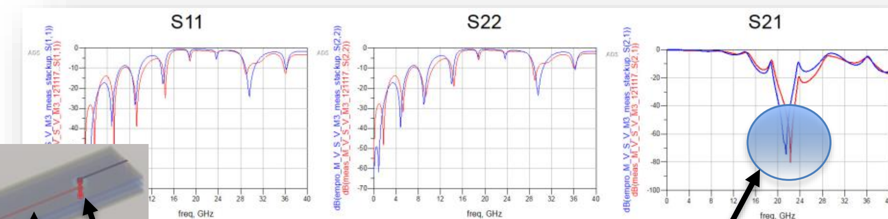
- Natural launch into via requires top-to-bottom side probing, with precise viewing of probe placement and platform stability
- Alternative probing side-to-side, in vertical plane, can easily result in poor probe placement and measurement errors
- GTL-5050 Rotating Probing Platform offers “simultaneous” top-to-bottom view of probes with precise probe placement and platform stability

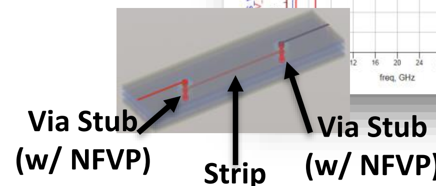


Validation Results

- Microstrip ⇔ Via ⇔ Microstrip Configuration
  - Compared for 0~40GHz
  - The agreement is very good, considering fabrication tolerances and material property imperfections
- Microstrip ⇔ Via (stub) ⇔ Strip ⇔ Via(stub) ⇔ Microstrip
  - Compared for 0~40GHz
  - Stub resonance is well matched
  - Very satisfactory agreement



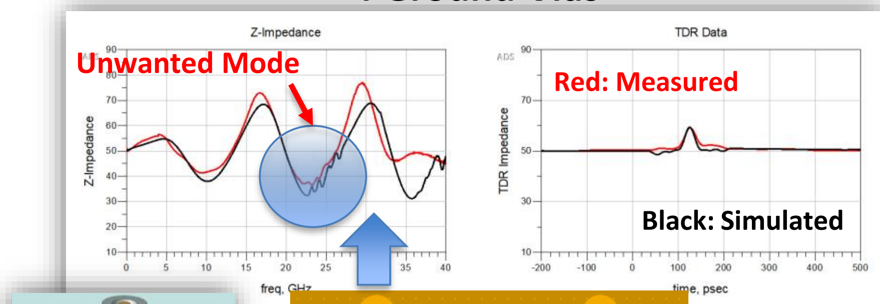


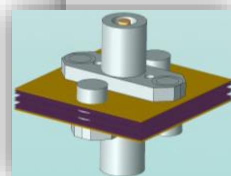


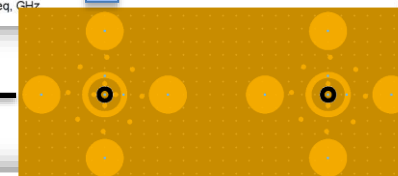
Validation Results

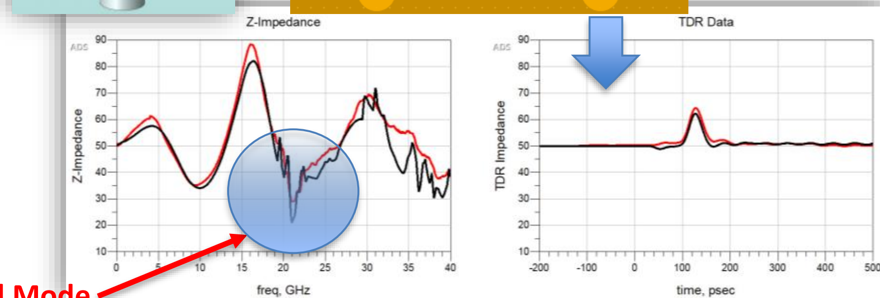
- 4 ground vias w/ NFVP
  - Z-impedance shows "inductive" at the lower frequencies as expected
  - Shows the frequency dependent Z-impedance and agrees well with the measurement
- 2 ground vias w/ NFVP
  - Z-impedance slope gets steeper, meaning more "inductive" in general, due to less number of return-path vias
- Noise data on Z-impedance plot reveals unwanted modes generated, which are not shown in TDR plot

4 Ground Vias







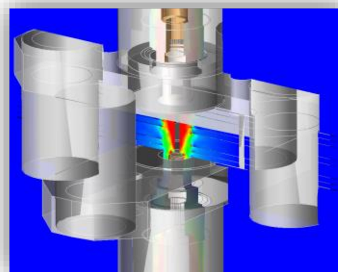


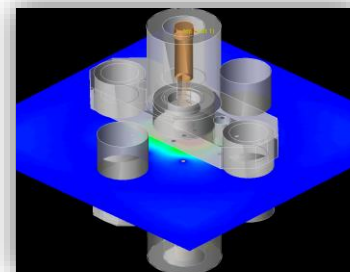
2 Ground Vias

Field Visualization of Unwanted Higher Modes

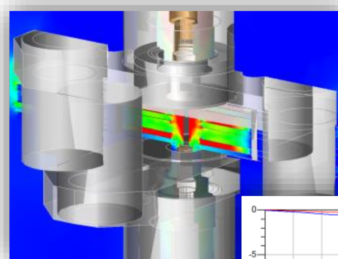
- Vertical and horizontal E-field data shown at 10GHz and 21GHz
- Electric energy at 10GHz is well contained so that there is no additional loss shown for the transmission characteristic
- Cavity or plane modes at 21GHz

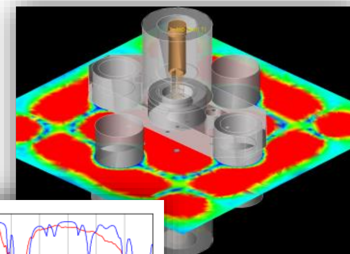
Vertical View | **Horizontal View**



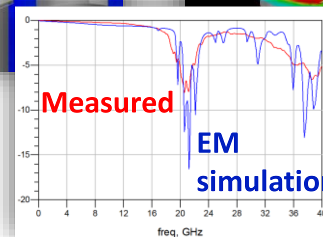


@ 10GHz





@ 21GHz



Conclusion

- With Z-input impedance approach, design engineers gain more insights for via designs including frequency dependent impedance characteristics and an accurate impedance value, which augments or overcomes the shortcomings of the traditional TDR method
- Our interest focused on single ended via structure with a high return-path via count, but this Z-input impedance concept can be easily expanded to differential structures, which is left for the future study
- It is more common in PCB design to use 1 or 2 return path vias instead of 8. This more common structure should be explored further and characterized so that impedance can be modeled and controlled