VRM Modeling: A Strategy to Survive the Collision of Three Worlds

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An Overall Perspective

In any electronic product, the Power Distribution Network (PDN) consists of three elements: the power generator often referred to as the Voltage Regulator Module (VRM), power consumers, which are the active devices, and a passive network of interconnects linking the two. The VRM is the essential power generation component. It converts some AC or DC input voltage into the DC voltages required by active devices. These active devices ultimately transform electrical energy into actions such as information processing, sensing, actuating, displaying, or communicating. The passive network of interconnects includes the board, packages, and decoupling capacitors.

In many design teams, different engineers, different groups, or even different companies are sometimes responsible for developing one of these three elements, often without sufficient knowledge of the other elements. Although each element may have a specification that defines its input and output performance, rarely does the specification alone contain enough detail to guarantee the correct, integrated performance of the entire network because the other elements can vary over a wide performance range.

The unfortunate product manager is ultimately responsible for ensuring the final product works when all three elements of the PDN are integrated together. How can the product manager be confident, before the product is built, that the VRM, interconnects, and active devices, which interact, meets the product performance specs, margin tests, and cost targets in all operating conditions?

One practical approach is to use some level of modeling for each element. This allows analysis of nominal and worst-case situations and, if necessary, exploration of alternative designs before final design decisions are made. An added benefit of this approach is that each design group can examine the models of the other elements and gain an understanding of how their element might interact with the rest of the system.

Selecting a model to use for each element requires establishing a dynamic balance between acceptable simulation accuracy and the costs in effort, expertise, time, risk, and dollars required to attain that accuracy.

Although more detailed and accurate models of each element may increase the accuracy of the simulations, higher accuracy comes at some cost. Generally, the more accurate the model, the more complex it is, the more expertise is required to use it correctly, the more time it might take to run through scenarios, and the more difficult it might be to debug the results and build confidence in their accuracy.

If the model is so complex that only a few experts can understand it and use it without introducing artifacts, the risk of generating inaccurate results is high when less-experienced engineers use the model. On the other hand, if the model is so simple that it does not include features that might affect performance dramatically, it would have little value.

The design process still relies on engineering intuition. Although the final design signoff can be based on a detailed system-level simulation, the initial creation and optimization of a design is often based on the judgement of an experienced engineer. An appropriately complex model that is still simple enough to grasp can be a powerful tool to guide initial design decisions.

A complete PDN contains many sources of noise. Some elements act as aggressors and some as victims. Ultimately, the product manager is responsible for identifying all sources of noise that have the potential to cause an error in any operating conditions.

In practice, only those with high levels of expertise can identify and minimize all possible self-aggression and mutual-aggression noise sources, so in most situations only the most common noise sources are analyzed. This approach results in some risk that a noise source not included in the analysis might cause a product failure.

This paper reviews four levels of VRM models that VRM designers, board level interconnect designers, semiconductor designers, and product managers often use to explore design tradeoffs throughout the PDN system. The choice of which one to use involves considering engineers' levels of expertise and what problems they expect to analyze. Some tradeoffs and relative merits of the models are described.

From the Core Logic's Perspective

To guide the investigation of the four models, we start with a worldview from the core logic circuit's perspective. Although this is only one perspective, it helps identify self-aggression noise caused by transient currents in the core logic circuits, as viewed by the silicon transistors that draw current from the PDN. Figure 1 shows a rough schematic of the rest of the PDN system as seen by the pads on the core logic rails on the die, and the small signal impedance profile looking into the PDN.

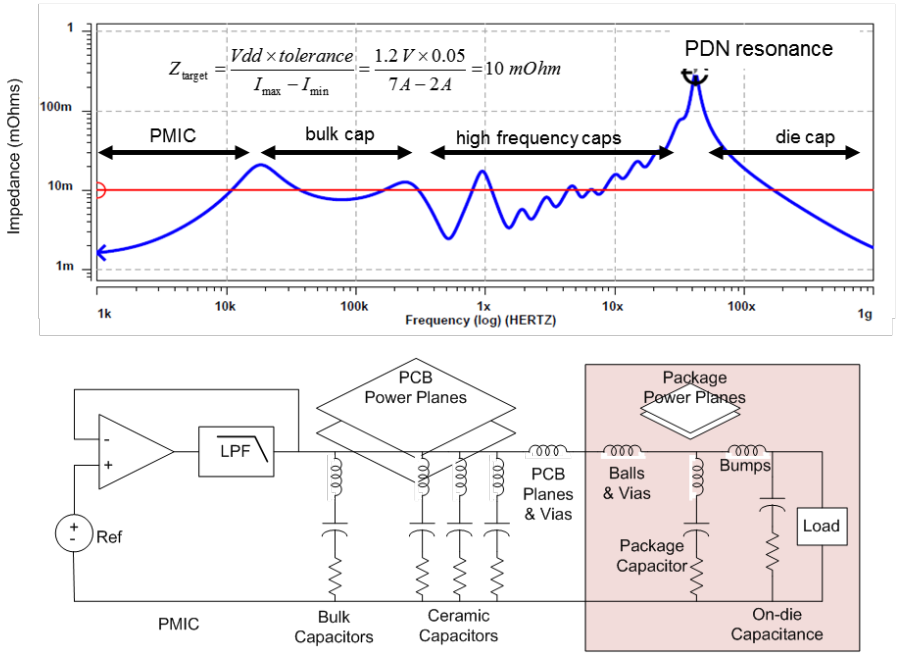


***Figure 1**: PDN components that control frequency domain impedance, from the perspective of the pads of the die.*

The Vdd self-aggression noise depends on the properties of the board-level decoupling capacitors, board power planes and vias, the package balls, package vias, power planes and package caps, and the die bumps, the on-die power grid, and the on-die capacitance for the silicon load as shown in the bottom portion of Figure 1. This is the remainder of the PDN system beyond the VRM. The VRM is also known as the power management integrated circuit (PMIC).

The board and chip level PDN components are important in the 1 MHz to 500 MHz frequency band, which is beyond the bandwidth of the VRM or PMIC as indicated in the top portion of Figure 1. The board level components of the bulk cap, high frequency caps, package caps, and on-die capacitance supply the current and charge consumed by the silicon load above the bandwidth of the VRM.

Silicon loads are capable of consuming full current steps in just a few clock cycles. A 3 GHz microprocessor idling at 2 A might suddenly require 7 A one nanosecond later. Fast step currents must come from energy and charge stored in PDN capacitance. It must come through inductive PDN structures such as the die bumps, package vias, power planes and balls, and board vias, power planes, and capacitor mounting structures. Eventually, several microseconds later, the required power is delivered from the VRM or PMIC.

Target impedance is very useful figure of merit when designing the board level PDN elements to control self-aggression noise on the core logic. In the situation described above, the microprocessor demanded a 5 A step current (7A – 2A) with a 1 nSec rise time. The voltage tolerance for the microprocessor may be 5%; that is, it is expected to function properly with a 3 GHz clock frequency if the voltage stays within the ± 5% tolerance.

A simple Ohms law calculation reveals that the PDN system impedance should be approximately 10 mOhms when the nominal PDN voltage is 1.2V. Using the rule of thumb that the frequency content is $0.35 / t_{Rise} = 0.35 / 1\,\text{nSec} = 0.35\,\text{GHz}$, the PDN should meet the target impedance up to 350 MHz.

$$Z_{target} = \frac{V_{dd} \times tolerance}{I_{max} - I_{min}} = \frac{1.2\,\text{V} \times 0.05}{7\,\text{A} - 2\,\text{A}} = 10\,\text{mOhm}$$

All PDN systems operate in this manner. A server system may rely more on large electrolytic bulk capacitors and lower bandwidth VRM, and a mobile system may rely on a higher bandwidth PMIC and small ceramic capacitors; this is the structure of all PDN systems that supply current to silicon loads. It is from this perspective that we look at some of the VRM models.

What is Missing

The target impedance provides a guideline for designing PDN elements. When using a 5% noise tolerance on the core logic rail, it is assumed all the noise is self-aggression noise. But mutual-aggression noise sources, such as voltage transients from the VRM, or from other switching currents through the board level impedance, can add to the Vdd on-die rail noise.

The package lead inductance and on-die capacitance act as low-pass filters and generally filter out higher frequency components from the board onto the die above the pole frequency of the Bandini Mountain frequency. However, low frequency noise below 10-100 MHz can make its way on the die. This additional noise will add to the 5% noise from the self-aggression sources.

In this initial look, we will focus on self-aggression noise from Vdd transient currents. The simple VRM models introduced to guide the design of PDNs in which Vdd self-aggression noise is analyzed will not predict any of the mutual-aggression noise, such as the switching noise from the VRM, the noise coupling over from the external power source that is not blocked by the power supply rejection ratio (PSRR) of the VRM, or the ringing noise from the transient response of the VRM reacting to step current loads changes. A non-linear VRM model is required to model these sources of noise, as detailed below.

The Simplest VRM Model: An Ideal Voltage Source

The simplest VRM model is an ideal voltage source. This representation has zero output resistance and is the worst model to use in any context because it does not predict any of the most important noise behaviors.

Unfortunately, an ideal voltage source is used to represent the VRM in many time domain power integrity (PI) simulations. The problem with the ideal voltage source is that it is zero impedance and shorts out (DC and AC) any PI component it is across.

The PI design flow often involves extraction of S-parameter models for the printed circuit board. The extraction tool offers ports to attach the VRM, board caps, and packaged silicon components (microprocessor load). Then a circuit simulation tool uses a schematic to connect PDN components to the ports of extracted board and package models. An example of two models is shown in Figure 2.

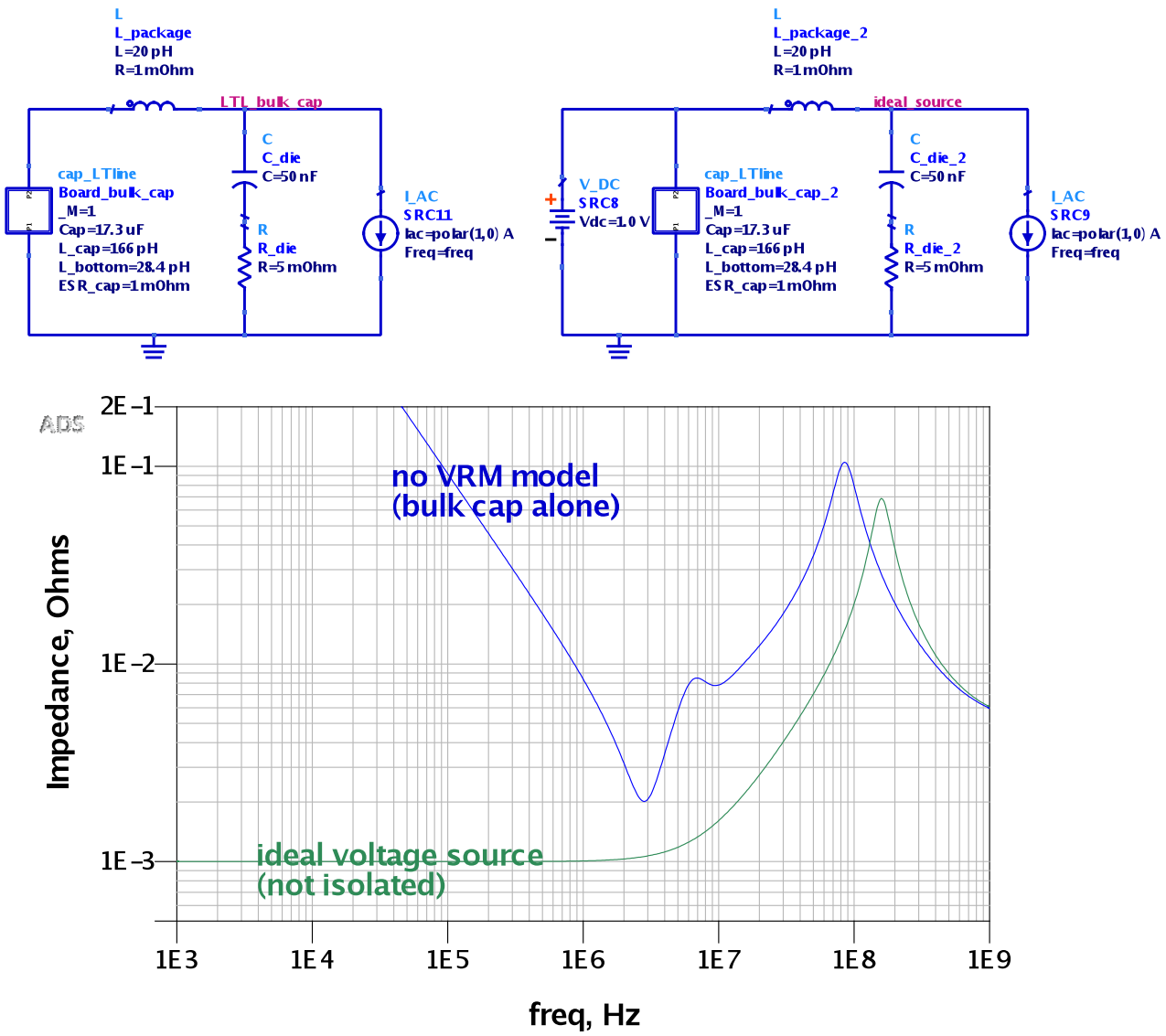


Figure 2: *Schematic on the left shows the impedance simulation of on-die capacitance, package impedance, and board bulk capacitance, and produces the blue impedance curve on the graph. The schematic on the right is identical, but has an ideal voltage source shunting the board cap and produces the green impedance curve.*

The schematic on the left in Figure 2 shows an impedance model of some PDN components. An AC current amplitude of 1 A is forced into the 50 nF on-die capacitance with 5 mOhm ESR. There is a package connection (20 pH, 1 mOhm) to a board bulk capacitor represented by a lossy transmission line model [2]. The simulated impedance versus frequency for this topology is shown in the blue curve (bulk cap alone). The Bandini Mountain impedance peak is clearly seen at 100 MHz, as well as the profile produced by the cap model and package. This is expected behavior.

Software tools are often used to extract the impedance properties of a printed circuit board. There is a temptation to attach an ideal voltage source at the extracted port terminals for the VRM as shown in the schematic on the right in Figure 2.

We have attended many design reviews and found that this tendency of attaching an ideal voltage source as the VRM to the board level S-parameter model is all too common. It is an unfortunate mistake made by many PI engineers.

Attaching a zero-impedance voltage source to the PMIC or VRM port of the extracted PCB effectively shorts out all the PDN components on the board with some small equivalent inductance and resistance associated with the board port connections. This is shown in the schematic on the right in Figure 2. As seen in the graph in Figure 2, the zero-impedance ideal voltage source creates a flat line below 1 MHz and eliminates the signature of the bulk cap. The bulk cap has been shorted out.

The goal in the PDN design and simulation for self-aggression noise is to evaluate the effectiveness of bulk caps, high frequency caps, board power plane connections, and so forth; therefore, shorting them out with an ideal voltage source is a major error. Unfortunately, many PI analyses have been corrupted by using an ideal voltage source.

It is very important that ideal voltage sources are **never** used in PDN simulations, especially when impedance or transient responses to fast step current loads are being evaluated.

A First-Order Linear RL Model for a VRM

The simplest linear model that represents the VRM output impedance behavior, and is commonly used for frequency domain simulations, is a series RL model. This model has the advantage of being easy to implement and accounting for some of the interactions of the VRM with the rest of the PDN, from the die's perspective, when simulating Vdd self-aggression noise. Of course, this simple model cannot begin to address the non-linear, stability, noise ripple, and saturation properties of a real VRM.

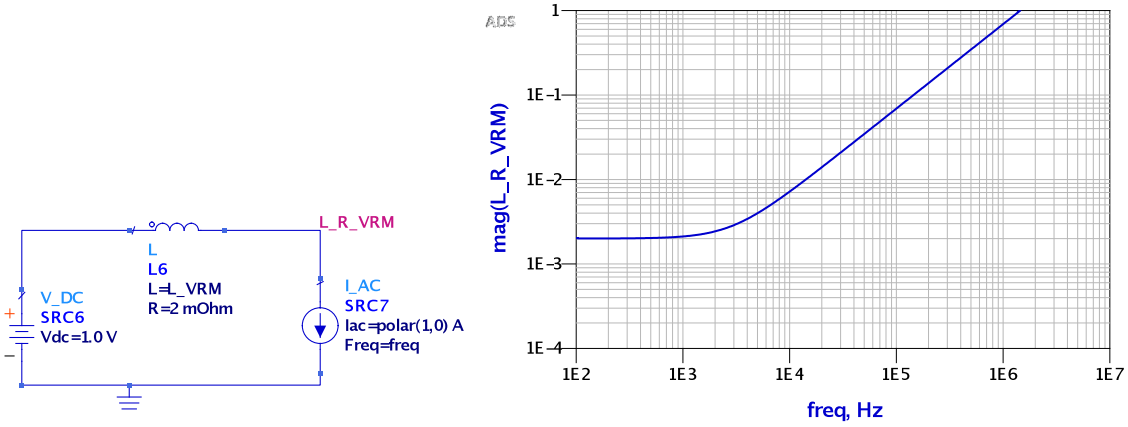


Figure 3: *RL model for VRM.*

As illustrated in Figure 3, the output impedance rise of the VRM due to the internal feedback response bandwidth, is well represented by an inductor and resistor. The resistor represents the VRM voltage drop that is proportional to DC current. The inductor provides an increasing impedance with frequency beyond some corner frequency.

The inductance value is calculated from the current ramp response time or by matching the resonant frequency between the VRM inductance and bulk (output) capacitance. Note that the inductance value for the simple linear model is not related to the inductor value in the SMPS model. The inductor of the

linear RL model simply captures the behavior of the regulation loop (either SMPS or LDO), and does not represent any physical element. The resistance value (R) in the VRM model (R_VRM) is simply the resistance at DC or some very low frequency (100 Hz) at which the impedance curve bottoms out.

A frequency domain calculation for the inductance of the inductor in the VRM model (L_VRM) is based on the frequency of the VRM impedance peak. This can be found by measuring the impedance of a VRM system as a function of frequency. Due to the non-linear nature of all VRMs, the frequency and height of the VRM impedance peak are not unique and change slightly according to load conditions. Properties change from lightly loaded conditions (small signal and linear) to full load transient conditions in which damping is highly load dependent. Nonetheless, the frequency of the VRM impedance peak is relatively stable.

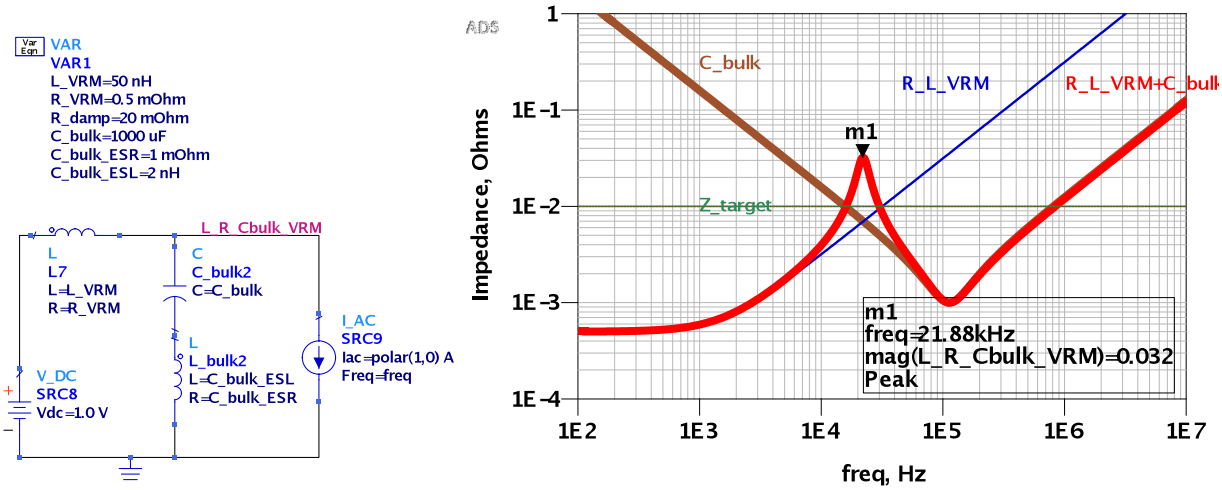


Figure 4: *Two-element RL model and RLC bulk cap model show high VRM impedance peak. The peak frequency is used to find the equivalent VRM inductance.*

Figure 4 shows a VRM impedance peak at about 22 kHz because of the resonance between the bulk capacitance and the effective VRM inductance. The capacitance is extracted from the measured impedance with the VRM turned off, or from knowledge of the capacitance components used. Although this is the total on-board capacitance, it is dominated by the bulk capacitance. The effective VRM inductance is calculated from the resonant frequency and on-board capacitance.

$$f_0 = \frac{1}{2\pi\sqrt{L \times C}} \quad \text{and} \quad L_{Loop} = \frac{1}{(2\pi f_0)^2 \times C} = \frac{1}{(2\pi \times 22\,kHz)^2 \times 1000\,\mu F} = 52\,nH$$

This is the inductance in the resonant loop that causes the impedance peak at 22 kHz. The schematic parameters indicate that the simulated parameter for the VRM was 50 nH and the inductance of the bulk capacitor was 2 nH, the sum of which is 52 nH. This demonstrates that the resonant peak frequency can be used to determine what the equivalent VRM inductance must have been. The VRM resonant peak can be measured.

It is highly desirable that the inductor impedance cross the capacitor impedance exactly at the target impedance line. In the literature, this is known as impedance matching [3] or the characteristic impedance that gives a good PDN step response [4]. This impedance is the special point at which

inductive reactance crosses the capacitive reactance and the target impedance line. We want the characteristic impedance of the VRM peak, $Z_0 = \sqrt{L/C}$, to be the same as the target impedance to keep the step response at or below the voltage droop tolerance, with a low q-factor to damp out any ringing. This results in a maximally flat impedance profile that is sufficiently low to deliver the full transient current with a droop that is within the voltage tolerance.

A time domain calculation of the inductance parameter comes from the $V = L \times di/dt$ property. When the load demands a fast step of current, the output of the VRM is limited by a maximum current rise time (di/dt rate). The rise time for the load from a Vdd rail transient current step is often expressed in amps/nSec; the time for the VRM response is often given in amps/uSec, 1000 times slower.

The equivalent inductance for the linear VRM model can be determined using this property. When the VRM is driven by a ramp current load, the voltage response of the VRM is a measure of the output inductance. The equivalent large signal inductance of the VRM is calculated from $V = L \times di/dt$. In the special case in which the VRM inductive reactance crosses the capacitive reactance at the target impedance, the voltage drop for a step current of the worst-case transient Vdd current will be the same as the voltage tolerance used in the target impedance calculation.

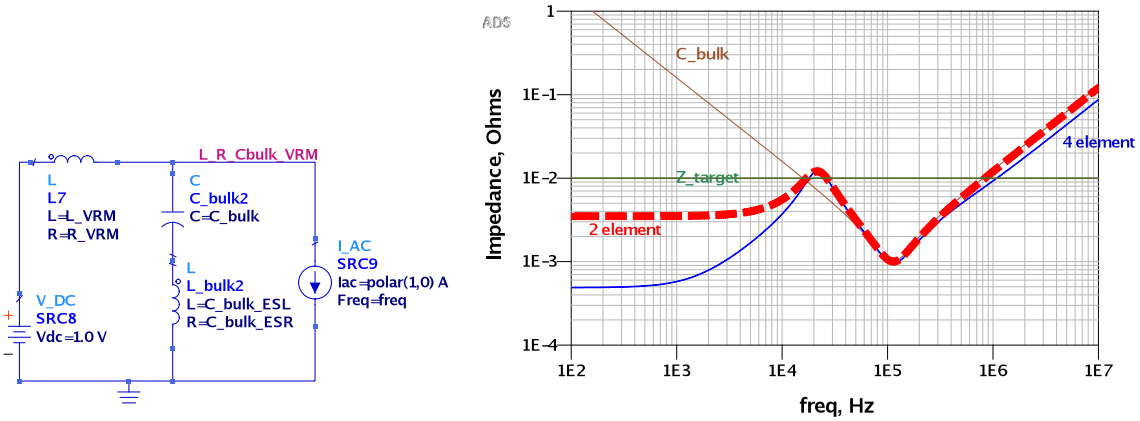


Figure 5: *The height of the impedance peak can be adjusted by increasing VRM resistance, but this would increase the DC resistance and contribute to an undesirable DC IR drop.*

The height of the impedance peak in the parallel resonance of the VRM output inductance and the bulk capacitor's capacitance is determined by system losses, including the losses attributed to the bulk cap. It is tempting to choose R for a 2-element series RL model to properly damp the impedance peak, but as shown in Figure 5, this would lead to excessive resistance in the path from the ideal voltage source and too much DC IR drop.

The R in the RL model needs to satisfy two properties: provide the correct damping for the parallel resonant peak and provide the correct DC output impedance. One single value can rarely do this. A more accurate model must include two values of resistance, and to be effective in the circuit, two series inductor values. This is a 4-element RL model.

Second Order Model of the VRM: A 4-element RL Model

Modeling the VRM as the parallel combination of two series RL circuits, as shown in Figure 6, offers a simple, linear circuit model for a VRM that includes a more accurate representation of the DC or low frequency impedance, the equivalent inductance of the feedback loop, and the damping resistance needed to account for the first parallel resonant peak.

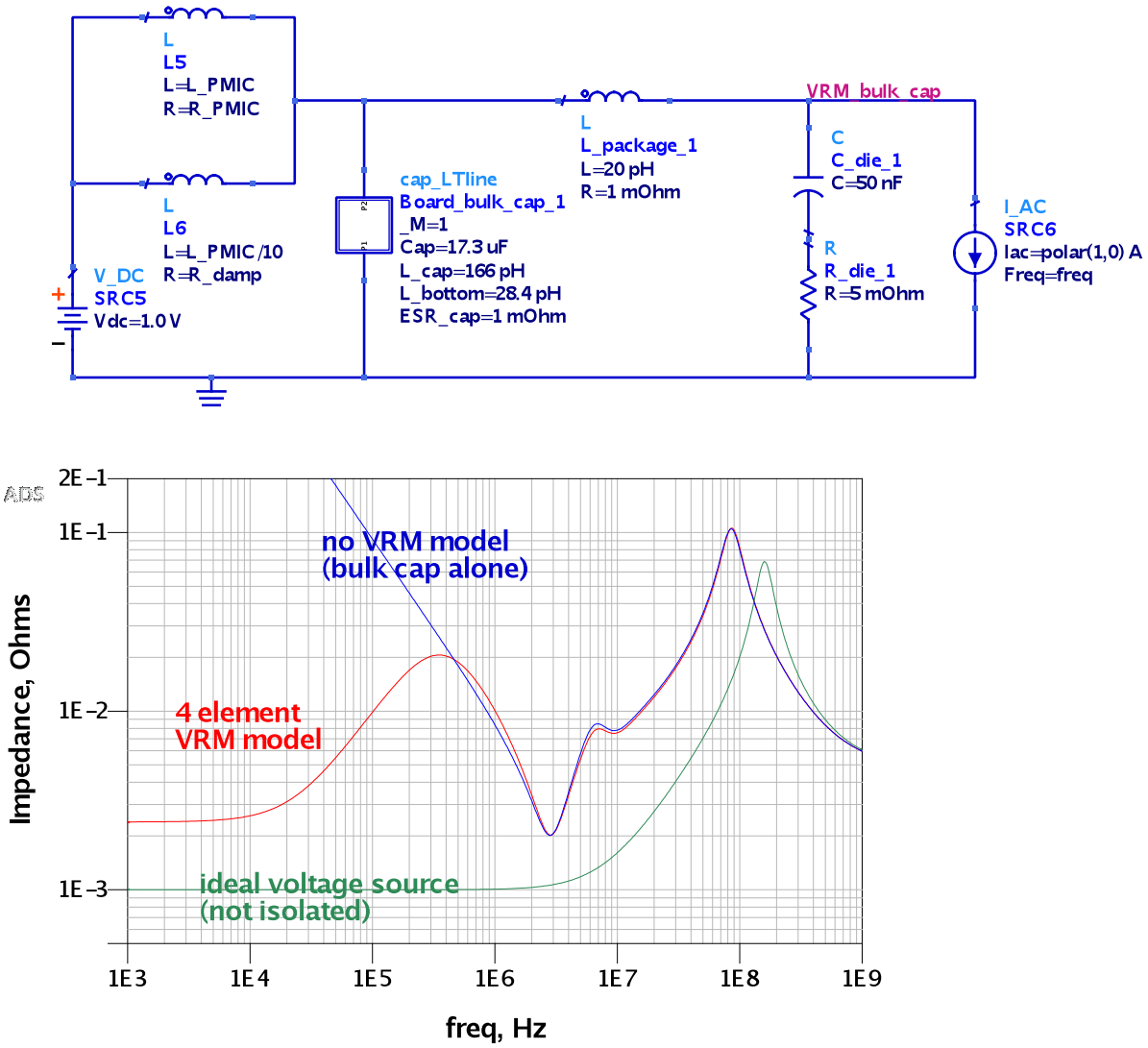


Figure 6: *A simple, linear, 4-element VRM model isolates the ideal voltage source from the rest of the PDN components and produces the red impedance curve. The impedance peak at about 300 kHz is due to the VRM output inductance interacting with the on-board bulk capacitor. The impedance peak between on-die capacitance and bump-package loop inductance appears at about 100 MHz as it should.*

This 4-element RL model has little impact on the higher frequency Bandini Mountain peak but will affect the lower frequency parallel resonance between the VRM and the bulk capacitor. This model is useful

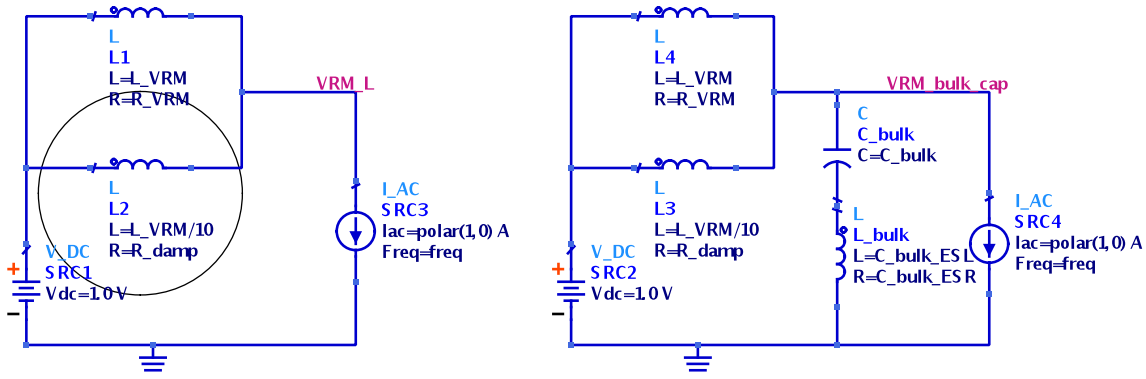
when analyzing on-die Vdd self-aggression noise. The element parameters can be chosen to give reasonably accurate simulation results in both frequency and time domains with this linear model.

If the VRM feedback points are internal to the VRM, then the VRM may be attached schematically to the VRM port on the extracted PCB. The port may be for a SMPS inductor if the bulk cap is mounted on the PCB power planes.

If, however, there are external feedback sense lines for the VRM that extend to some point in the PDN system (often some location on the board underneath a high-power consuming load), the mount point for the VRM model should not be at the VRM port. Special PCB ports should be created to mount the linear VRM model with low resistance and inductance connections close to the sense line terminations.

A real VRM with external sense points will regulate the voltage at the sense points. A simple linear VRM model has no provision for feedback compensation. If the simple VRM model is mounted at the extracted PCB port locations, DC IR voltage drop from the VRM port to the PCB feedback point will not be compensated.

The second resistor (R_damp) is used to independently damp the impedance peak while the first resistor is used to set the proper DC IR drop. A good starting value for R_damp is the target impedance, which would result in a q-factor of 1. This can be refined by PDN measurement of an active VRM with a VNA. The VRM will not deliver significant current at high frequency, so a second inductor with a value of approximately L_VRM/10 is used to model the blocked high frequency current. The 4-element VRM model delivers the blue curve seen in the graph in Figure 7. It provides the damping that brings the VRM impedance peak down to the target impedance without impacting the DC IR drop at low frequency.



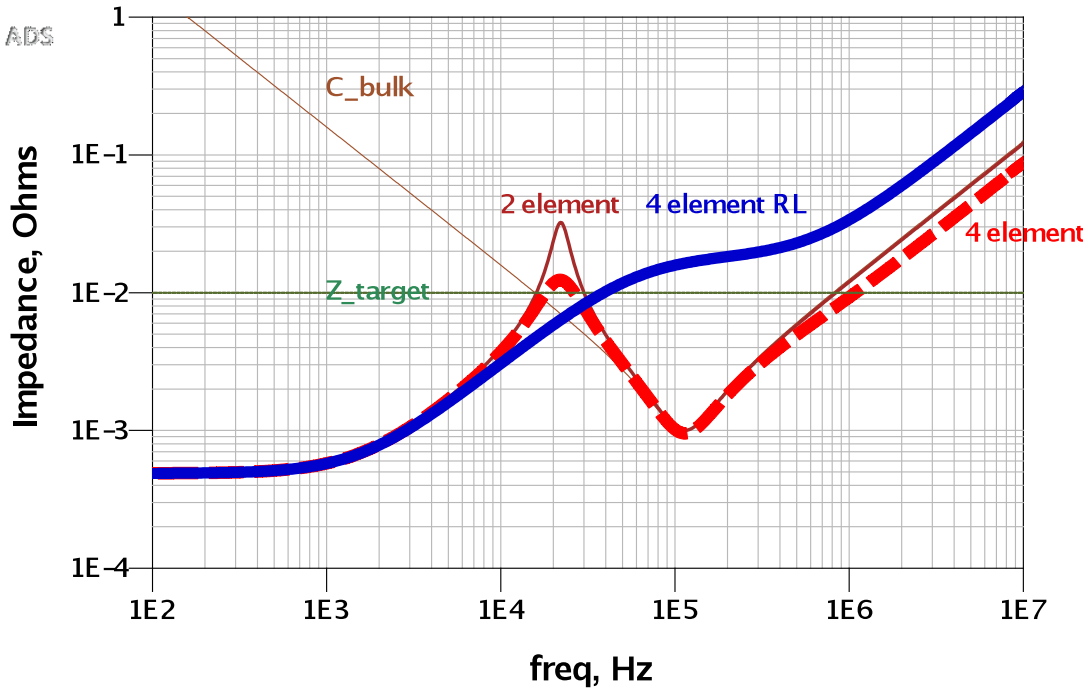


Figure 7: *Proper DC IR drop and damping for the VRM peak is achieved at the same time by adding an additional R and L to the 2-element model.*

Modeling Other Noise Sources: VRM Self-Aggression

None of these linear models can account for any of the noise on the Vdd rail from VRM-aggression, which can be caused by an inadequate PSRR and noise on the primary power source, switching noise from the internal VRM operation, or nonlinear transient response from changing current loads.

Any of these effects will generate more noise on the pins of the VRM and appear on the Vdd rail pads if their frequency components are below the pole frequency of the Bandini Mountain. These noise sources will add to the Vdd self-aggression noise caused by Vdd transient currents. In extreme cases, VRM and other aggressor noise can exceed the self-aggression noise tolerance and cause larger problems.

The factors that contribute to these noise sources are often not related to the PDN design features that we optimized to reduce the Vdd self-aggression noise. These factors must be analyzed and addressed independently of design features introduced to reduce the Vdd self-aggression noise.

A model that includes the non-linear feedback and PSRR of the VRM is required. Recent advances in VRM modeling techniques, which include harmonic balance and state space equations, have greatly reduced the complexity of VRM models and enabled faster simulation [1].

An accurate VRM model reflects the non-linear properties of transistors and feedback loops that occur when load currents transition from very low to very high values and the VRM is at the limit of its current delivery range. The accurate VRM model also takes into account switching noise and PSRR effects, as well as small- and large-signal impedance effects. Accurate models are required for closed loop feedback simulations to determine the best circuit elements and parameters for stability analysis. Accurate VRM models are required for optimal VRM design and integration into the entire PDN system.

As an example, a simple SMPS buck converter schematic is shown in Figure 8. It converts some higher DC voltage to a DC voltage appropriate for CMOS logic, often about 1 V. It involves complex circuitry to sense and regulate the output voltage, monitor current, open and close switches at appropriate times, and maintain stability over different load conditions.

Basically, the top switch remains closed until the working inductor is fully charged with current. The bottom switch is then closed to allow current to continue through the inductor loop while the loop current and energy stored in the working inductor diminishes. Complex circuitry and algorithms enable this class of regulators to function. Simulation and modeling of the SMPS is a major discipline in itself and significant design efforts and computer resources have been dedicated to these efforts. Ultimately, it is with such models that the interactions of the VRM with the rest of the PDN can be analyzed and each element optimized.

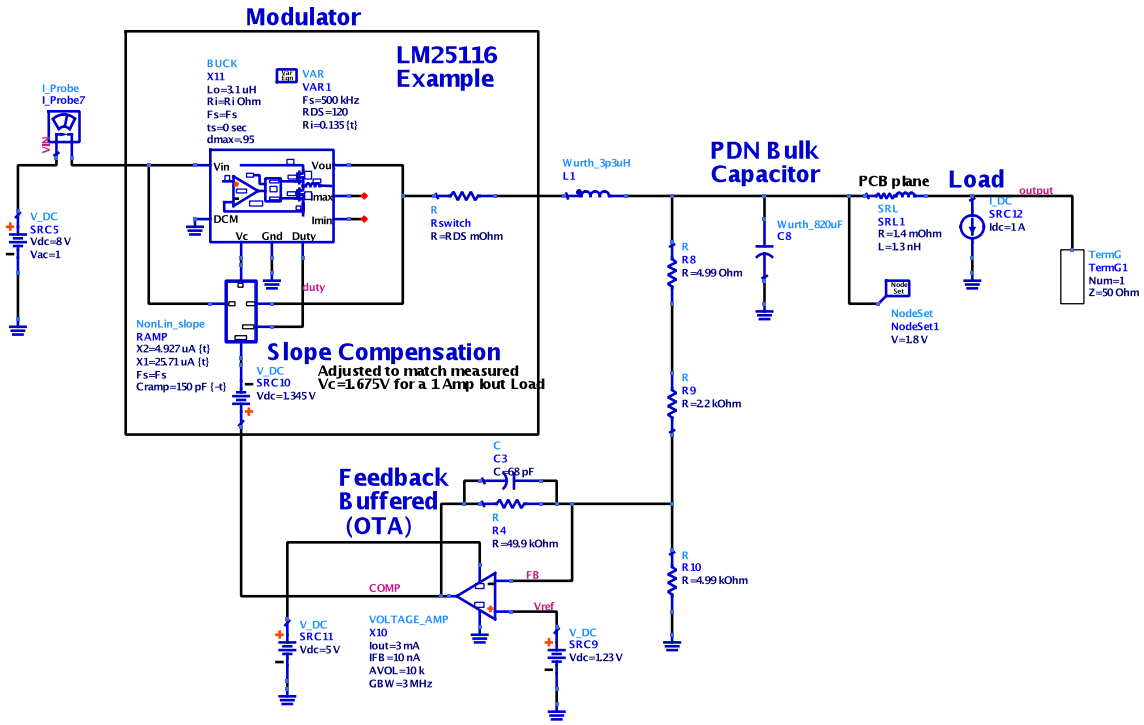


Figure 8: *Buck converter VRM.*

Conclusion

It is important to use a proper VRM model in PI simulations. An ideal voltage source should never be attached to a port of an extracted printed circuit board S-parameter model, as is often done, because it shorts out a significant portion of the PDN with zero impedance.

The ideal voltage source must be isolated from the board power planes and discrete capacitors by an impedance that represents the VRM. Preferably, the VRM model is tuned and correlated to regulator spec sheets and actual VRM measurements. If this information is not available, a 4-element RLRL model with an impedance peak at approximately the right magnitude and frequency may be used. The RLRL

parameter values may be determined from the properties of the impedance peak. The VRM model affects the PDN impedance curve in a certain frequency band, often 20 kHz to 20 MHz.

Although linear models for the VRM are critical for optimizing the board level PDN to manage Vdd self-aggression noise, they cannot provide any insight into noise that originates with the VRM.

For a complete description of the noise in the PDN, including the VRM self-aggression noise, a non-linear model is needed and can be implemented using a state space model.

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