



Network Synthesis Accelerates Impedance-Matching Circuit Design

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Introduction

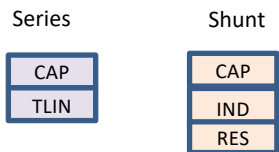
- The use of synthesis for matching networks can streamline design flows for a variety of RF and microwave applications:
 - High-power amplifiers (PAs), including harmonic matching
 - Low-noise amplifiers
 - Antenna matching, including multiple bands
 - Interstage matching in amplifiers
- Enables the designer to quickly explore a wide variety of matching network topologies
- Can work directly with load-pull data in the case of PAs
- Very useful at the beginning of a design to determine reasonable performance targets such as device sizing, decisions on active device periphery, performance limits, and more)

Synthesis Approach

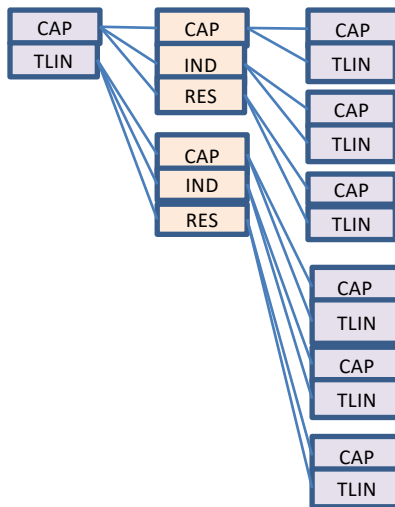
- Recent advances in computer processing power and algorithms have made possible new approaches to matching network synthesis
- More specifically, ~10 million circuit responses per second on a modern PC can be evaluated
- A variant of genetic optimization is used as the underlying algorithm for parameter values
- This method has proven to be very effective for circuit design problems

Search-Based Synthesis Engine

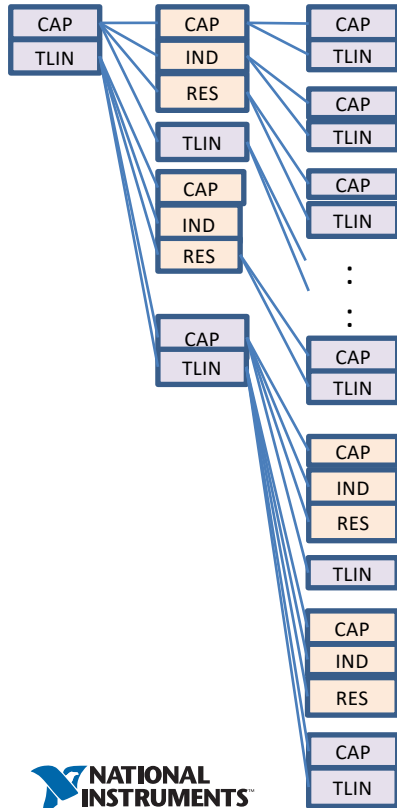
User decides which series and shunt elements to consider



Then, all possible topologies are explored by expanding the solution up the maximum number of user-defined matching sections



Search-Based Synthesis Engine - 2



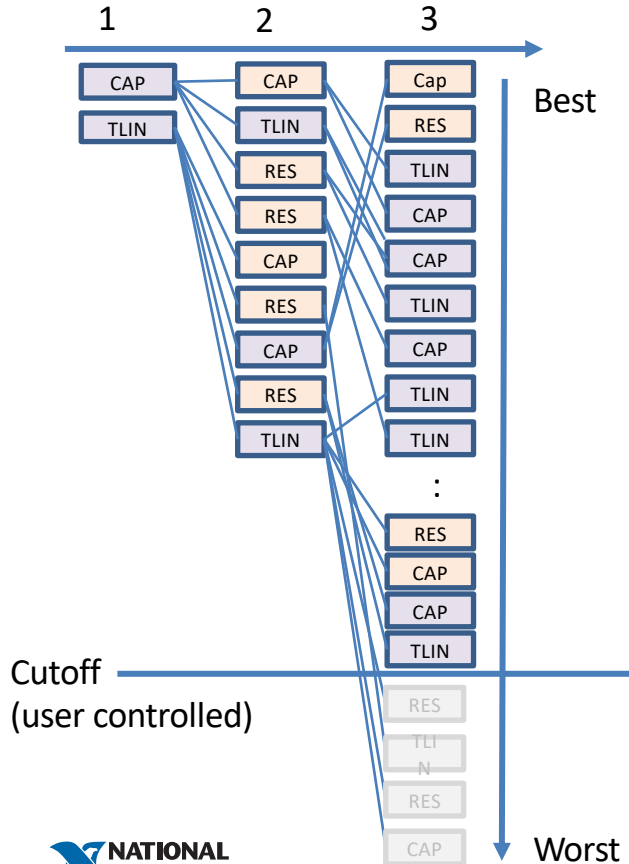
Heuristics are used to determine what can follow an existing element

- For example, a series TLIN can follow a series TLIN (for stepped impedance transmission lines)
- But, a series CAP cannot follow a series CAP

Practical considerations are also taken into account

- DC open and short paths
- Component limits and discrete values
- Impact of bias and feed networks
- Constraints on first/last elements in the network

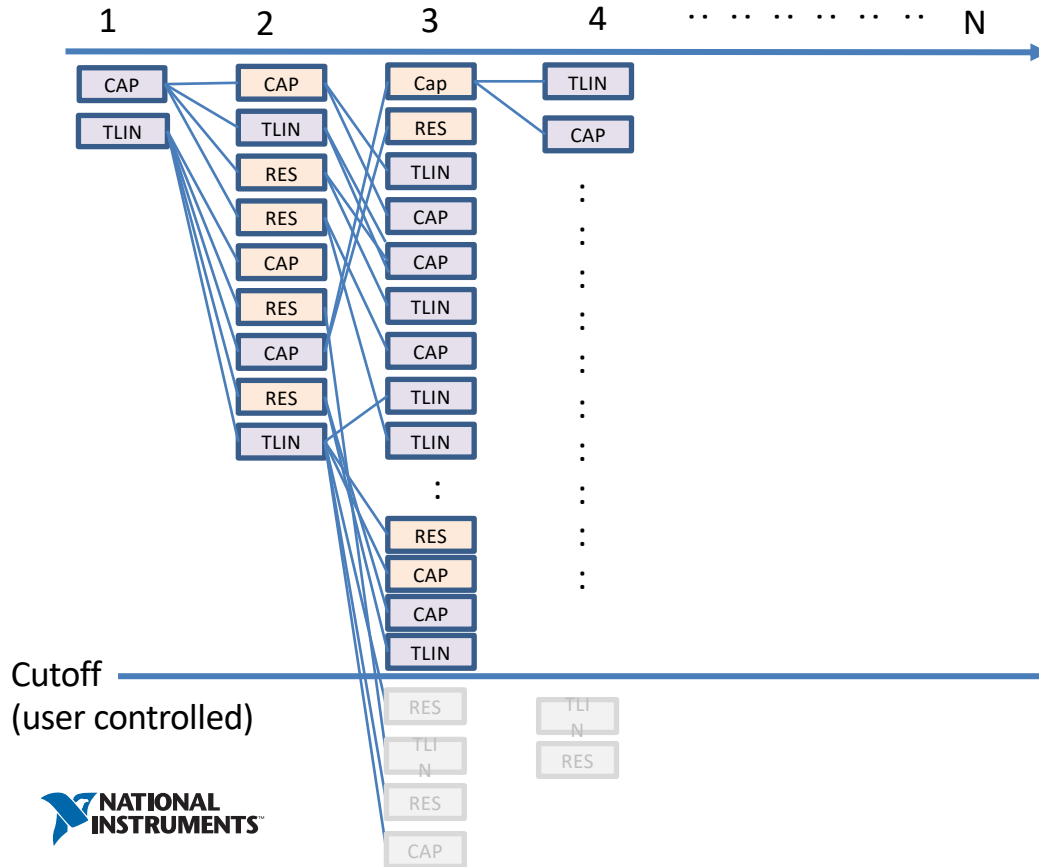
Search-Based Synthesis Engine - 3



Solutions are sorted from best to worst as each expansion is added

The user has some control over the threshold for which solutions are considered for the following expansion (this allows tradeoffs between speed and search depth)

Search-Based Synthesis Engine - 4



Overall result is an extremely comprehensive search

Controlling the Search Space

Network Synthesis - Example

Synthesis Definition Components Parameter Limits DC & Bias Feed Goals Search Options Results

Series components for search

Series component type

- ☒ Inductor
- ☒ Capacitor
- ☐ Resistor
- ☐ TLine

Shunt components for search

Shunt component type

- ☒ Capacitor
- ☒ Resistor
- ☐ Series RL
- ☐ Series LC
- ☐ Open TLine
- ☐ Short TLine

Topology constraints

Maximum number of sections 6

First component (Port A side) Any

Last component (Port B side) Any

☐ Replace TLines with MLINs

Select MSUB

Search space size (approximate)

Sections	Topologies
4	220
5	812
6	2944
7	10760
8	39184

Synthesize To MWO Close

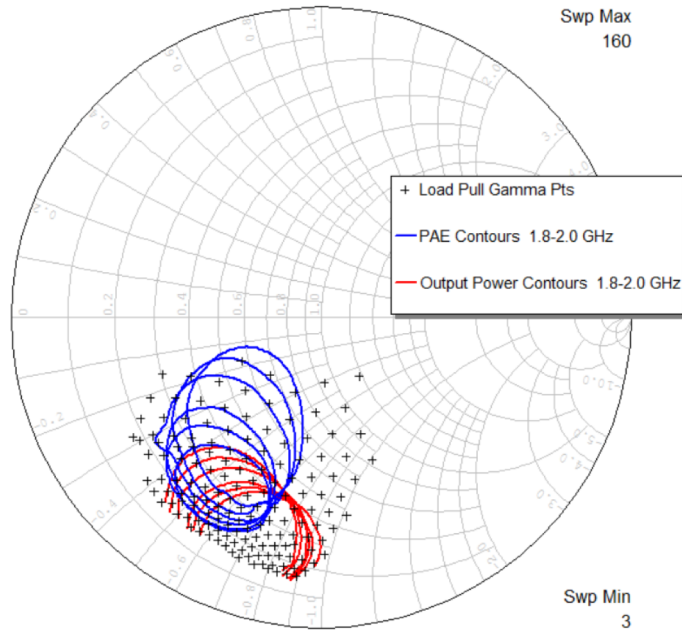
The user can set:

- Component types
- Elements in shunt and series
- Topology constraints (especially first and last elements)
- Number of sections

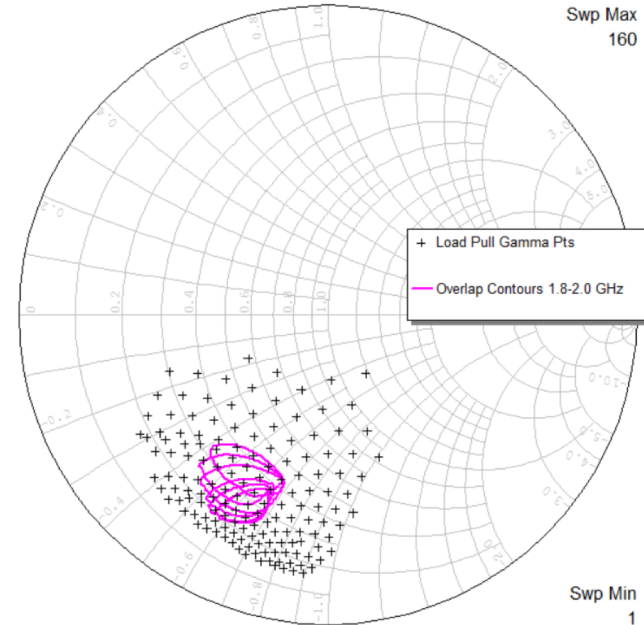
Load-Pull Example

Load-pull data can be used for the loads

Power and PAE Contours 5 Ohm



Power and PAE Contours 5 Ohm



5-ohm Smith chart to see the contours better

Load-Pull Example – Setting the Goals

Measurement

400AV_m1510_Carrier_28V_900mA_1805_1995MHz:LoadPull_A(PLoad,1,G_CompressMG,1,1)[Auto]

BLC8G20LS_400AV_m1510_Carrier_28V_900mA_1805_1995MHz:LoadPull_A(PAE,1,G_CompressMG,1,1)[Auto]

BLC8G20LS_400AV_m1510_Carrier_28V_900mA_1805_1995MHz:LoadPull_A(PLoad,1,G_CompressMG,1,1)[Auto]

New/Edit Meas...

Goal Type

☒ Meas > Goal

☐ Meas < Goal

☐ Meas = Goal

Range

Start ☒ Min ☐ Max

MIN GHz MAX GHz

☒ Enable goal

OK

Cancel

Help

Cost=Weight * | Meas-Goal | ^L

☐ Sloped

Goal 51 dBm Weight 1

☒ Use default L

L 2

Measurement

S_400AV_m1510_Carrier_28V_900mA_1805_1995MHz:LoadPull_A(PAE,1,G_CompressMG,1,1)[Auto]

BLC8G20LS_400AV_m1510_Carrier_28V_900mA_1805_1995MHz:LoadPull_A(PAE,1,G_CompressMG,1,1)[Auto]

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New/Edit Meas...

Goal Type

☒ Meas > Goal

☐ Meas < Goal

☐ Meas = Goal

Range

Start ☒ Min ☐ Max

MIN GHz MAX GHz

☒ Enable goal

OK

Cancel

Help

Cost=Weight * | Meas-Goal | ^L

☐ Sloped

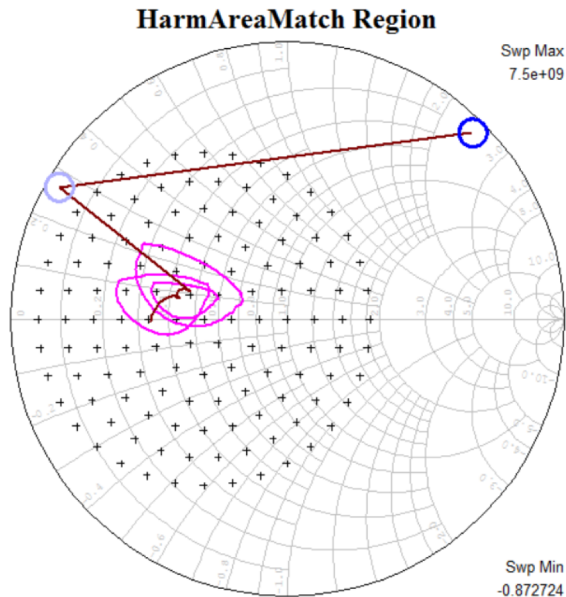
Goal 63 % Weight 1

☒ Use default L

L 2

- Goals are based directly on load pull data....that is to say, actual performance targets rather than impedance targets
- Can be based on sub-bands if necessary, rather than the entire frequency band

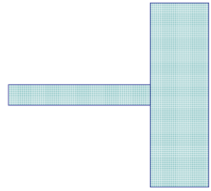
Load-Pull Example – Other Goals



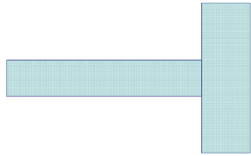
- Additional goals, which aren't load-pull based, can also be added
- For example, a Smith chart region target for second or third harmonics

Load-Pull Example – Comparing Results

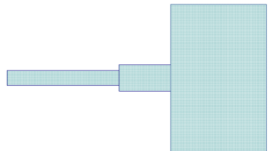
Candidate 1



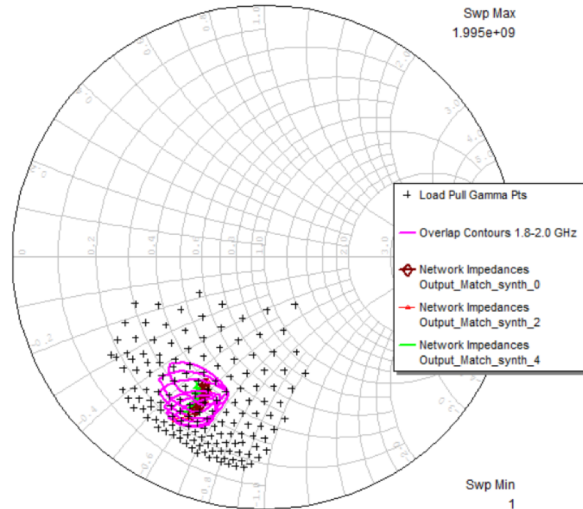
Candidate 2



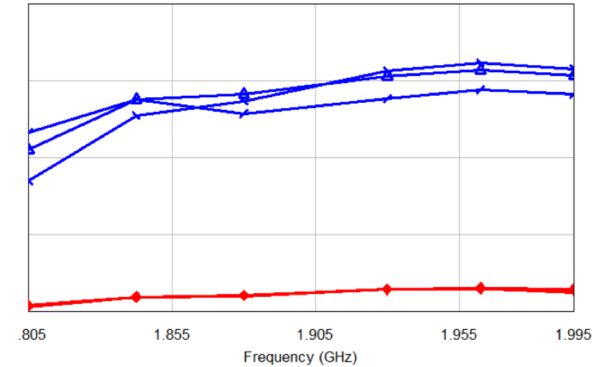
Candidate 3



Power and PAE Contours 5 Ohm



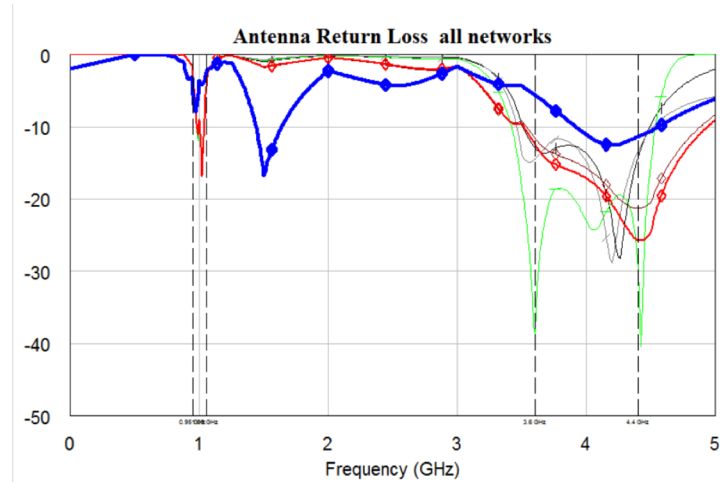
Performance vs Frequency



- At the end of the synthesis run, a user-defined number of candidate networks are generated
- Easy to compare performance results of each network

Additional Applications

- Direct conjugate matching
 - Useful for broadband and multiband antenna matching
- Inter-stage matching
 - Driver to power amplifier inter-stage match
 - Matching between two sets of complex impedances across frequency is often time consuming when done manually
- Noise match
 - For low-noise amplifier applications
 - Can be combined with other synthesis goals
- Smith chart impedance targets
 - Can also be used for fundamental frequency targets



Antenna matching for three sub-bands

Conclusions

- Matching network synthesis has been added to Microwave Office circuit design software
- A ladder-type filter is created using genetically-based synthesis algorithms
 - They evaluate a large number of possibilities (computers are fast!)
- It works for matching any input and output load
 - PA matching – can use load-pull data for for harmonic-load matching
 - Antenna matching – multi-band match