High-Speed Board Design Rules

to Get Your PCB Designed

Right the First Time

Shalom Shlomi Zigdon

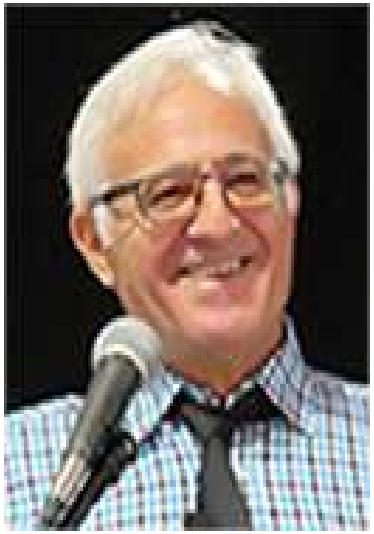
+972509771770 Whatsup / Linkedin

Shalom-shlomi-zigdon@itech-icollege.com

www.iTech-iCollege.com

About me

My name is: **Shalom Shlomi Zigdon**



CEO of iTech iCollege – Board Design Academy

1981-2001 20 yrs as HW Engineer, VP Engineering, Startup CEO

2014-2018 Chairman of IEEE Symposium **Signal Integrity & EMC** Conference

2017-2018 TAC [Technical Advice Committee] member of Boston EDI CON

2002-today Hi-Speed Consultant for SI/PI/EMC + PCB Layout

Lecturer and CEO at Board Design Acadmy for SIPI&EMC

1981 B.Sc. in Electronics, Technion, the Israel institute of technology.

1985 M.A in Project Management, University of Haifa, Israel

2002 C.I.D. at Silicon Valley IPC Designers Council

Shalom-Shlomi-Zigdon@iTech-iCollege.com

2017+2018 TAC [Technical Advisory Committee] Members:

Eric Bogatin
Steve Sandler, Managing Director, Picotest
Shalom Shlomi Zigdon, CEO & Owner, iTech iCollege Israel
Bert Simonovich, Consultant & Founder LAMSIM Enterprises Inc.

Tim Boles, Technology Fellow & Director of Strategy, MACOM
Syed Bokhari, Technical Manager SI & EMC, Fidus Systems, Inc.
Gregory M. Bonaguide, Senior Product Line Engineer R&S USA, Inc.
Diana Baxter, Director of Engineering, Peregrine Semiconductor
Antonio Ciccomancini Scogna, Principal Engineer, Samsung
Jay Diepenbrock, SI/RF Consultant
Lewis Dove, SI Architect, Keysight Laboratories—ASIC Technology
Patrick Hindle, Editor, Microwave Journal
Sheena Hussaini, PhD, R&D Engineer, Nokia
Henry Lau, CEO, Lexiwave Technology, Inc.
Gary LeRude, Technical Editor, Microwave Journal
Anil-Kumar Pandey, Principal R&D Engineer, Keysight Technologies
Ray Pengelly, GaN Power Amplifier Design Consultant
Granthana Rangaswamy, Senior System SI Engineer, Juniper Networks
Kalyu Zhao, R&D Engineer, Synopsys

Boston EDI CON 2017

IPC-2251 High-Speed PCB Design Committee members since 2002

IPC-2251 Task Group

Amit Bhardwaj, Polar Instruments (AP) Pte. Ltd.

Dr. Eric Bogatin, Giga Test Labs

Robert Bremer, Litton Systems Inc.

Christine R. Coapman, Delphi Delco Electronics Systems

David J. Corbett, Defense Supply Center Columbus

Theodore Edwards, Dynaco Corp.

Werner Engelmaier, Engelmaier Associates, L.C.

Martyn Gaudion, Polar Instruments Limited

Michael R. Green, Lockheed Martin Space Systems Company

Richard P. Hartley, C.I.D., Hartley Enterprises

Phillip E. Hinton, Hinton 'PWB' Engineering

David H. Hoover, Flextronics

Michael Jouppi, Thermal Man, Inc.

Thomas E. Kemp Rockwell Collins

George T. Kotecki, Northrop Grumman Corporation

Rene R. Martinez, Northrop Grumman

Deepak K. Pai, C.I.D.+, General Dynamics-Advanced Information

Nicholas G. Paulter, NIST

Lee W. Ritchey, Speeding Edge

Mohammad Rahnavard, Xerox Corporation

John Reynolds, Rogers Corporation

Lowell Sherman, Defense Supply Center Columbus

Ken Taylor, Polar Instruments, Inc.

Daniel Welch, Arlon MED

Philip R. Wellington, L-3 Communications

Shlomi Zigdon, B.Sc., C.I.D., Shlomi Zigdon Technologies Ltd.

USA Activities

EDI CON: Santa Clara 2018 + Boston EDI CON 2017

IPC - A committee-member of 3 **IPC Standards**:

IPC-2251 Hi-Speed Board Design for Signal Integrity

IPC-2221 PCB Design

IPC-2226 HDI- Hi Density PCBs Design.

Seminars & Consultant

5 Days Course - Intel Santa Clara 2015 +

Project PCB Design and Simulations – BD, Maryland

San Diego - PCB Layout & Simulation 2016

NYC Hilton – Hi-Speed Board Design 2017

Next USA Seminars [hopefully] :

Santa Clara January 28-31

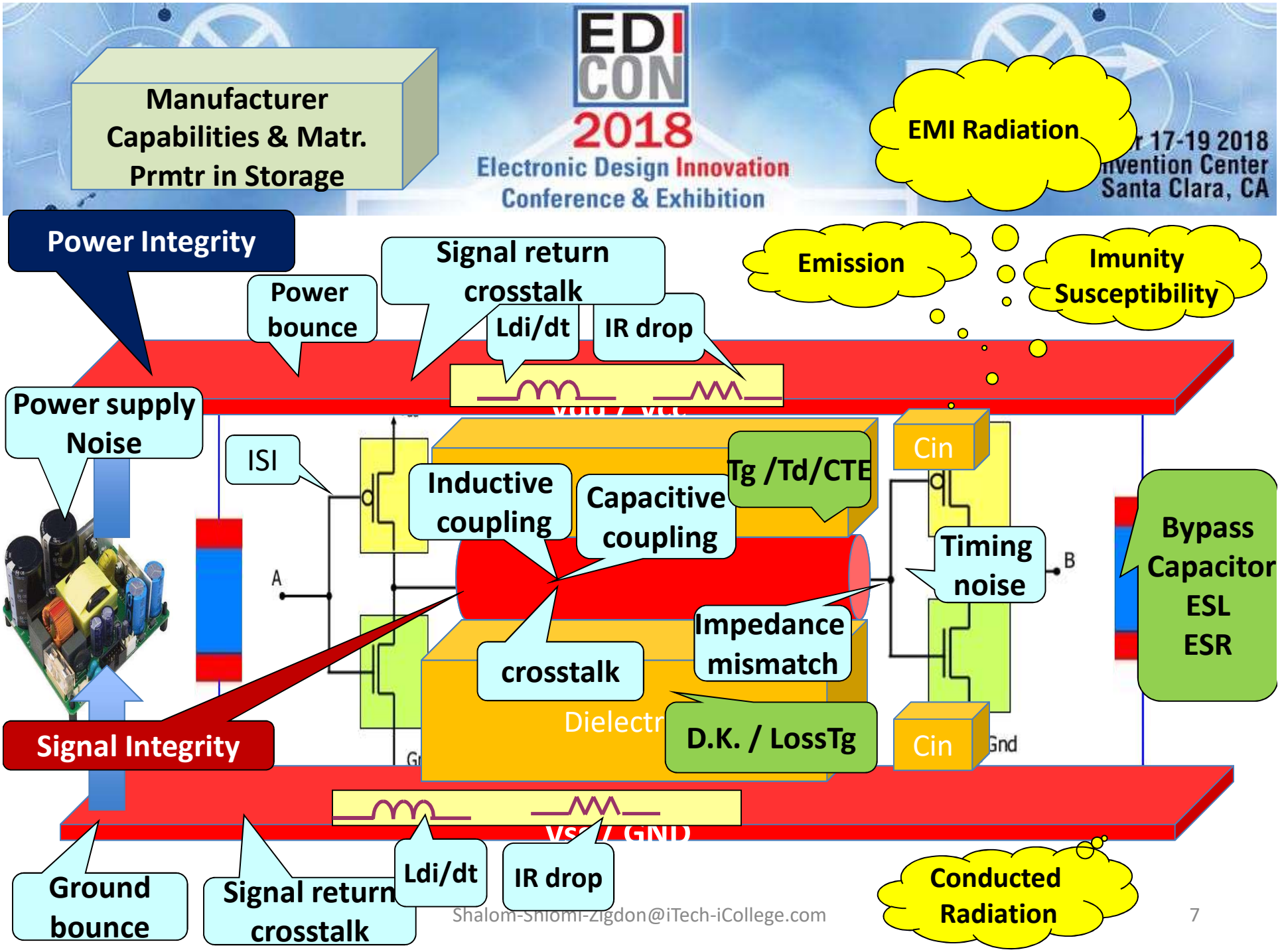
Los Angeles April 15-18

Agenda

SI/PI/EMI main problems

What prevent us from The first time right possibility

Practical guidelines to the PCB Layout Design


Manufacturer Capabilities & Matr. Prmtr in Storage
EMI Radiation
Power Integrity
Emission
Imunity Susceptibility
Signal return crosstalk
Power bounce
Ldi/dt
IR drop
Power supply Noise
ISI
Inductive coupling
Capacitive coupling
Tg /Td/CTE
Cin
Timing noise
B
A
Bypass Capacitor ESL ESR
Impedance mismatch
crosstalk
Dielectr
D.K. / LossTg
Cin
Gnd
Signal Integrity
Ground bounce
Signal return crosstalk
Ldi/dt
IR drop
Conducted Radiation

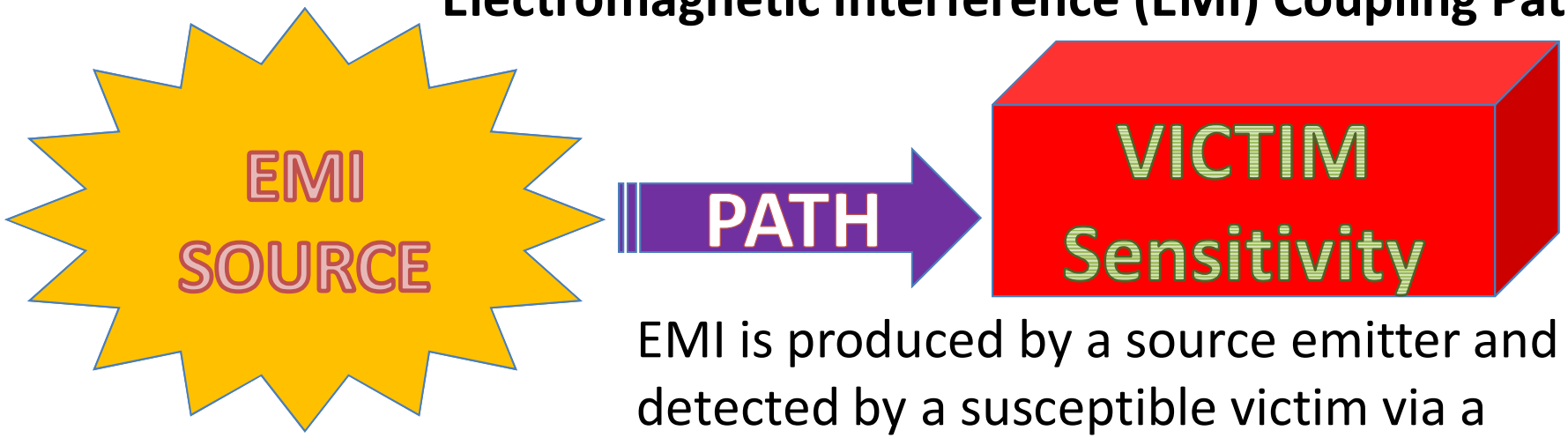
Definition of EMI

Any Electro Magnetic phenomena causing an equipment or system to malfunction

Definition of EMC

The Capability of a system to perform as designed in the intended Electro-Magnetic Environment

Electromagnetic Interference (EMI) Coupling Path



EMI is produced by a source emitter and is detected by a susceptible victim via a coupling path

mechanisms:

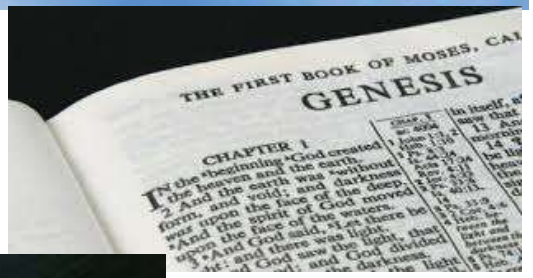
1. **Conduction** - **electric current**
2. **Radiation** - **electromagnetic field**
3. **Inductive Coupling** - **magnetic field**
4. **Capacitive Coupling** - **electric field**

Right the First Time?

An impossible mission

Even God did not create the world Right the First Time!!!

The Book of Genesis



the Book of Genesis chapter 1:

1

....

....

31

re was

ev

th

11

ence.

12

le on earth

ha

13

for the earth

is

troy both

them and the earth.

Adam & Eve where in Paradise
with a Snake inside it

our Project may look like Paradise
as long as it's at the Schema stage

but The PCB is full of Snakes

The Snake desired Eve

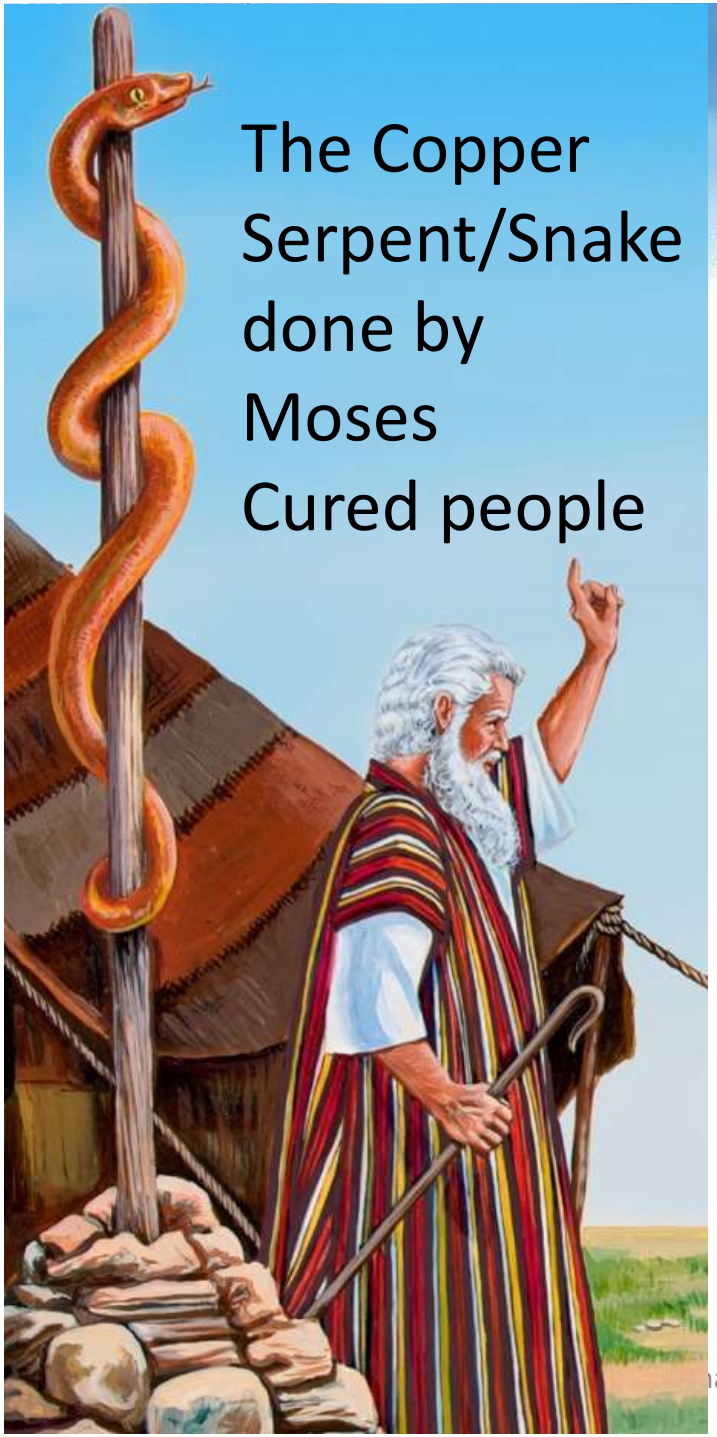
I can understand that

God did not

Genesis:**23**

So the LORD God banished him from the Garden of Eden to work the ground from which he had been taken.

The Expulsion from the Garden of Eden



EDICON 2018
Electronic Design Innovation Conference & Exhibition

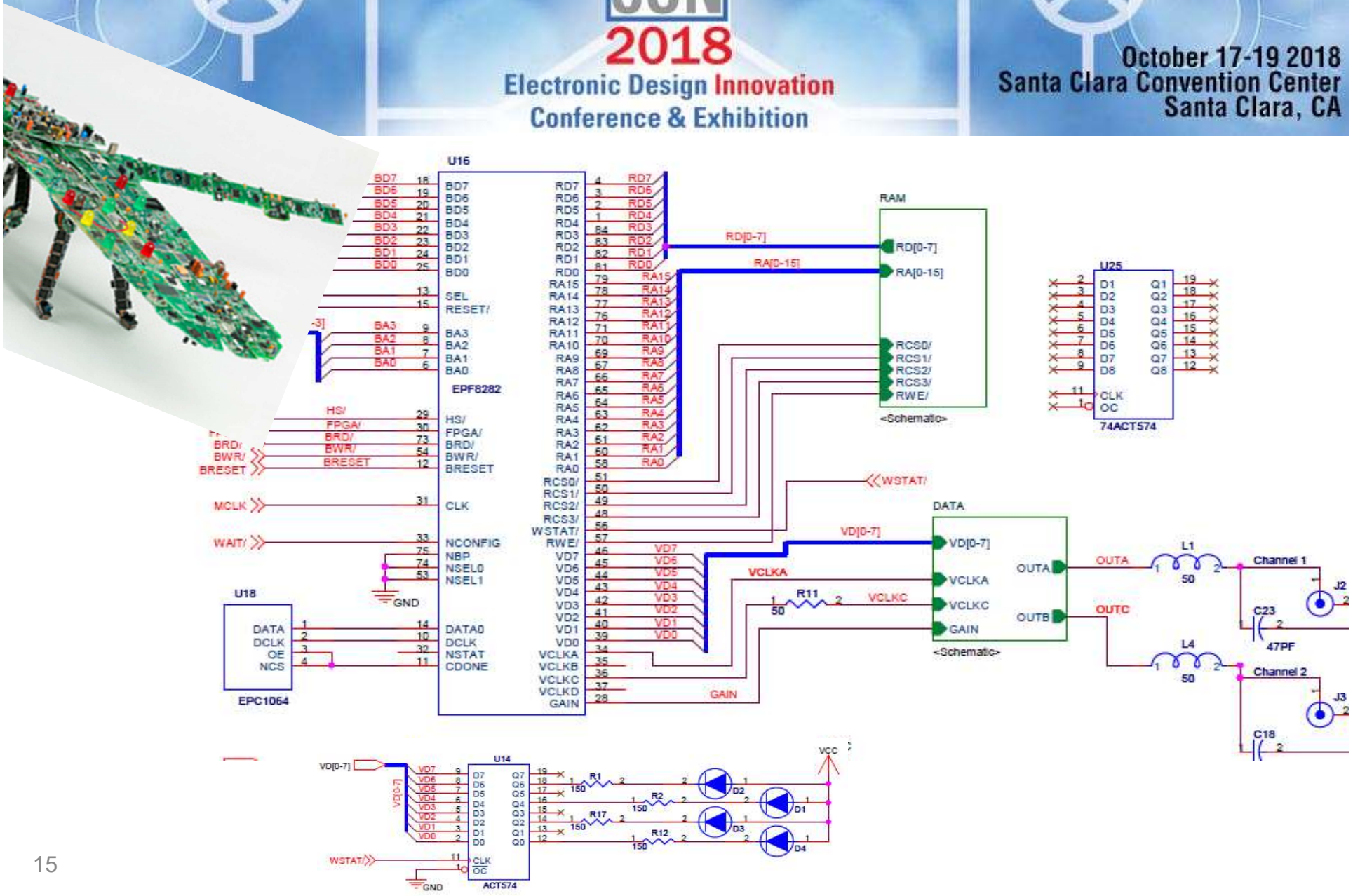
October 17-19 2018
Santa Clara Convention Center
Santa Clara, CA

Copper Snakes can Cure Hidden Snakes in your PCB

Our Premium Snake is The Return Current through the GND/PWR Planes of Copper

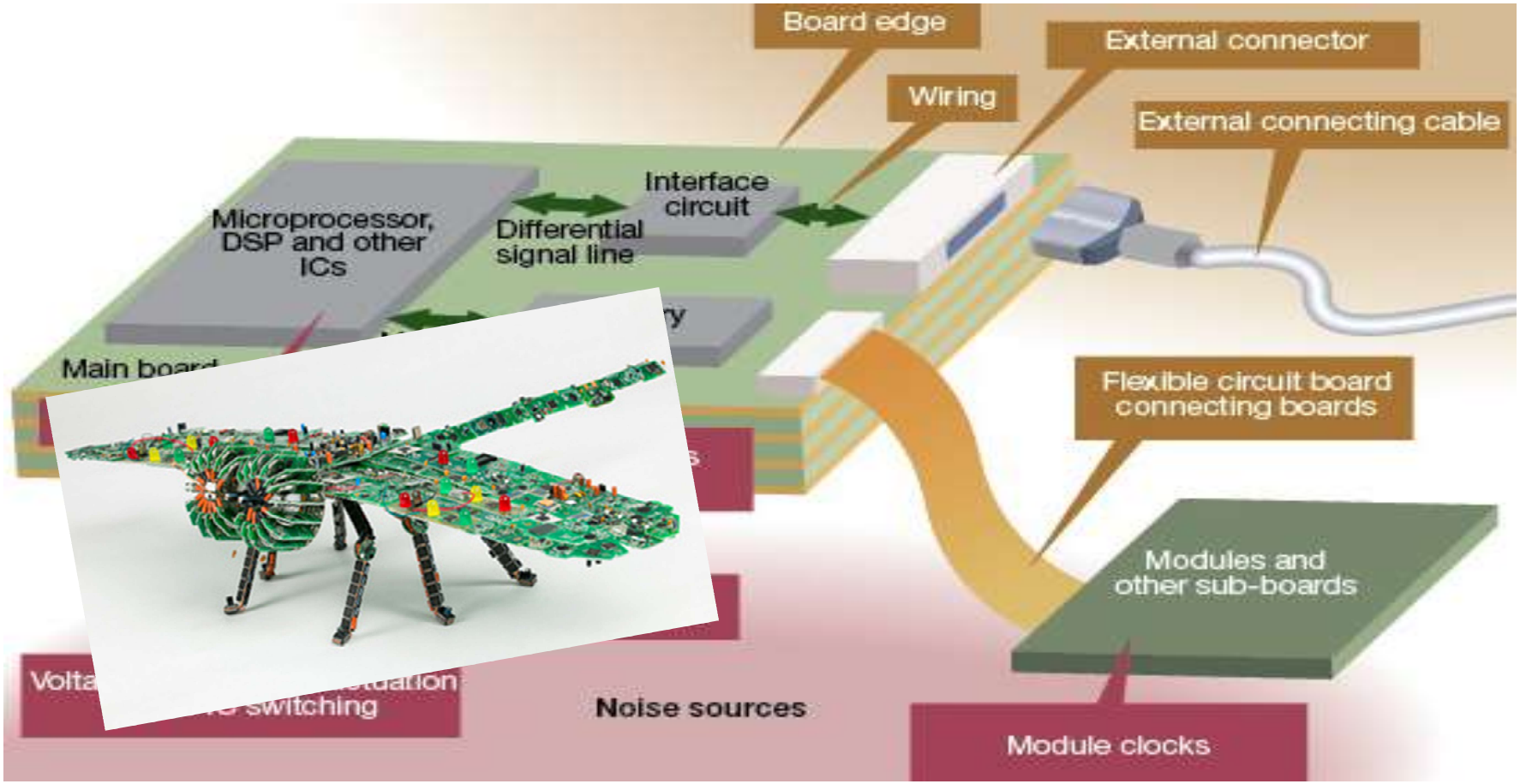
And the Parasitic Elements of the PCB Materials

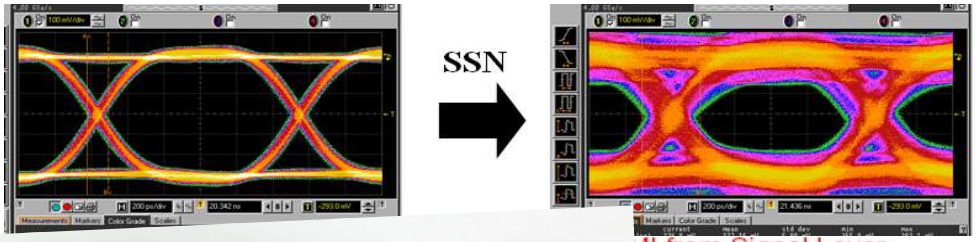
Design it
Control it


U16
EPF6282
RAM
<Schematic>
U25
74ACT574
U18
EPC1064
DATA
<Schematic>
U14
ACT574
RD[0-7]
RA[0-15]
WSTAT/
VD[0-7]
VCLKA
VCLKC
GAIN
R11
50
L1
L4
Channel 1
Channel 2
J2
J3
C23
47PF
C18
OUTA
OUTC
R1
R2
R17
R12
150
D1
D2
D3
D4
VCC
GND

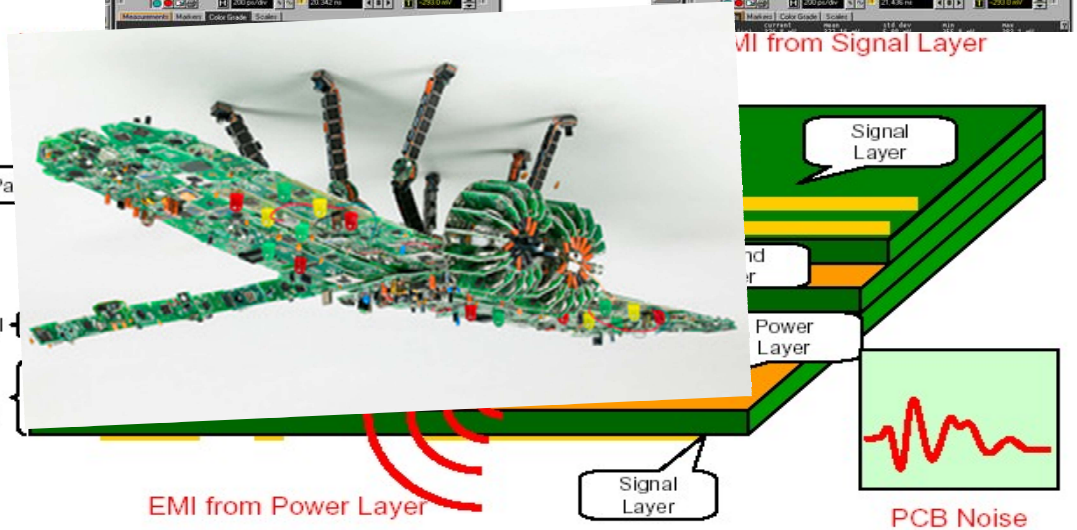
EDI CON 2018
Electronic Design Innovation Conference & Exhibition

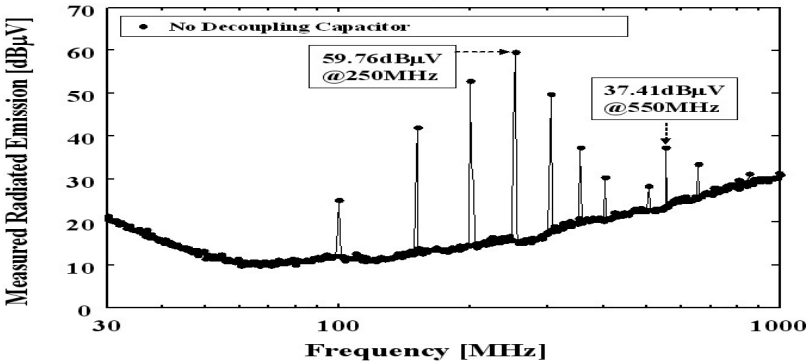
October 17-19 2018
Santa Clara Convention Center
Santa Clara, CA





Identify and Catch the Snakes





Snakes in the real PCB

The return current path is The hidden parts of the Signal Path

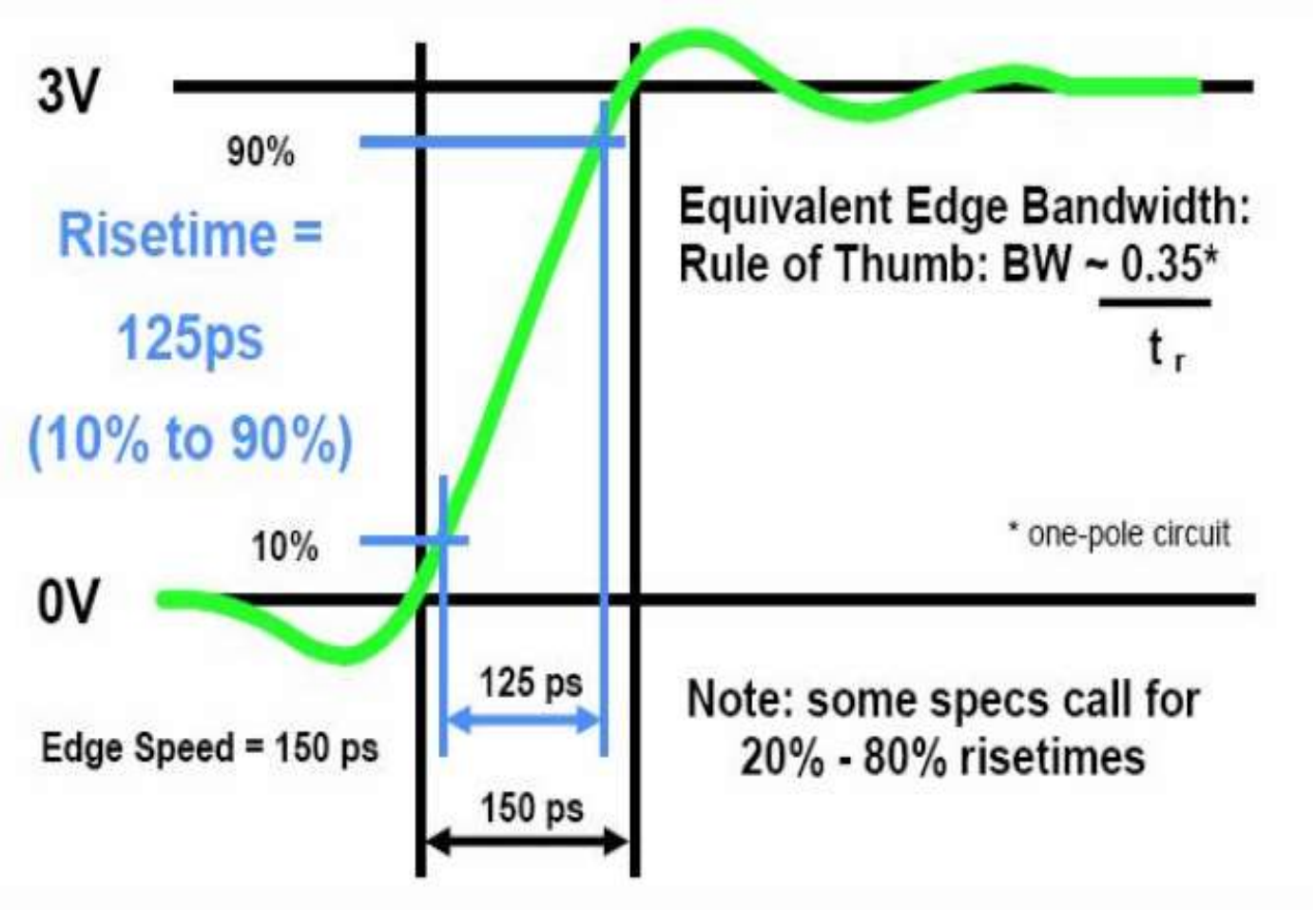
Materials:
Dielectric Constant & Loss Tangent of Basic Dielectric Material
Resistance & Inductance of Copper Conductors

Parasitic Capacitance between Conductors and Planes

Mutual Inductance >>>>>> Crosstalk by Coupling
Mutual Capacitance >>>>>> Crosstalk by Coupling

Switching Signals radiates Electromagnetic Fields

The AC of the DC



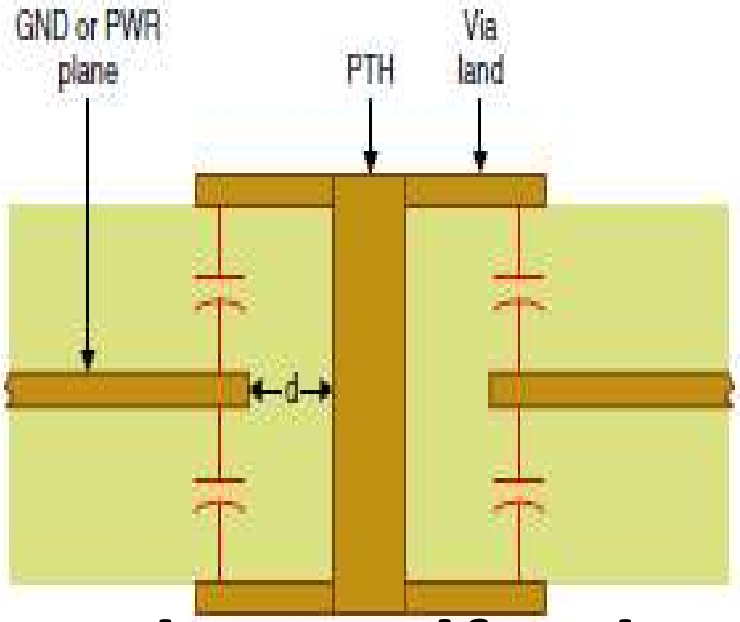
The Switching Time

During Switching time [tR, tF]

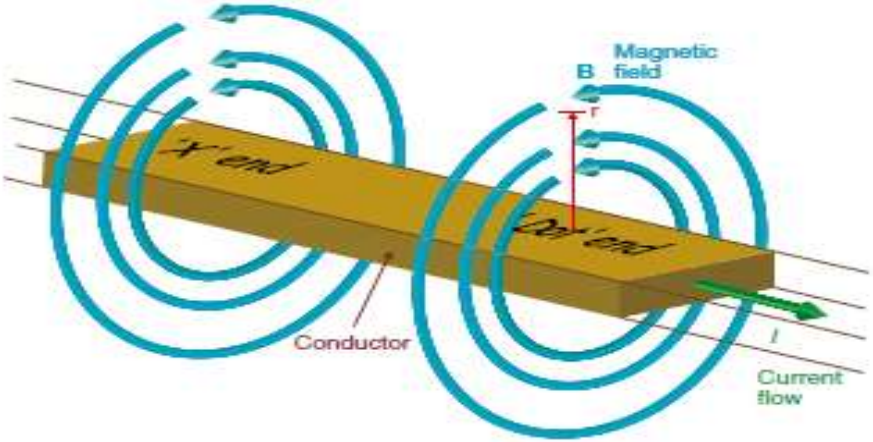
dV/dt	Causes	Electric Field	Capacitance
dI/dt	Causes	Magnetic Field	Inductance

The Signal has the potential to be an Electromagnetic Field propagating between the Conductor and the Reference Planes

Electric Fields and Self Inductance during Switching Time [Rise Time or Fall Time]



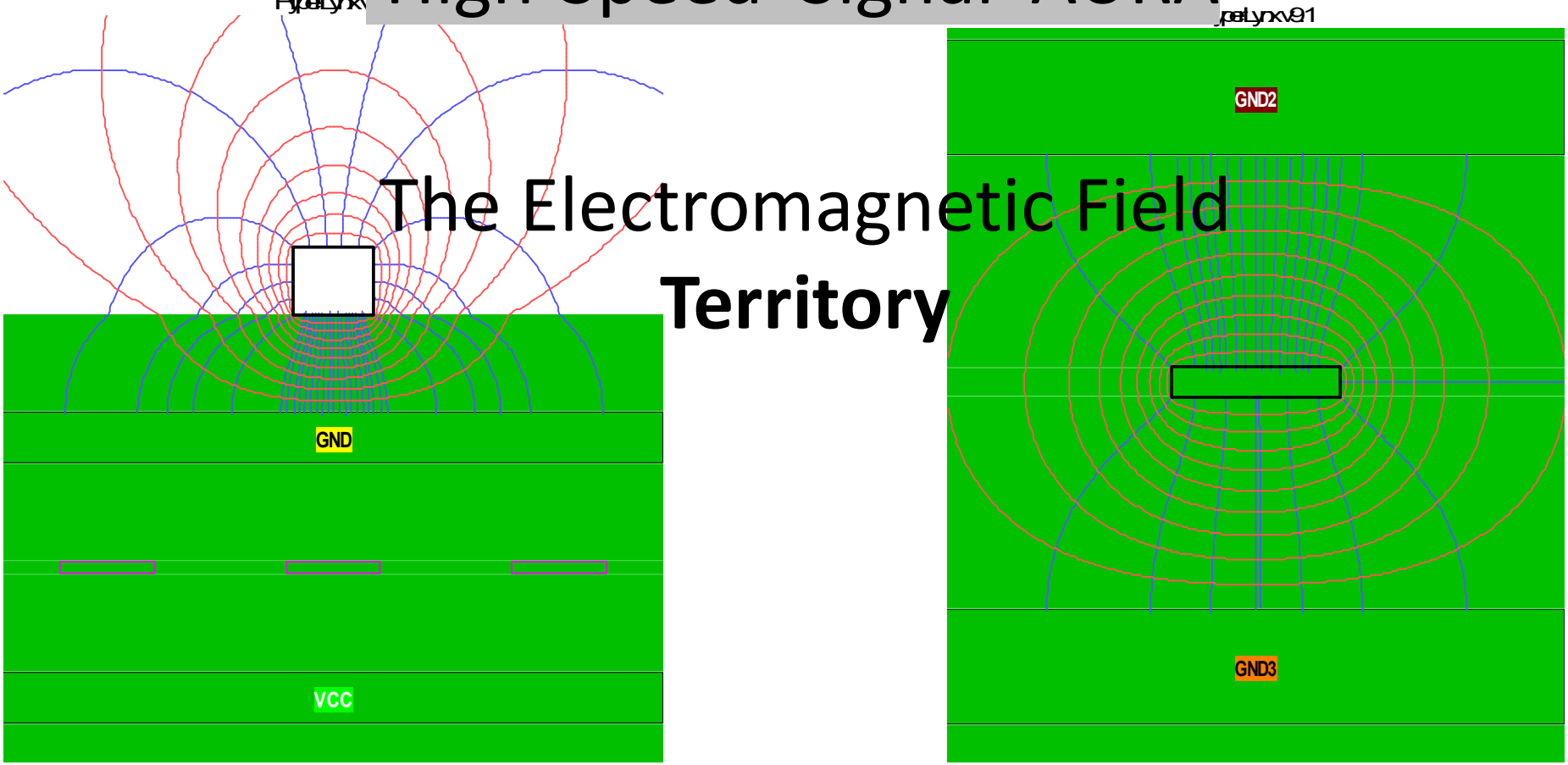
Lself ~ length / ln w

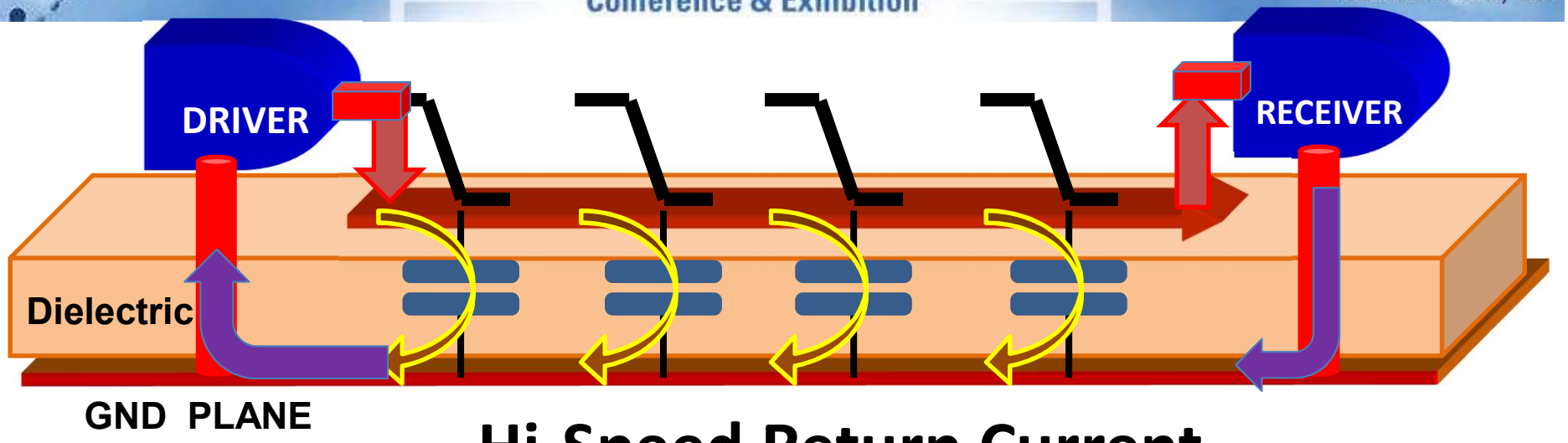


Reduce Self Inductance of Conductors by minimizing length and/or by maximizing width

High-Speed Signal AURA

The Electromagnetic Field **Territory**





Hi-Speed Return Current

For F>100 KHz, the Signal Returns through lowest Inductance (Loop Area) and highest Capacitance

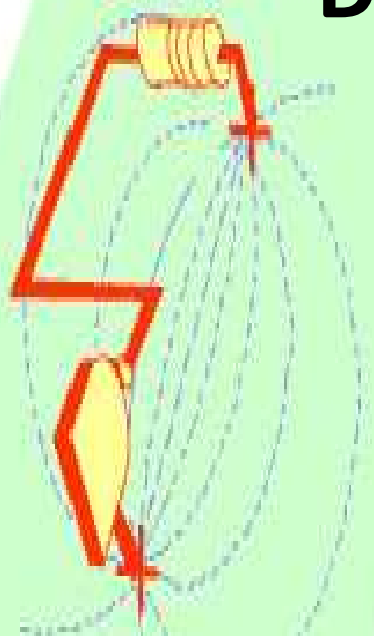
The PCB layout sets the Return Current Path

Shalom-Shlomi-Zigdon@iTech-iCollege.com

Return current path

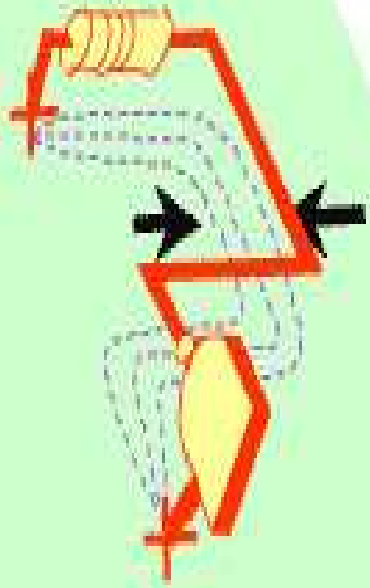
=Shortest possible connection

DC



Less Resistance

AC



Less Impedance

James Clerk Maxwell

Maxwell's Equations

1. **Guass's Law** – The greater the charge, the greater the electric field
2. **Guass's Law for magnetism** - Magnetic flux is zero through a closed surface
3. **Faraday's Law** – An electric field is produced by a changing magnetic field
4. **Ampere-Maxwell Law** - A magnetic field is produced by a changing electric field (moving charge)

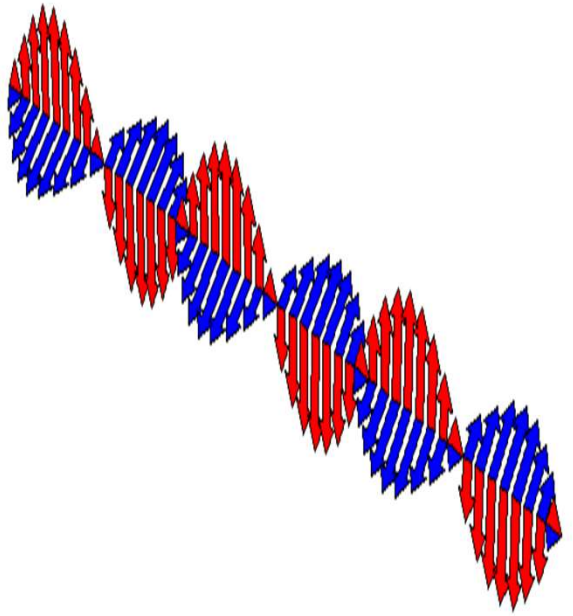
(1) $\nabla \cdot E = \frac{\rho}{\epsilon_0}$

(2) $\nabla \times E = -\frac{\partial B}{\partial t}$

(3) $\nabla \cdot B = 0$

(4) $c^2 \nabla \times B = \frac{\partial E}{\partial t} + \frac{j}{\epsilon_0}$

[1] [2] [1] [0] [2]



[0] An electric current (j) causes circulation of B ($\nabla \times B$)

[1] A *changing* magnetic field ($\partial B/\partial t$) causes circulation of E ($\nabla \times E$)

[2] A *changing* electric field ($\partial E/\partial t$) causes circulation of B ($\nabla \times B$)

The Fourier Transform

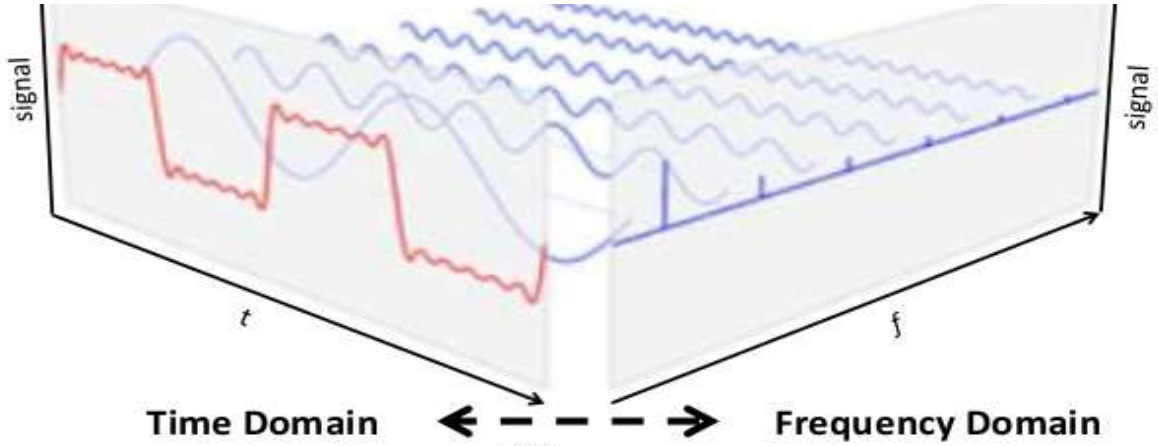
The Fourier Transform .com

$$\mathcal{F}\{g(t)\} = G(f) = \int_{-\infty}^{\infty} g(t)e^{-i2\pi ft}\,dt$$

$$\mathcal{F}^{-1}\{G(f)\} = g(t) = \int_{-\infty}^{\infty} G(f)e^{i2\pi ft}\,df$$

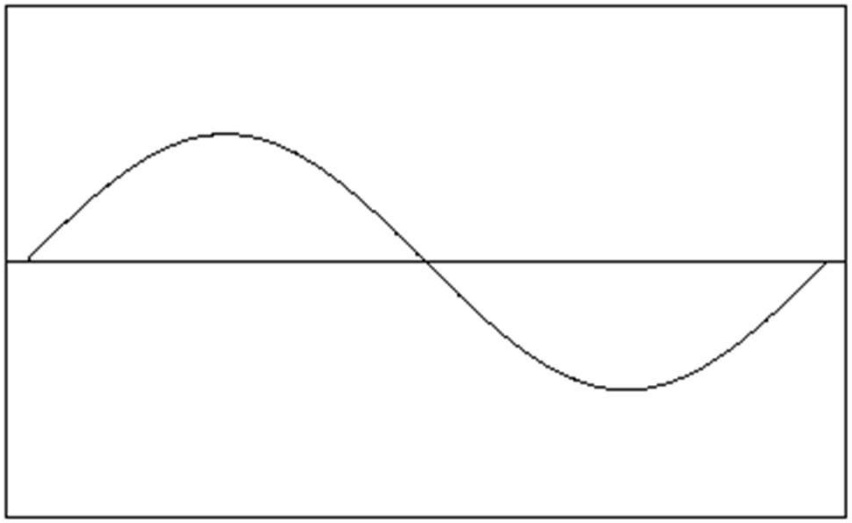
Shalom-Shlomi-Zigdon@iTech-iCollege.com

Signal on Time Domain
is
a sum of infinite Analog Waves
on Frequency Domain

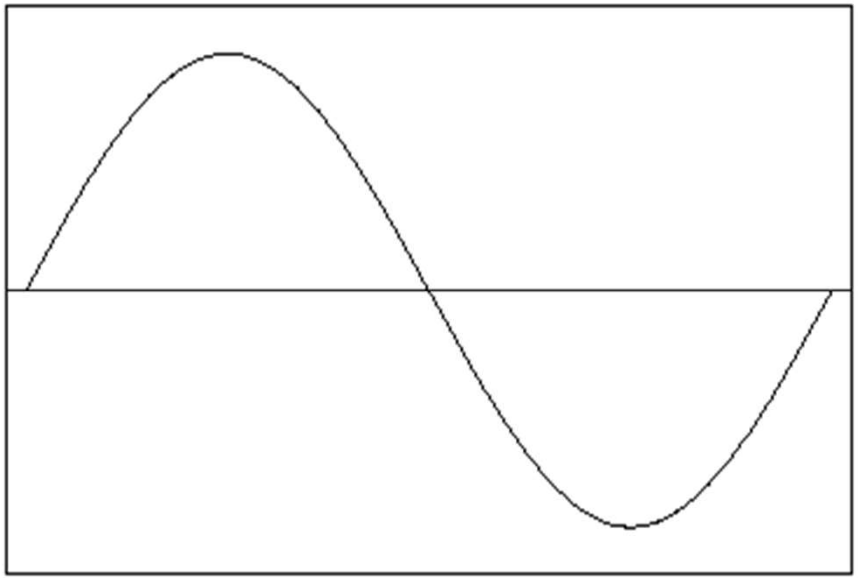


$$\hat{f}(\xi) = \int_{-\infty}^{\infty} f(x)\, e^{-2\pi i \xi x}\, dx$$

Fourier composition of a sawtooth wave

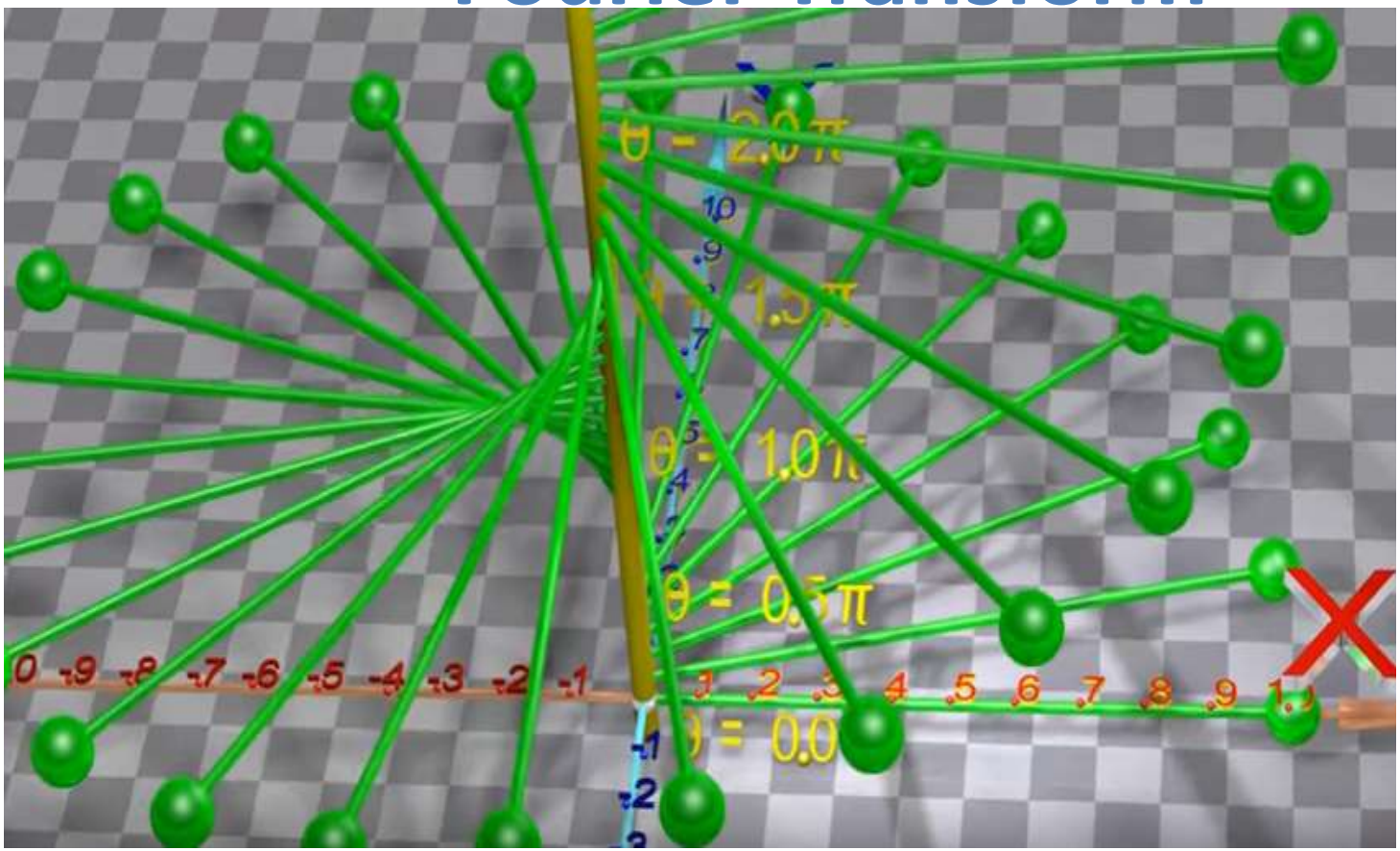


Fourier composition of a square wave




1
0.8
0.6
0.4
0.2
1

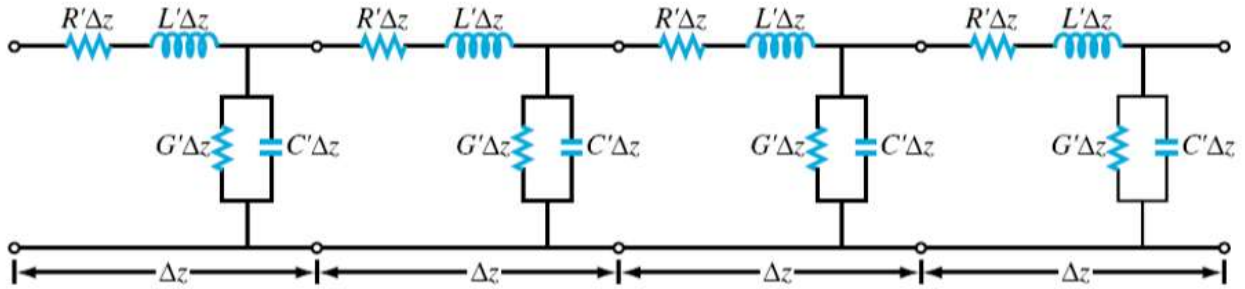
Fourier Transform



VIDEO

(a) Parallel-wire representation

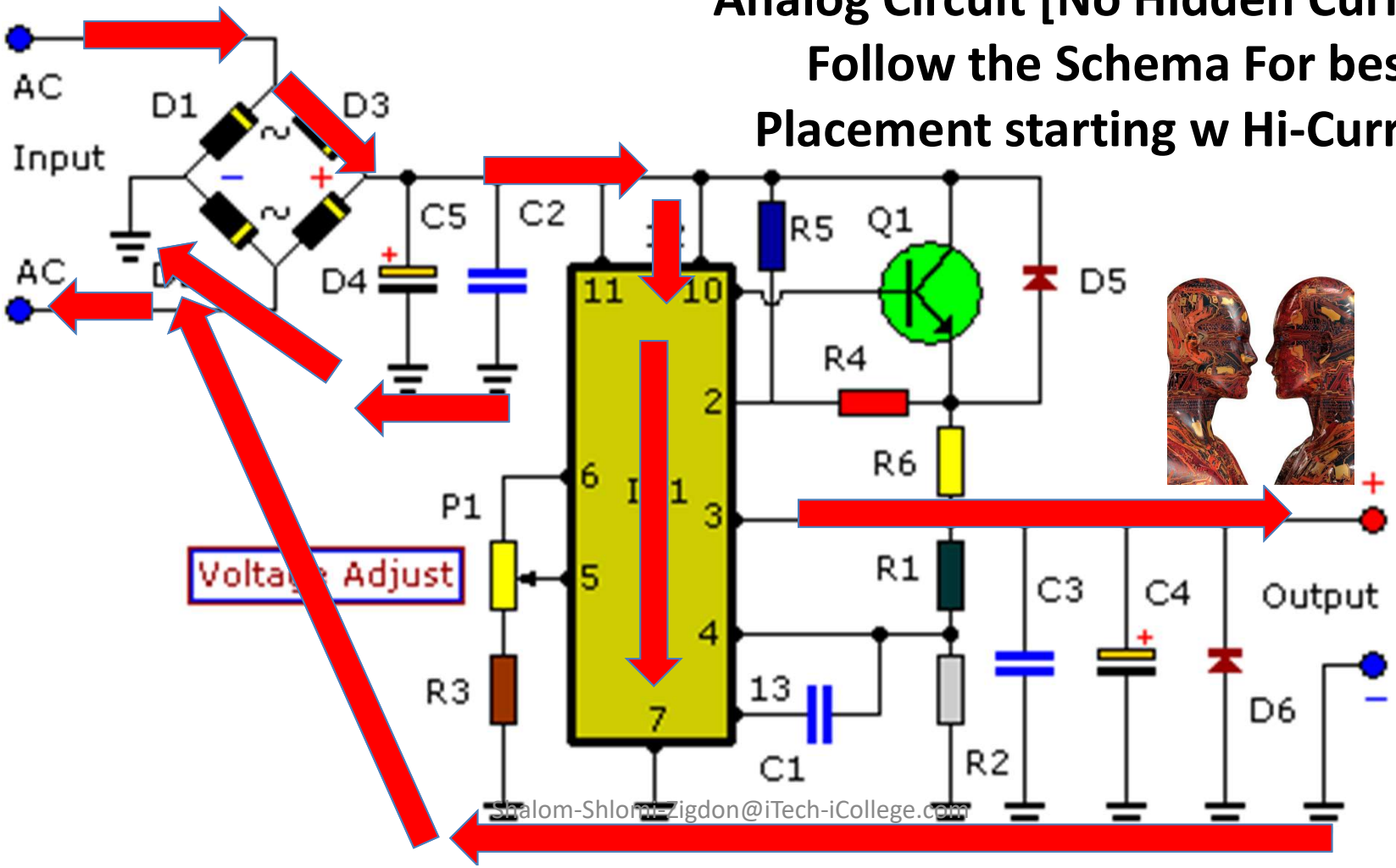
(b) Differential sections each Δz long



(c) Each section is represented by an equivalent circuit

PLACEMENT RULES

Analog Circuit [No Hidden Currents]
Follow the Schema For best Placement starting w Hi-Current

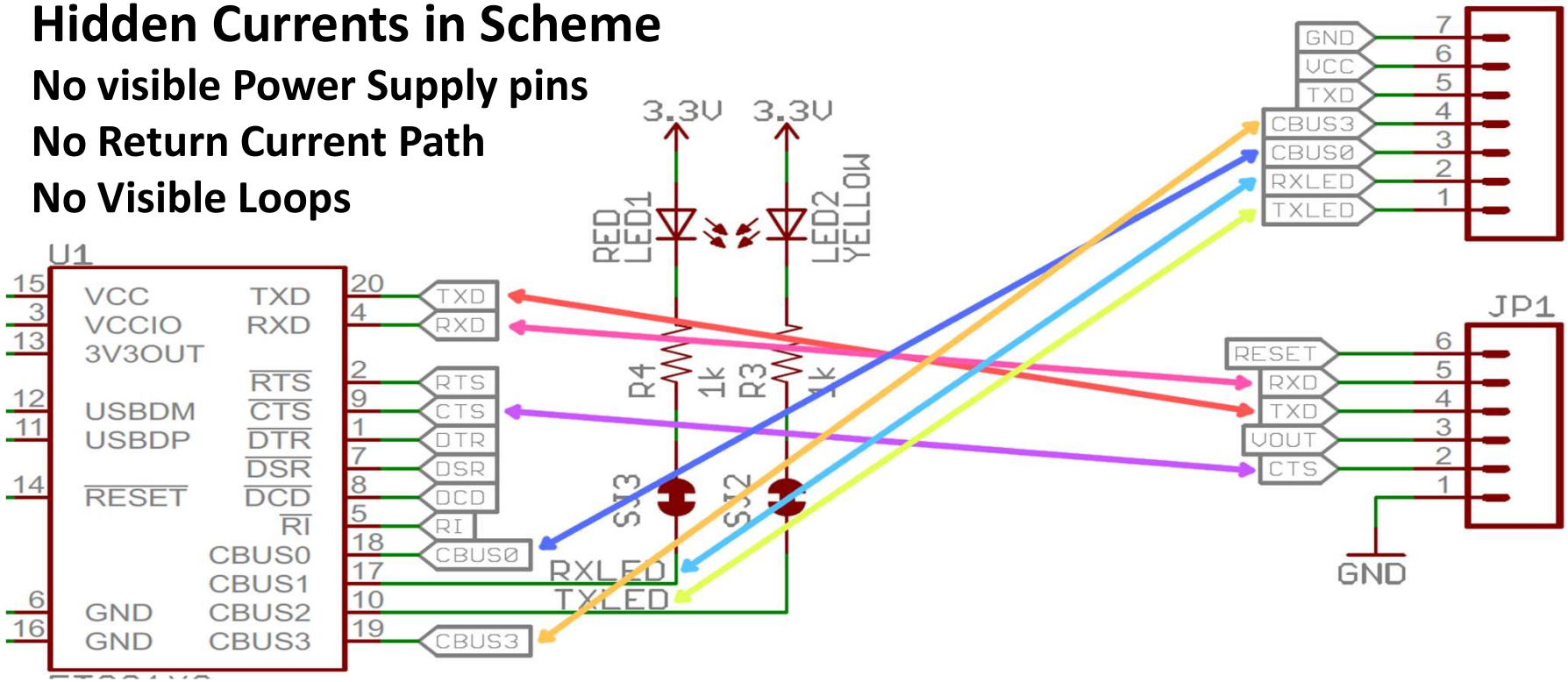


Hidden Currents in Scheme

No visible Power Supply pins

No Return Current Path

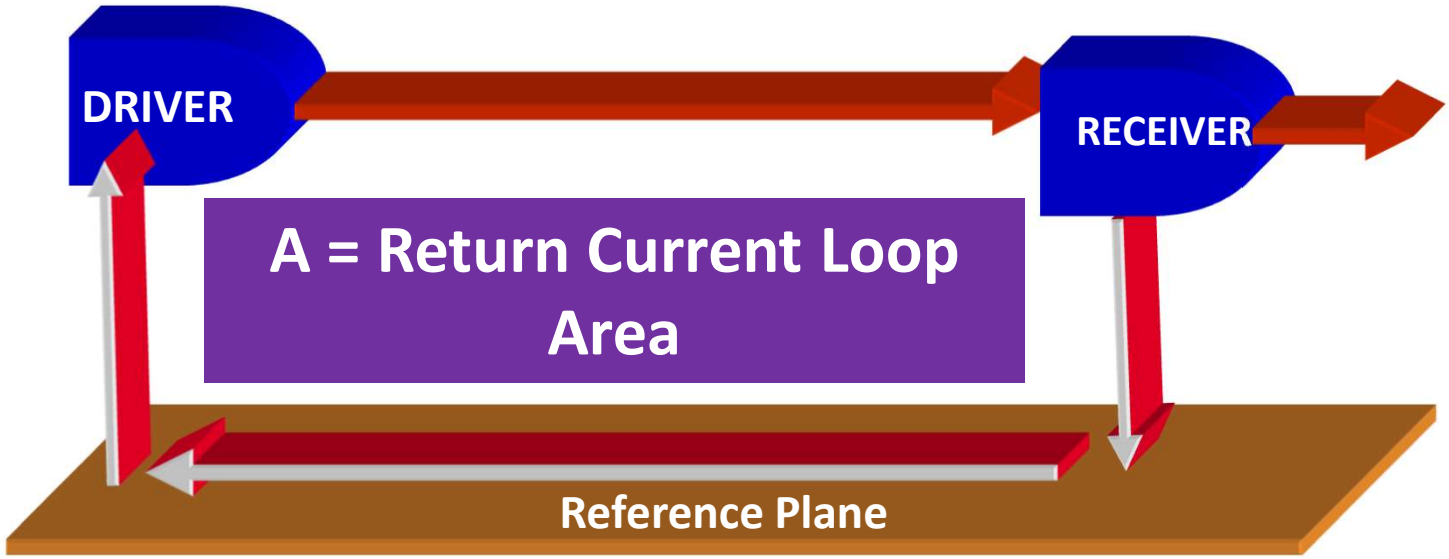
No Visible Loops



As a result, the R&D Engineer, fails to communicate essential information to the PCB Designer

Fact: current flows in a loop

There must be a return current

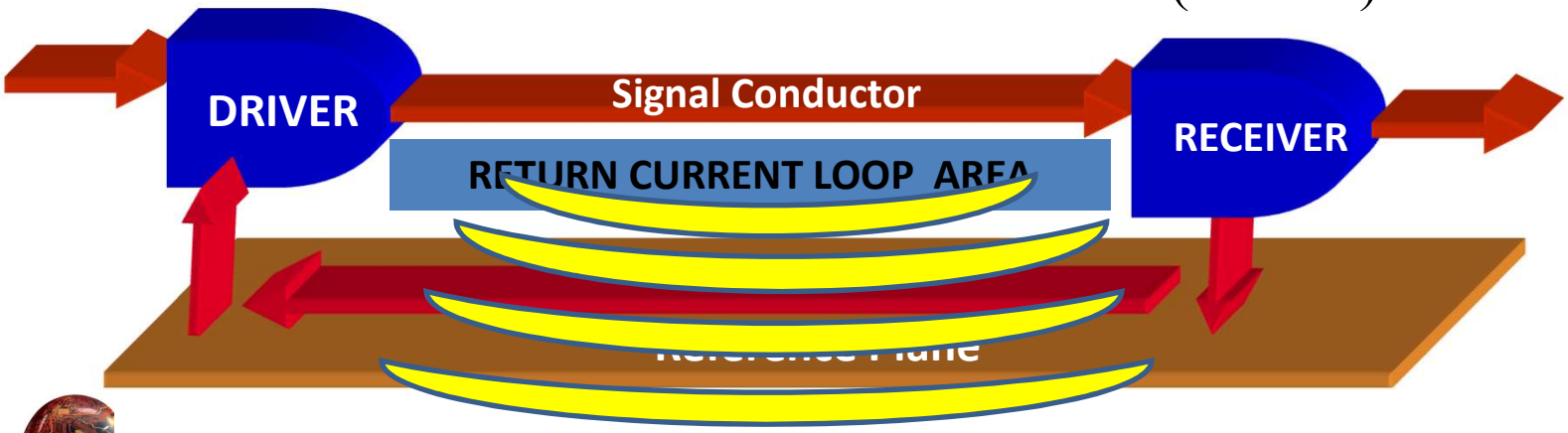


Today, in Digital Design, any "Line" in Schema is actually a Loop in the PCB/System behaving as an "Unwanted Antenna"

Shalom-Shlomi-Zigdon@iTech-iCollege.com

Any loop Generates Radiation – "Antenna"

$$E_{(V/m)} = 1.3 f^2_{(MHz)} * A_{(cm^2)} * \frac{I_{(amps)}}{R_{(meters)}}$$



Minimize the dielectric thickness between

Signal Layers and Power Planes

Terminations – Impedance Matching

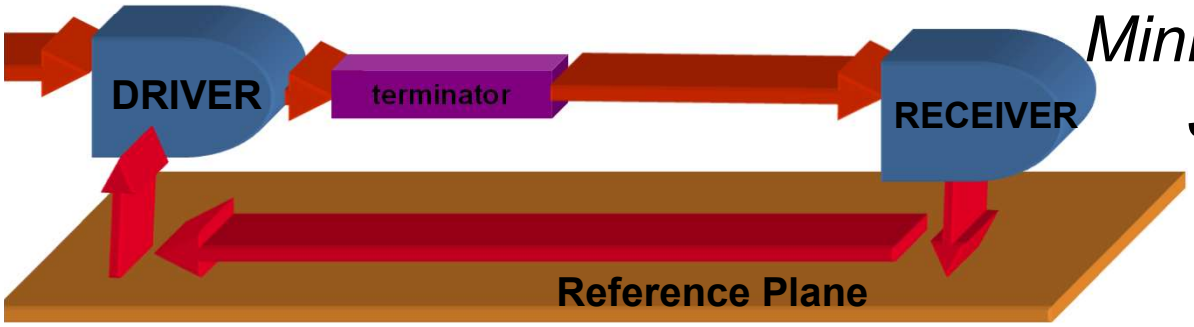
Parallel Termination is easier

Prefer Series Termination

Minimize Current

Minimize EMI Radiation

Smaller Antenna



from Ohm/Kirchhoff to Maxwell ?

When Conductor Length is greater than

T.E.L/10

[not TEL/2, not TEL/4, not TEL/6]

T.E.L = Transmission Electrical Length

= the Distance a Signal E.M. Field [not the Current] propagates during its Switching Time

FR4 D.K=4 6” in 1 nSecond

So, for Tr= 1 nS

keep your Conductors 0.6” w/o Termination

Estimate the "Hidden Current" of the Hi-Speed Signals

The Six options:

Microstripe closed to GND Plane

- Low-to-High Transition,
- High -to- Low Transition

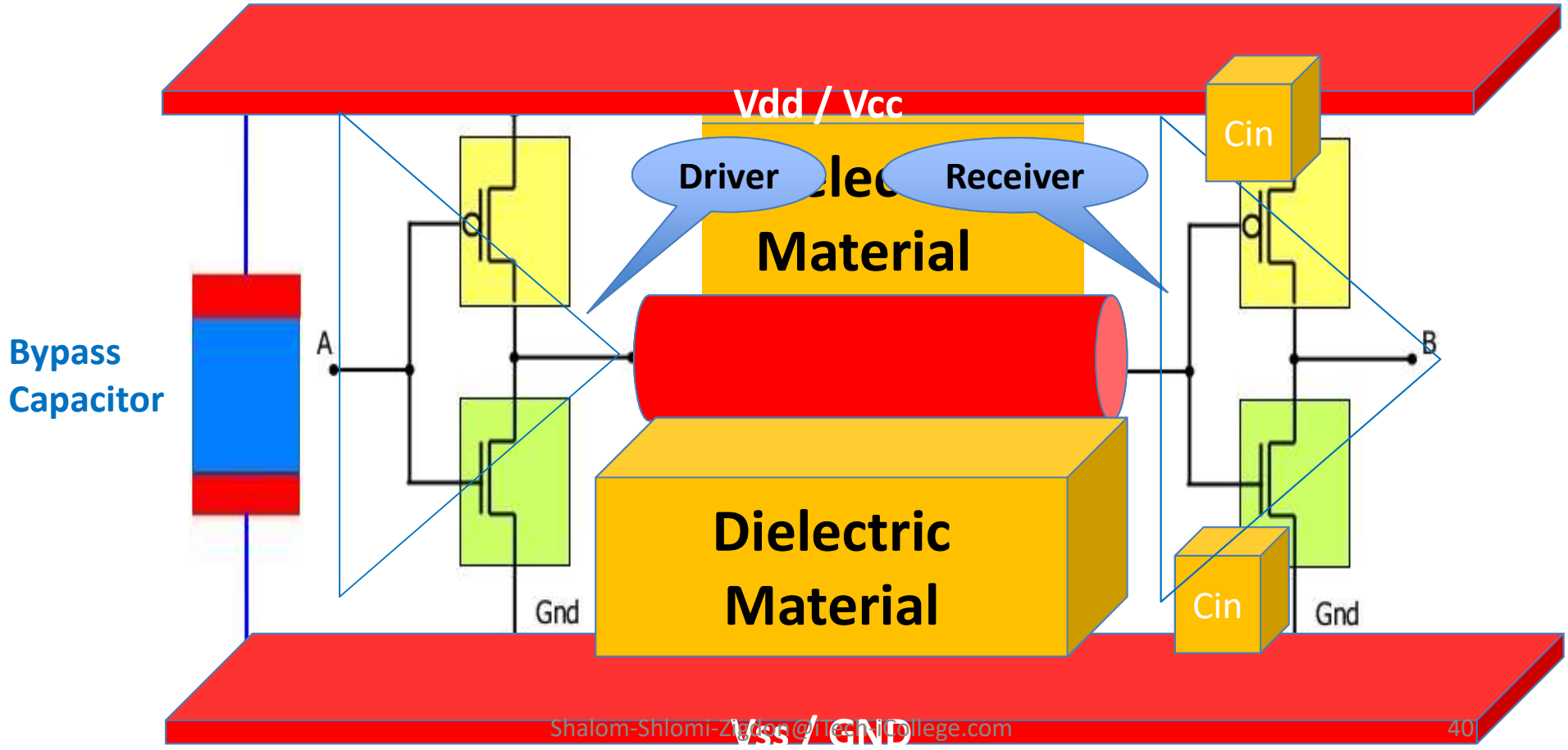
Microstripe closed to VCC Plane

- Low-to-High Transition,
- High -to- Low Transition

Stripline between Power Planes

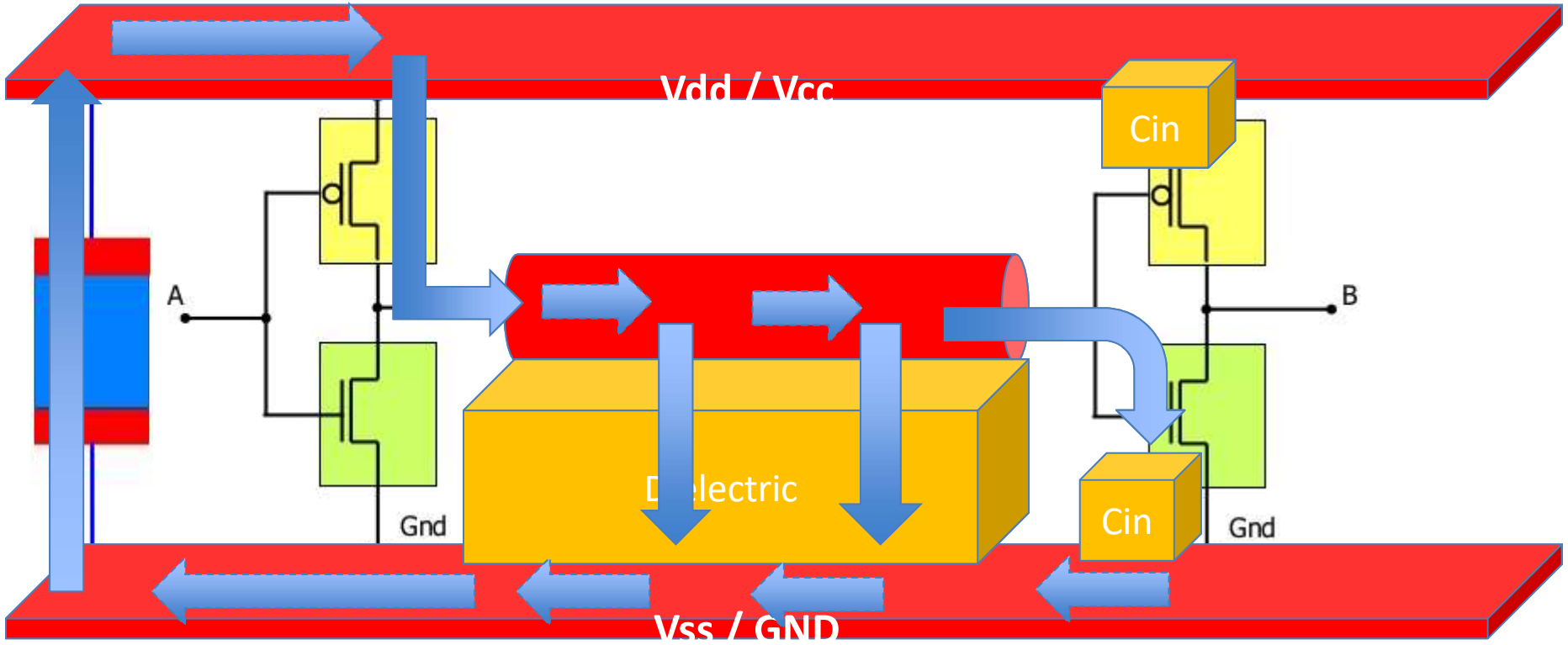
- Low-to-High Transition,
- High -to- Low Transition

The hidden parts of the Signal Path



DIGITAL CIRCUIT CURRENT PATH

Trace Adjacent to a Ground Plane (Microstrip) - Low-to-High Transition

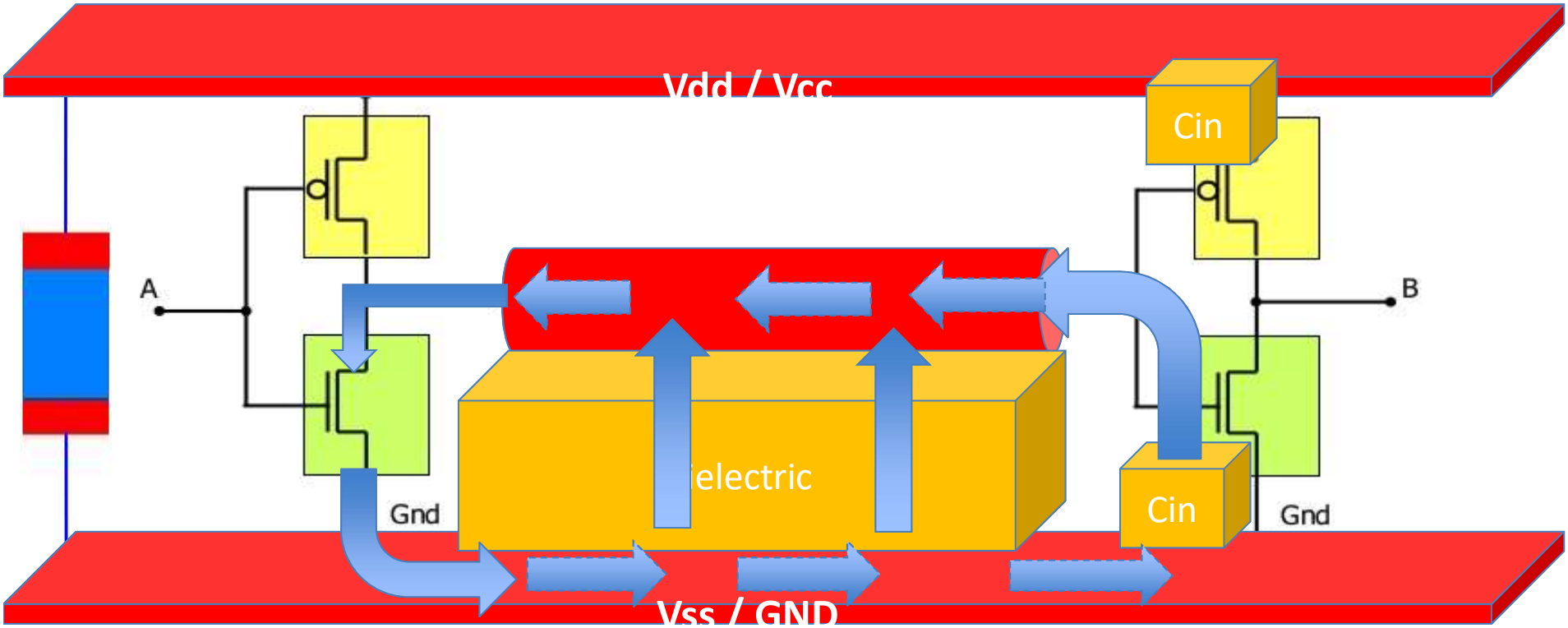


Current Source: **Bypass/Decoupling Capacitor**

Return Current Path: **GND / Vss Plane**

DIGITAL CIRCUIT CURRENT PATH

Trace Adjacent to a Ground Plane (Microstrip) High -to- Low Transition

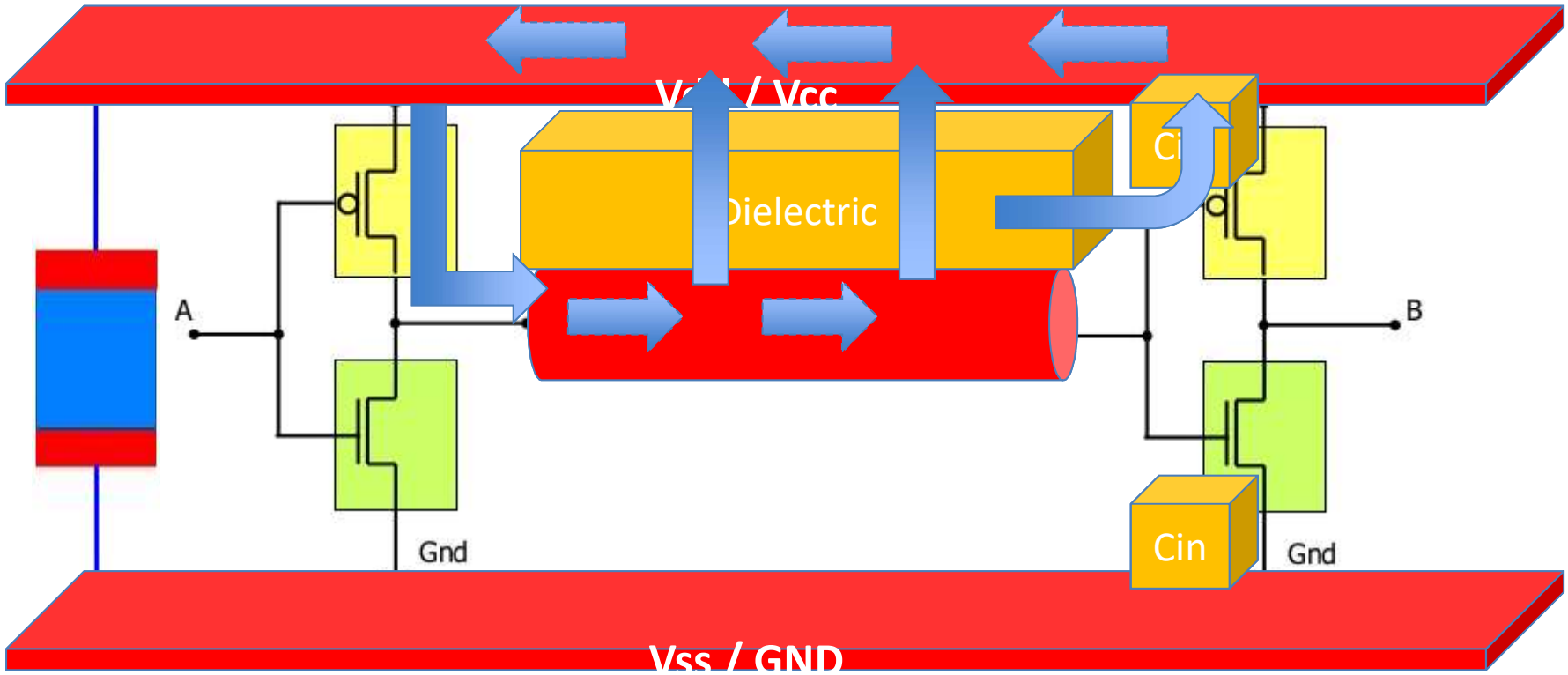


Current Source: **Parasitic Capacitance**

Return Current Path: **GND / Vss Plane**

DIGITAL CIRCUIT CURRENT PATH

Trace Adjacent to a Power Plane (Microstrip) Low-to-High Transition

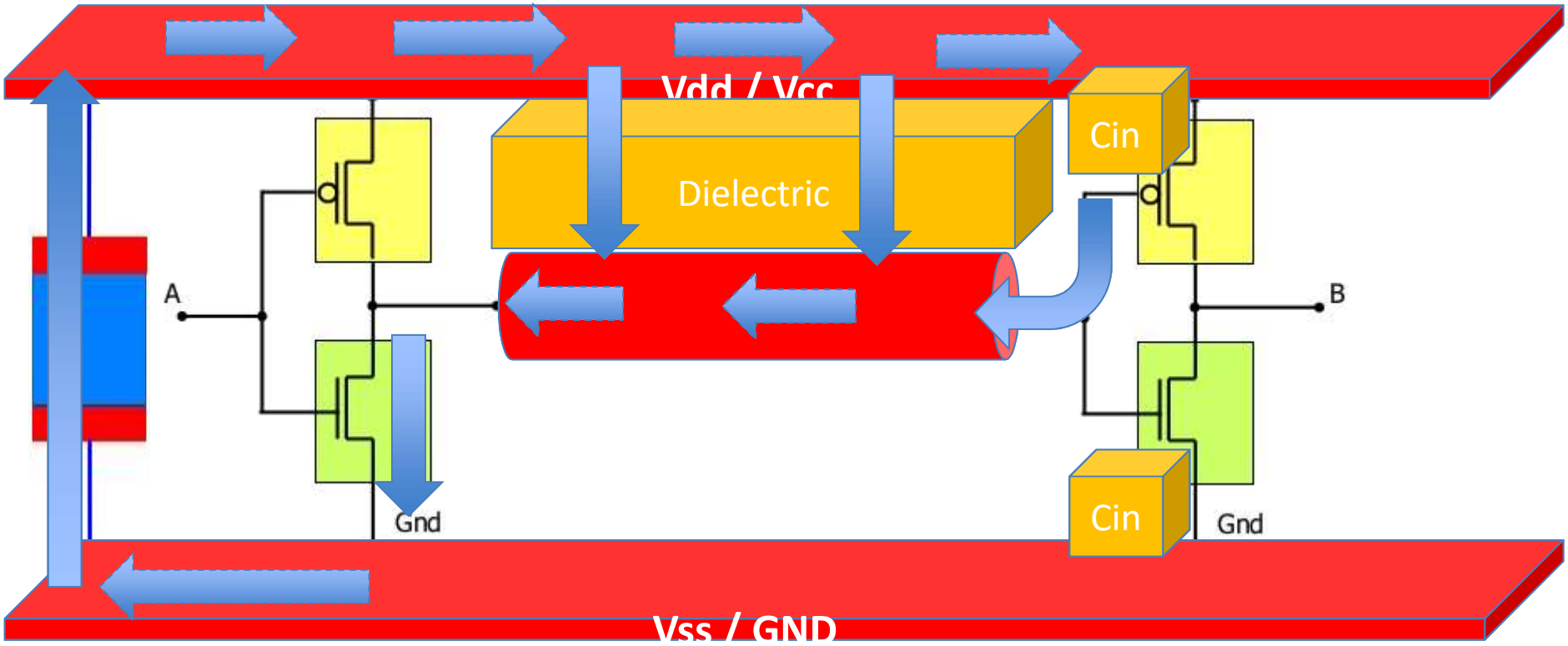


Current Source: **Parasitic Capacitance**

Return Current Path: **Power/Vcc/Vdd Plane**

DIGITAL CIRCUIT CURRENT PATH

Trace Adjacent to a **Power Plane** (Microstrip) **High -to- Low Transition**

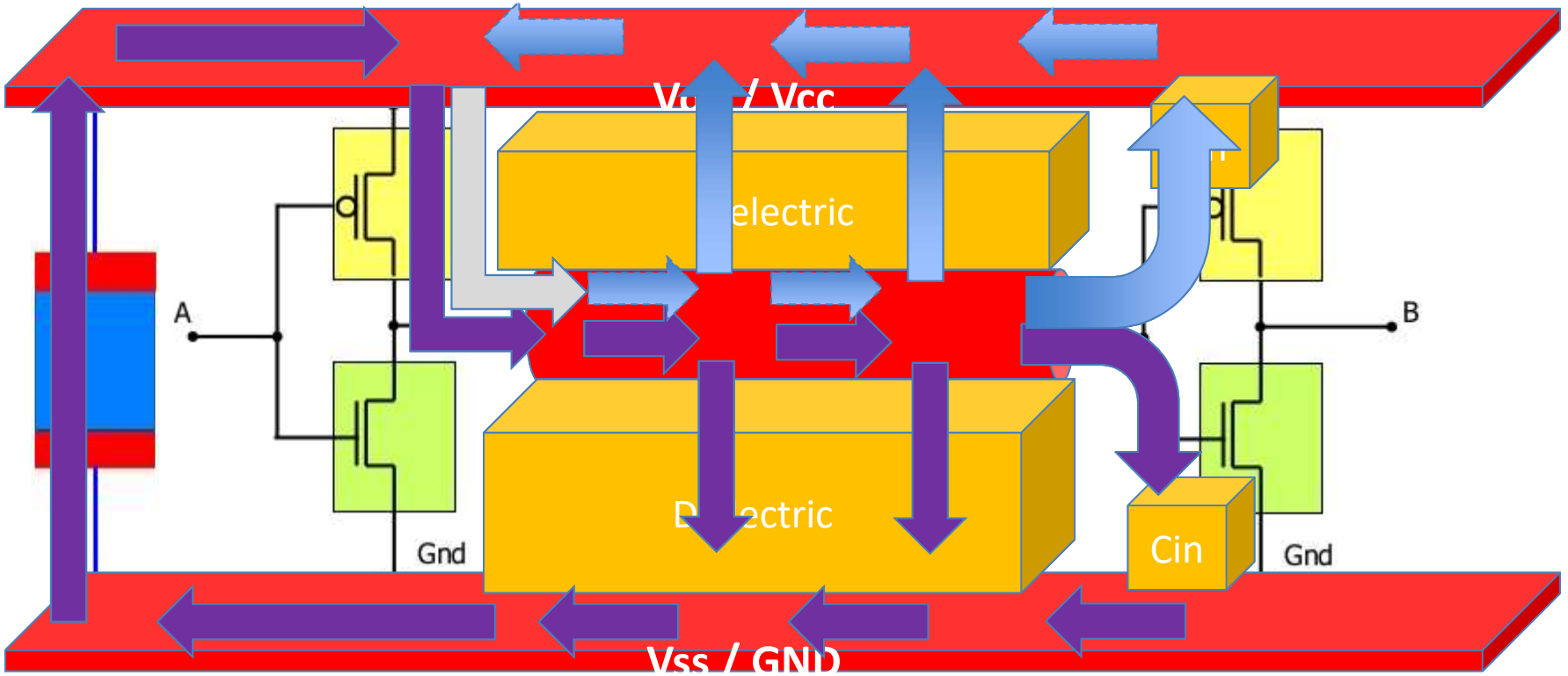


Current Source: **Bypass/Decoupling Capacitor**

Return Current Path: **Power/Vcc/Vdd Plane**

DIGITAL CIRCUIT CURRENT PATH

Trace **Between a Power & Ground** Planes (Stripline) **Low-to-High Transition**

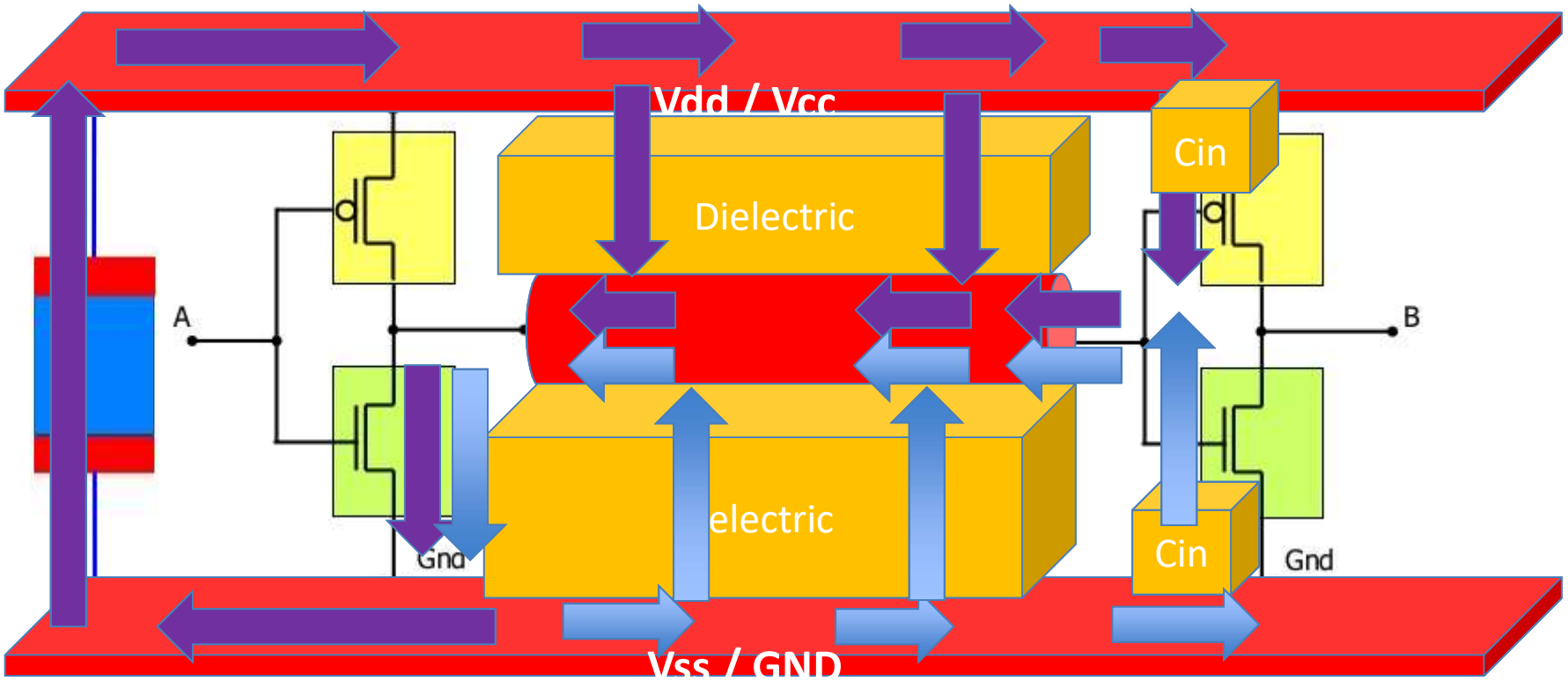


Current Source: **Bypass/Decoupling Capacitor & Parasitic Capacitance**

Return Current Path: **Power/Vcc/Vdd Plane & GND / Vss Plane**

DIGITAL CIRCUIT CURRENT PATH

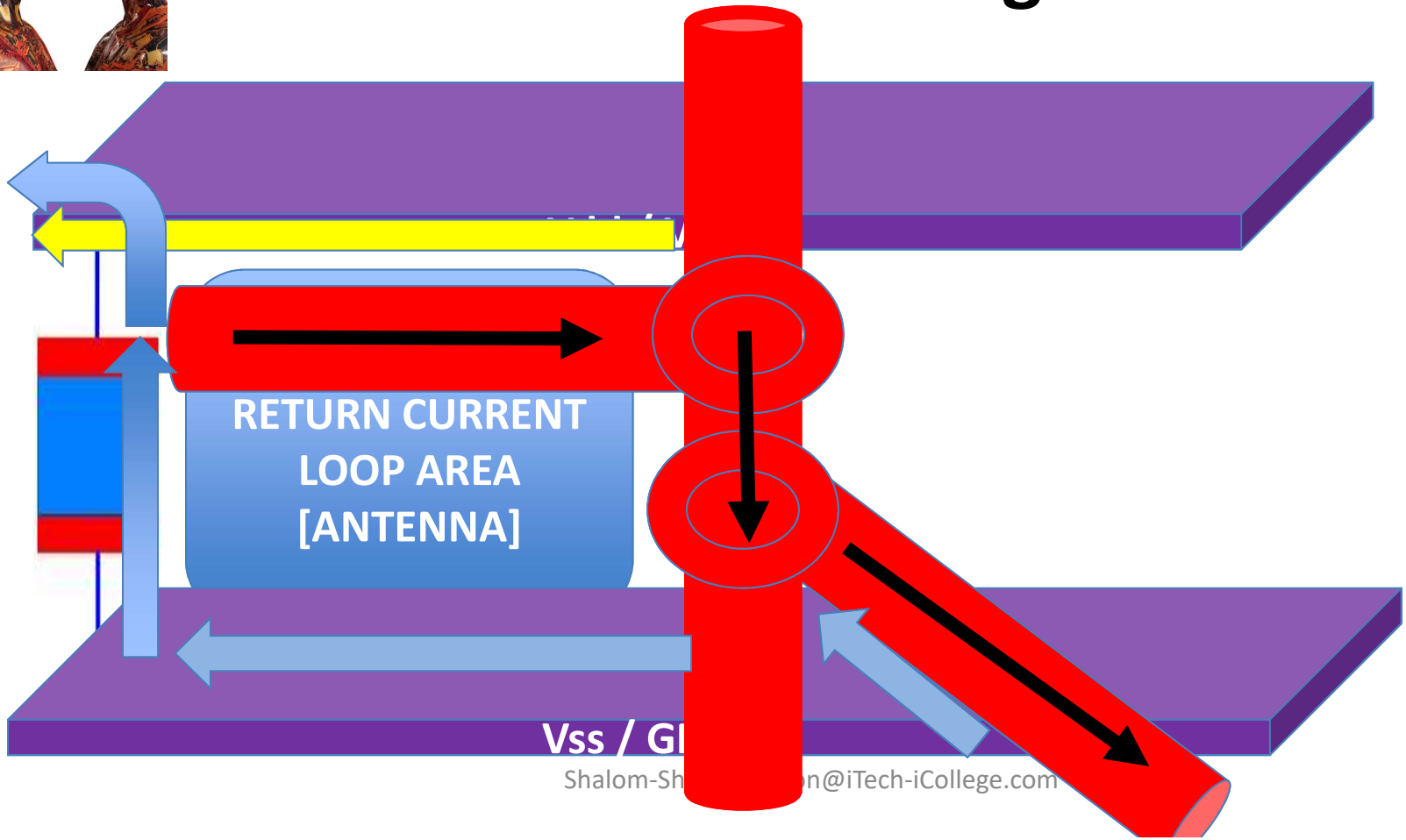
Trace **Between a Power & Ground** Planes (Stripline) **High-to-Low Transition**



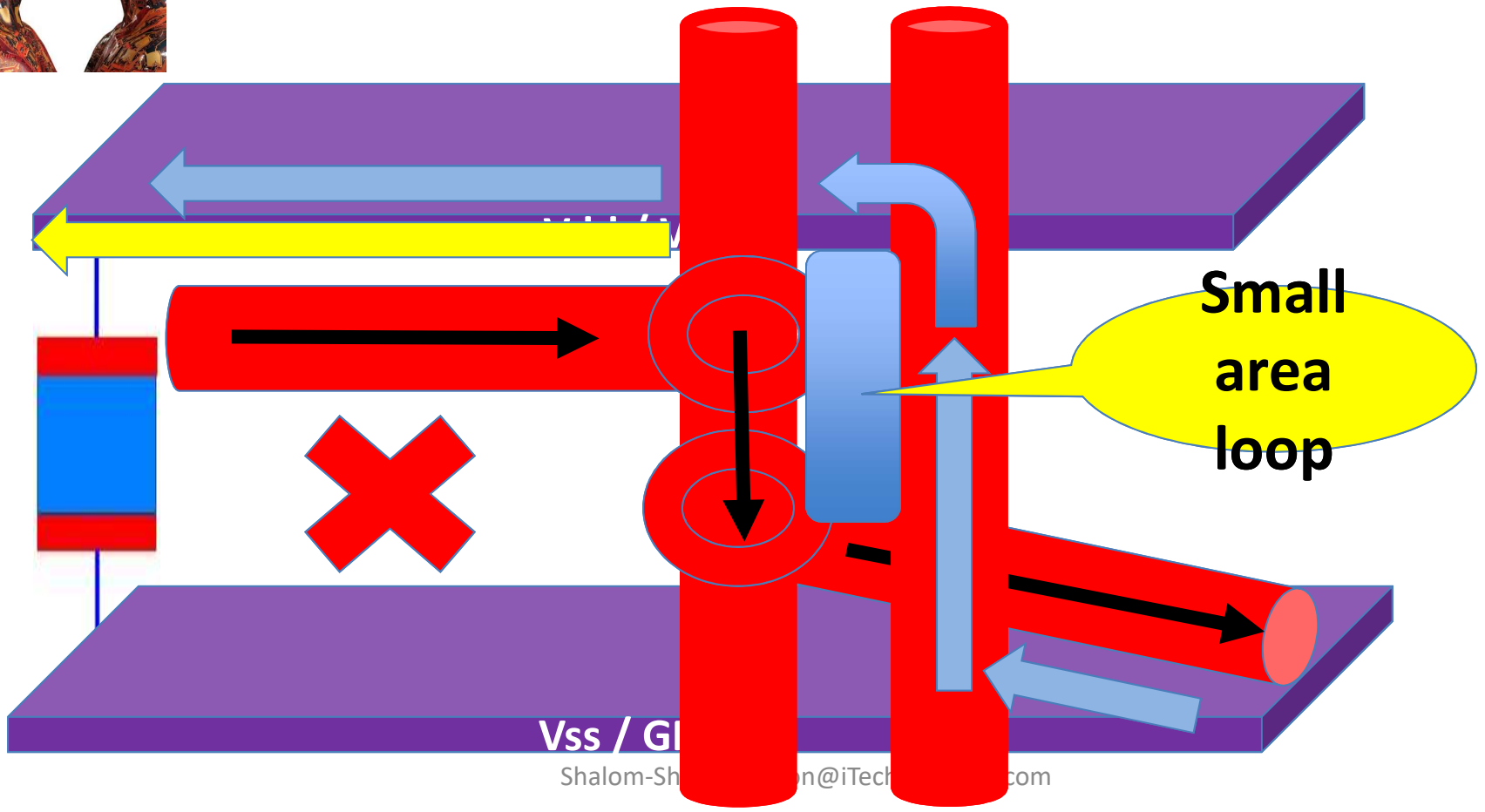
Current Source: **Bypass/Decoupling Capacitor & Parasitic Capacitance**

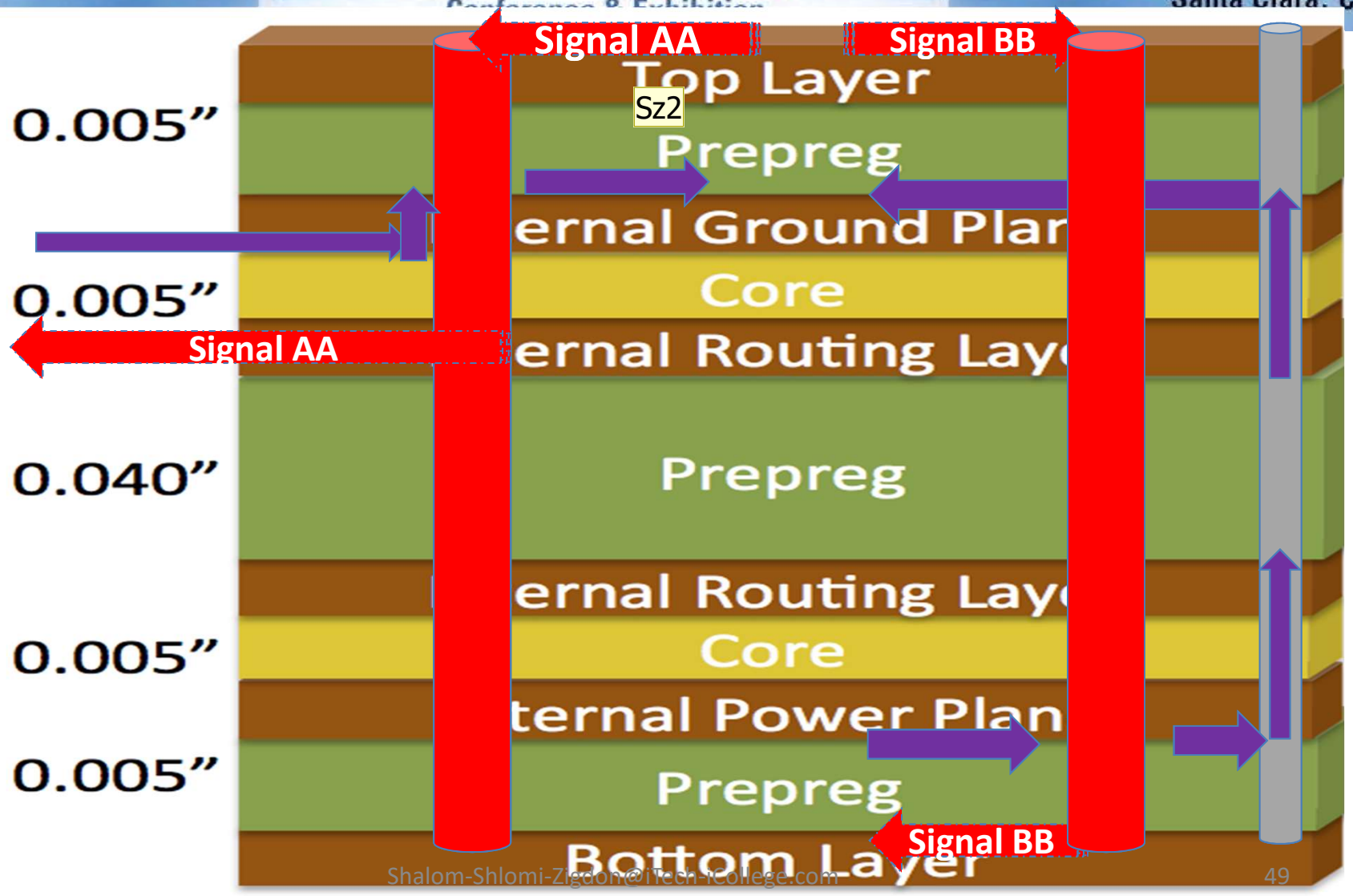
Return Current Path: **Power/Vcc/Vdd Plane & GND / Vss Plane**

Vertical & Horizontal Routing
Dont Rout the same Signal in the Cage



Add Stitching Via

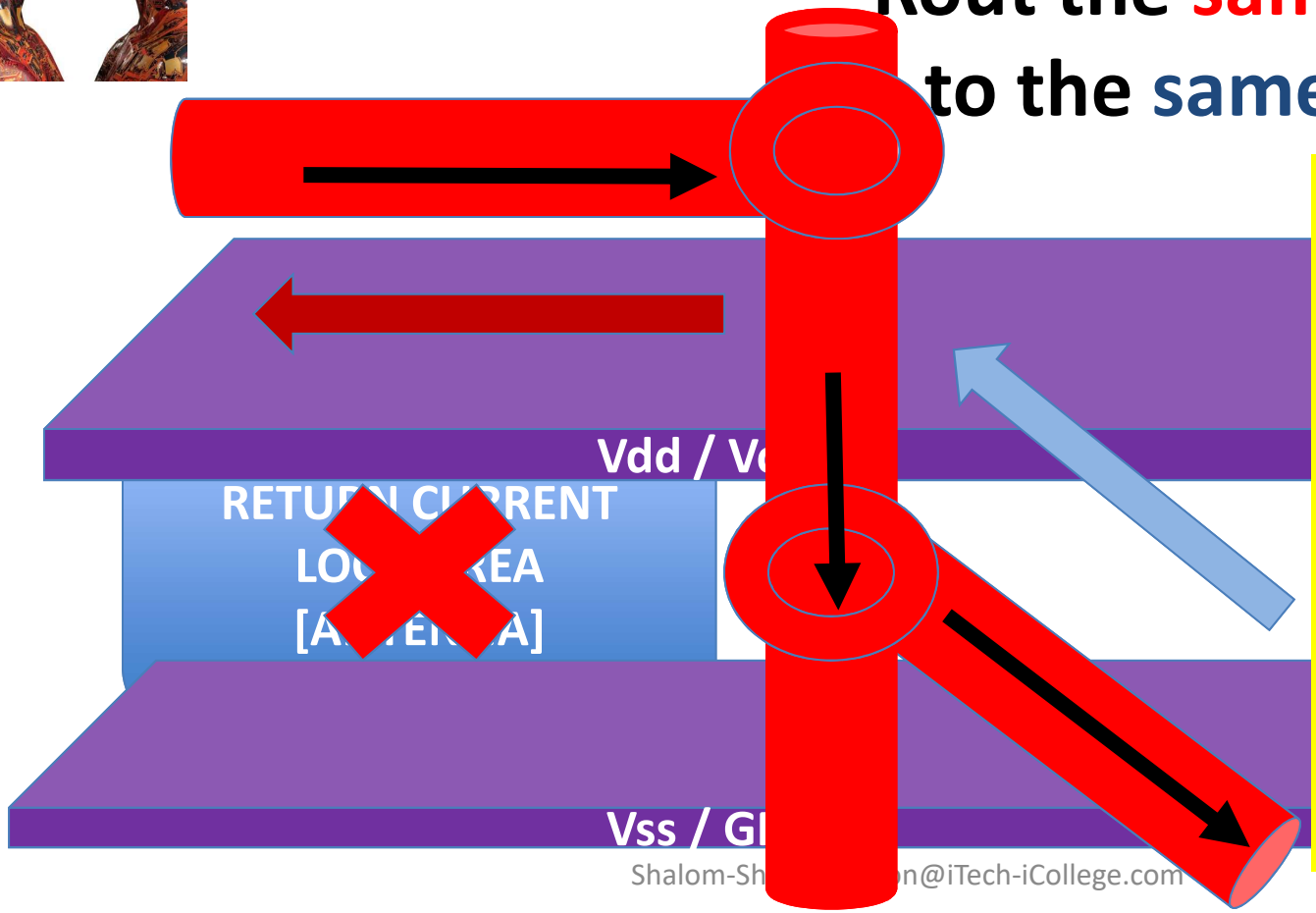



Signal AA
Signal BB
Top Layer
Sz2
Prepreg
ernal Ground Plar
Core
ernal Routing Laye
Prepreg
ernal Routing Laye
Core
ternal Power Plan
Prepreg
Bottom Layer
0.005”
0.005”
0.040”
0.005”
0.005”
Signal AA
Signal BB

Sz2 SHLOMI zigdon, 10/10/2018

Vertical & Horizontal Routing

Rout the same Signal closed to the same Power Plane



Returning signal current at this via pops between the top and bottom surfaces of the solid reference plane by passing through the clearance hole.

Faraday Cages

L1 TOP – ½+1 Oz
L2 GND - 1 Oz
L3 SIGNALS-H - 1/2 Oz
L4 GND Oz
L5 SIGNALS – V-1/2 Oz
L6 GND - 2 Oz
L7 Power Splitted – 2 oz

Short Pad
PLAN - 2 Oz
SIGNALS-H - 1/2 Oz
PLA 2 Oz
SIGNALS –V - 1/2 Oz

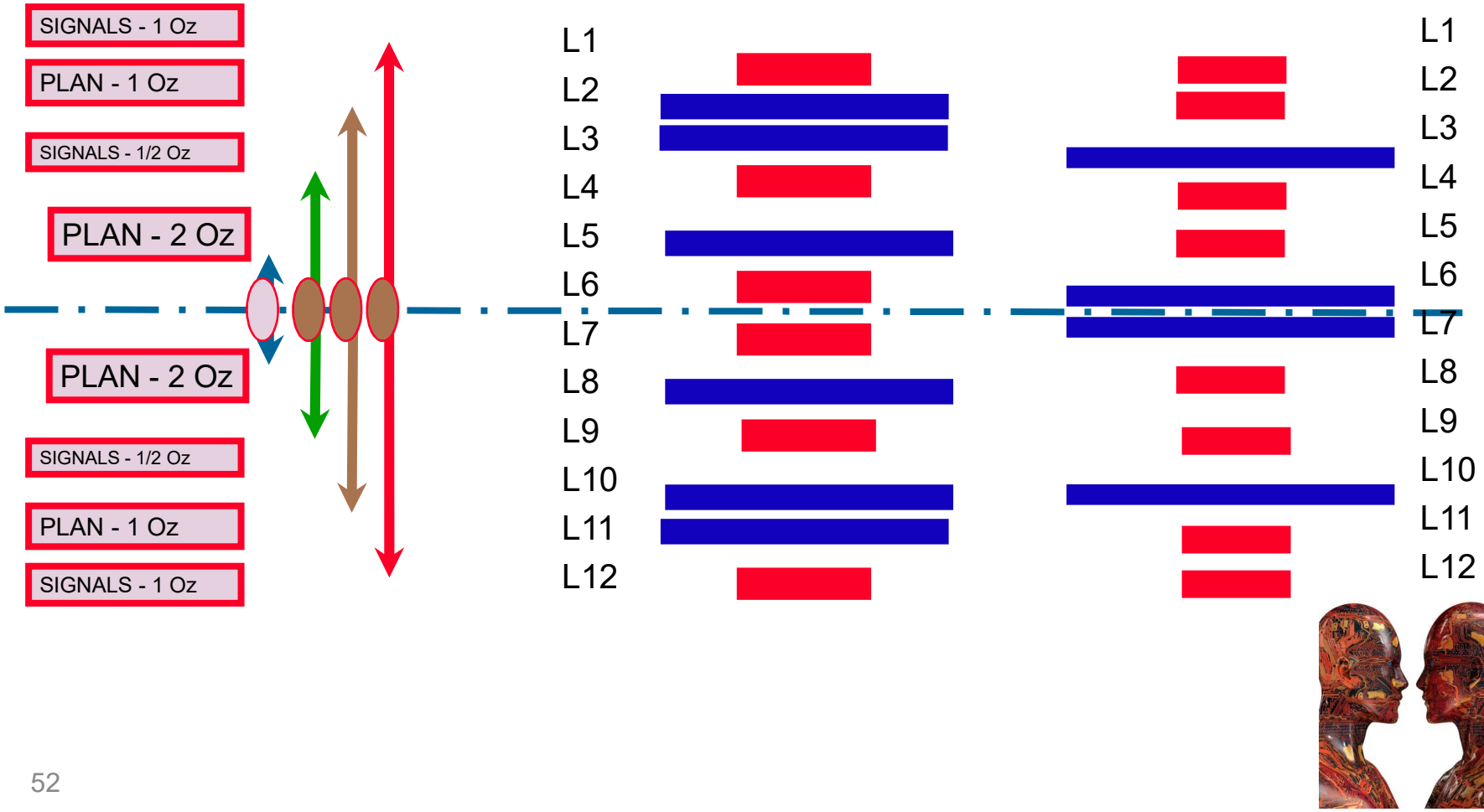
PLAN - 2 Oz
SIGNALS –V

L8 Power Splitted – 2 oz
L9 GND - 2 Oz
L10 SIGNALS – H-1/2 Oz
L11 GND - 1
L12 SIGNALS –V - 1/2 Oz
L13 GND - 1 Oz
L14 BOTTOM – ½+1 Oz

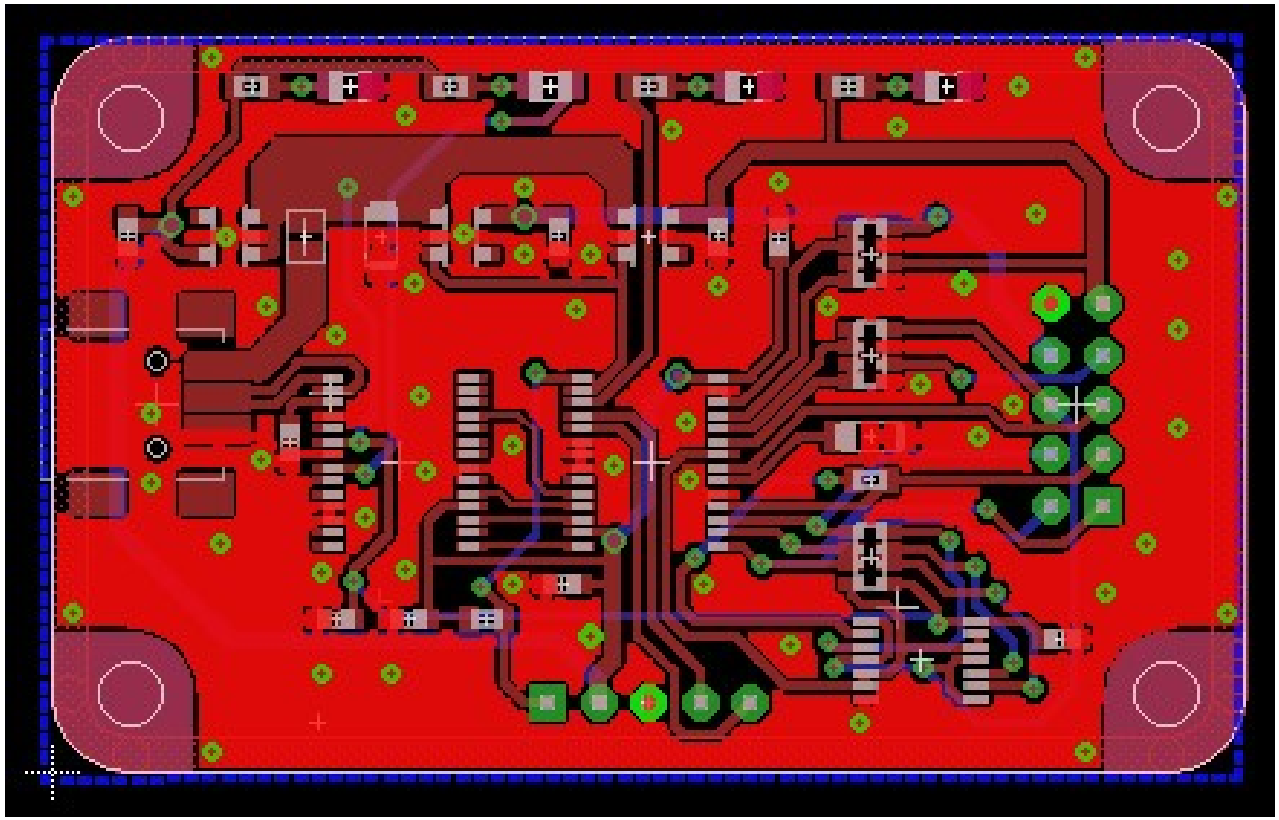
SIGNALS-H - 1/2 Oz
PLA 2 Oz
SIGNALS –V - 1/2 Oz
PLAN - 2 Oz
Pad Short

SIGNALS-H
PLAN - 2 Oz
DON'T

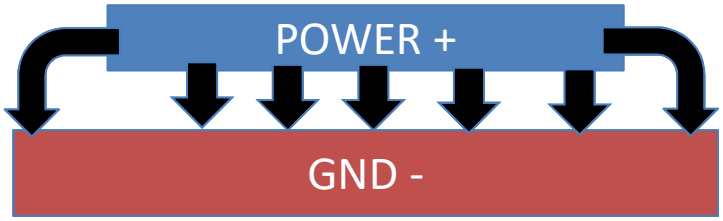
Copper Balance



In case of non balance – fill the Signal Layers in GND Copper

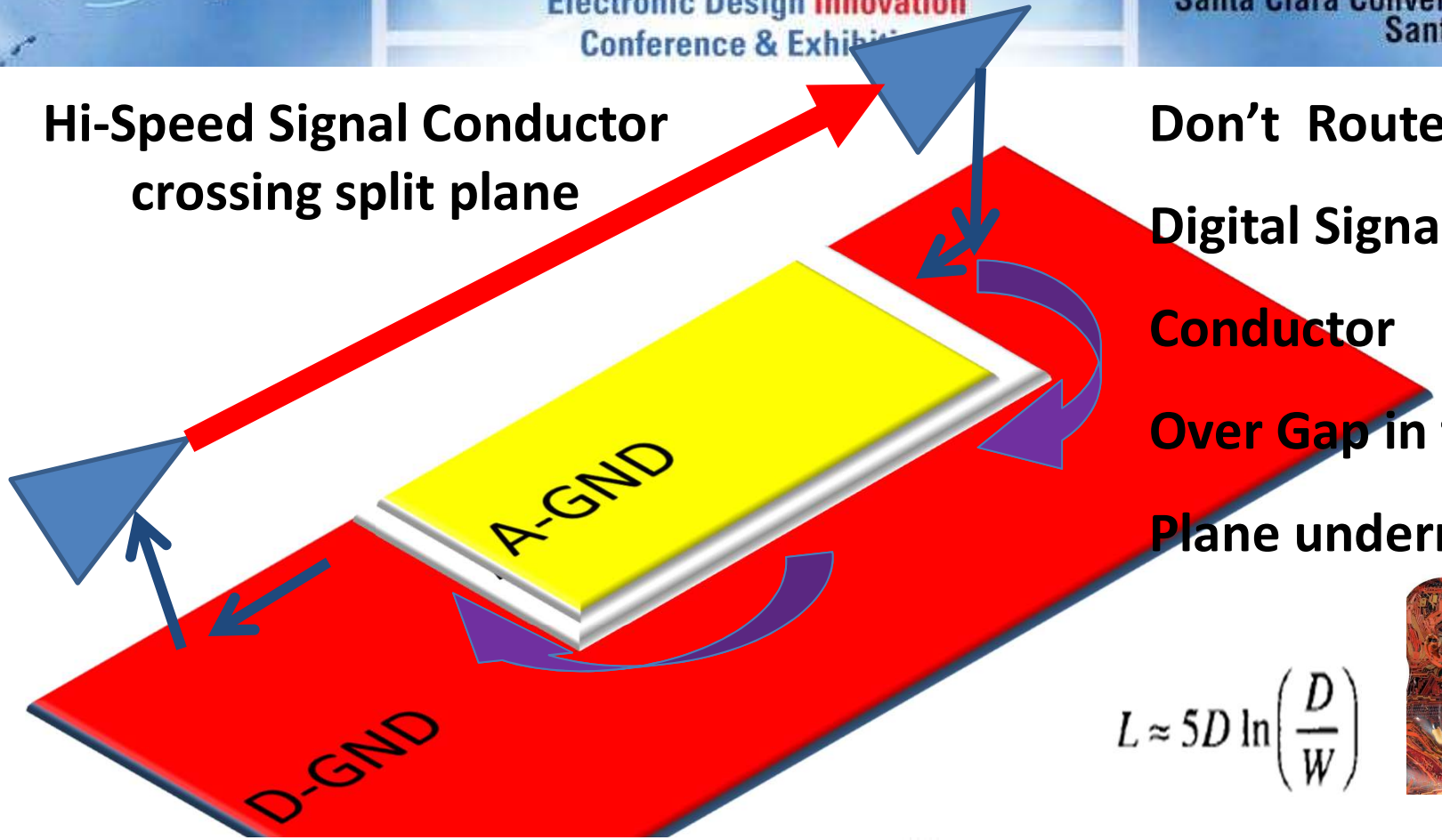


Prevent Fringing Fields



20 H RULE

Hi-Speed Signal Conductor crossing split plane



Don't Route Digital Signal Conductor Over Gap in the Plane underneath

$$L \approx 5D \ln\left(\frac{D}{W}\right)$$

$$T_{composite} = \left[\left(T_{10-90\,L/R}\right)^2 + \left(T_{10-90\,signal}\right)^2\right]^{1/2}$$

$$T_{10-90\,L/R} = 2.2\frac{L}{2Z_0}$$

High Speed Digital Design: A Handbook of Black Magic

Signal Groups Classes

Sensitive

Noisy

Natural

Lossy Lines [needs low “loss-tangent/Dissipation Factor/ Tangent Delta”]

High Speed Signals

Clocks

Differential Signals – “SEDRDES”

Communication – USB2, USB3, PCIexpress Gen 1/2/3/4, HDMI

Video/Audio

Power Groups Classes

External Power Supply [not Filtered]

Internal Power Supply [Filtered]

Different Voltages level

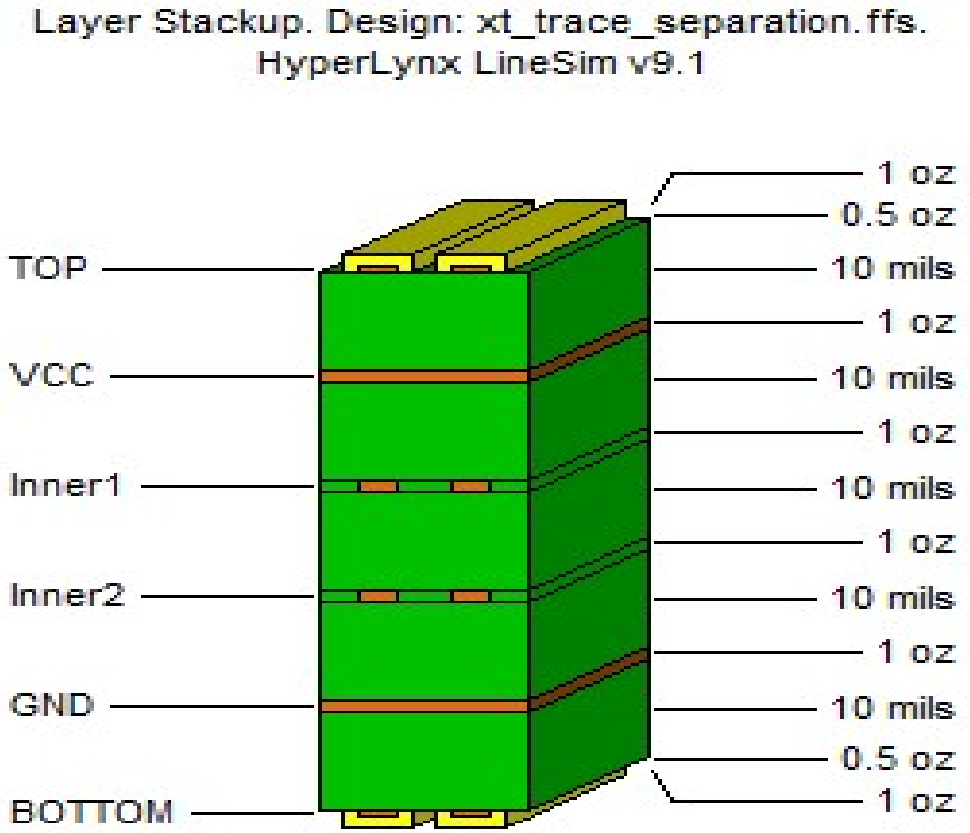
Different Grounds on PCB

Ground Tree, "Star-Point" placement [if Ground plane Splitted]

internal Dual Stripline h=10

Field Solver Stackup

Type	Thickness	Dielectric	Layer
Signal	2.02	1.00	TOP
Diel	10.00	4.30	
Plane	1.35	4.30	VCC
Diel	10.00	4.30	
Signal	1.35	4.30	Inner1
Diel	10.00	4.30	
Signal	1.35	4.30	Inner2
Diel	10.00	4.30	
Plane	1.35	4.30	GND
Diel	10.00	4.30	
Signal	2.02	1.00	BOTTOM



Crosstalk internal Dual-Stripline

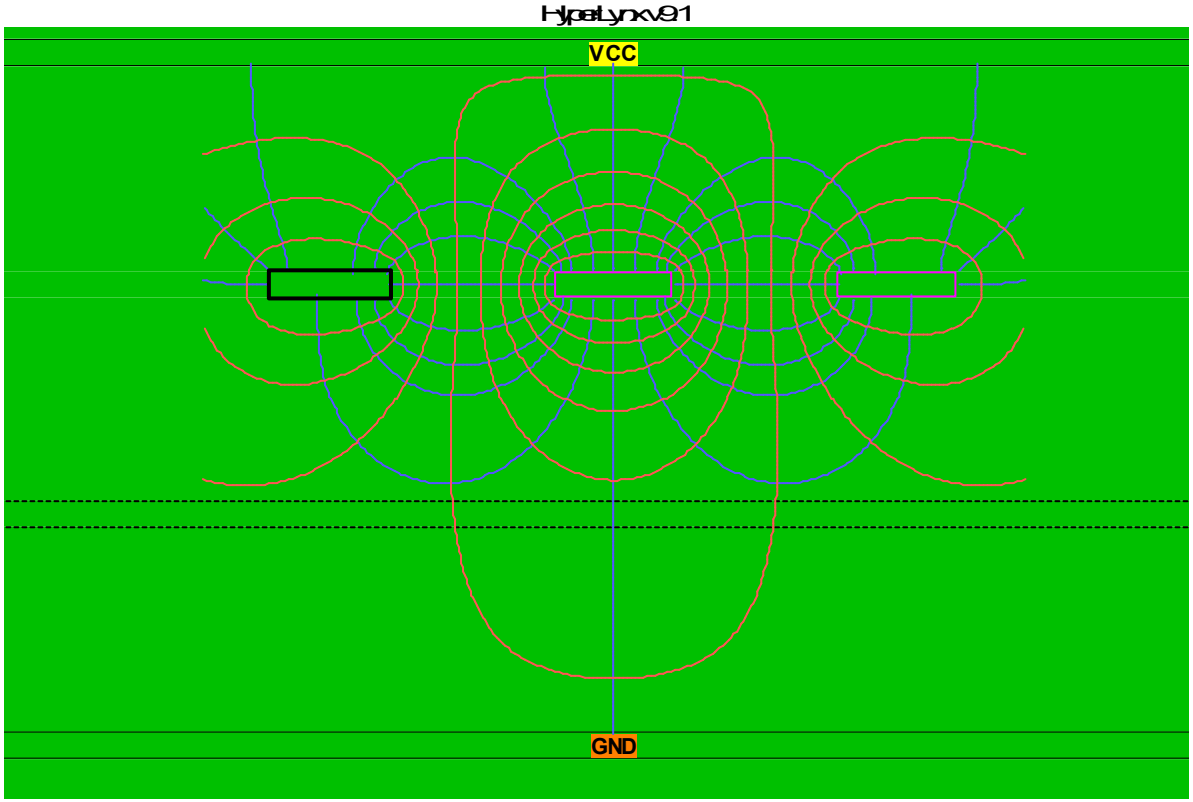
6/8/6/8/6 h=12 + - +

Capacitance Matrix [pF/m]:

	1	2	3
1	117.119	-25.128	-1.432
2	-25.128	123.450	-25.128
3	-1.432	-25.128	117.119

Inductance Matrix [nH/m]:

	1	2	3
1	428.627	92.346	25.053
2	92.346	425.150	92.346
3	25.053	92.346	428.627



Crosstalk internal Dual-Stripline

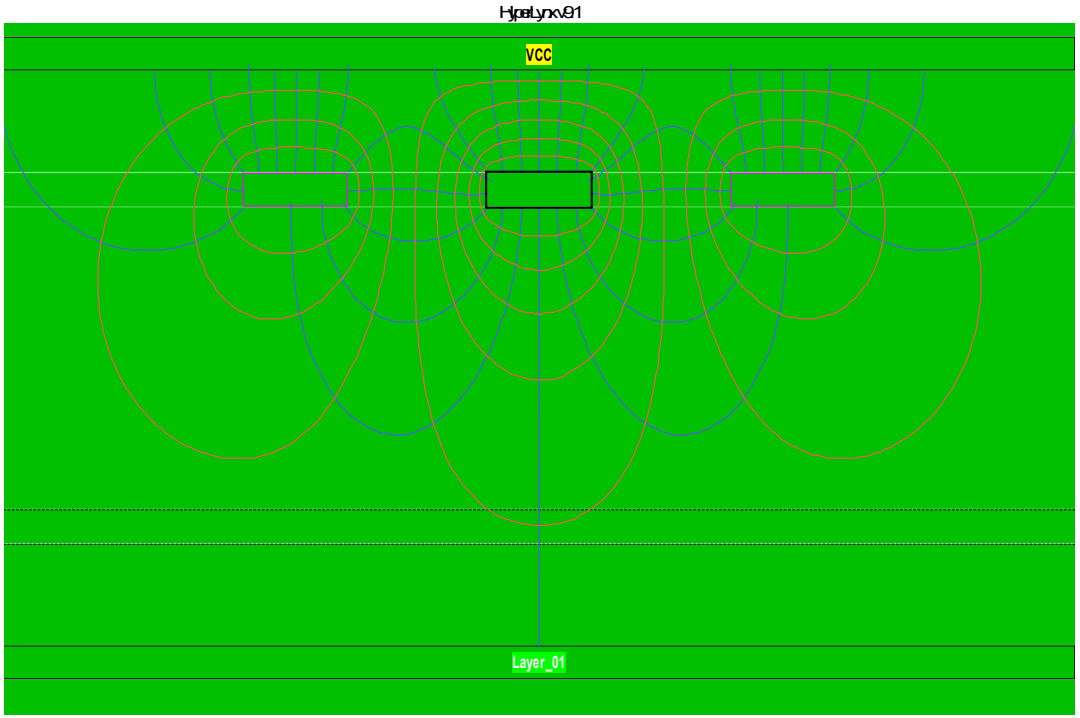
6/8/6/8/6 h=4 + - +

Capacitance Matrix [pF/m]:

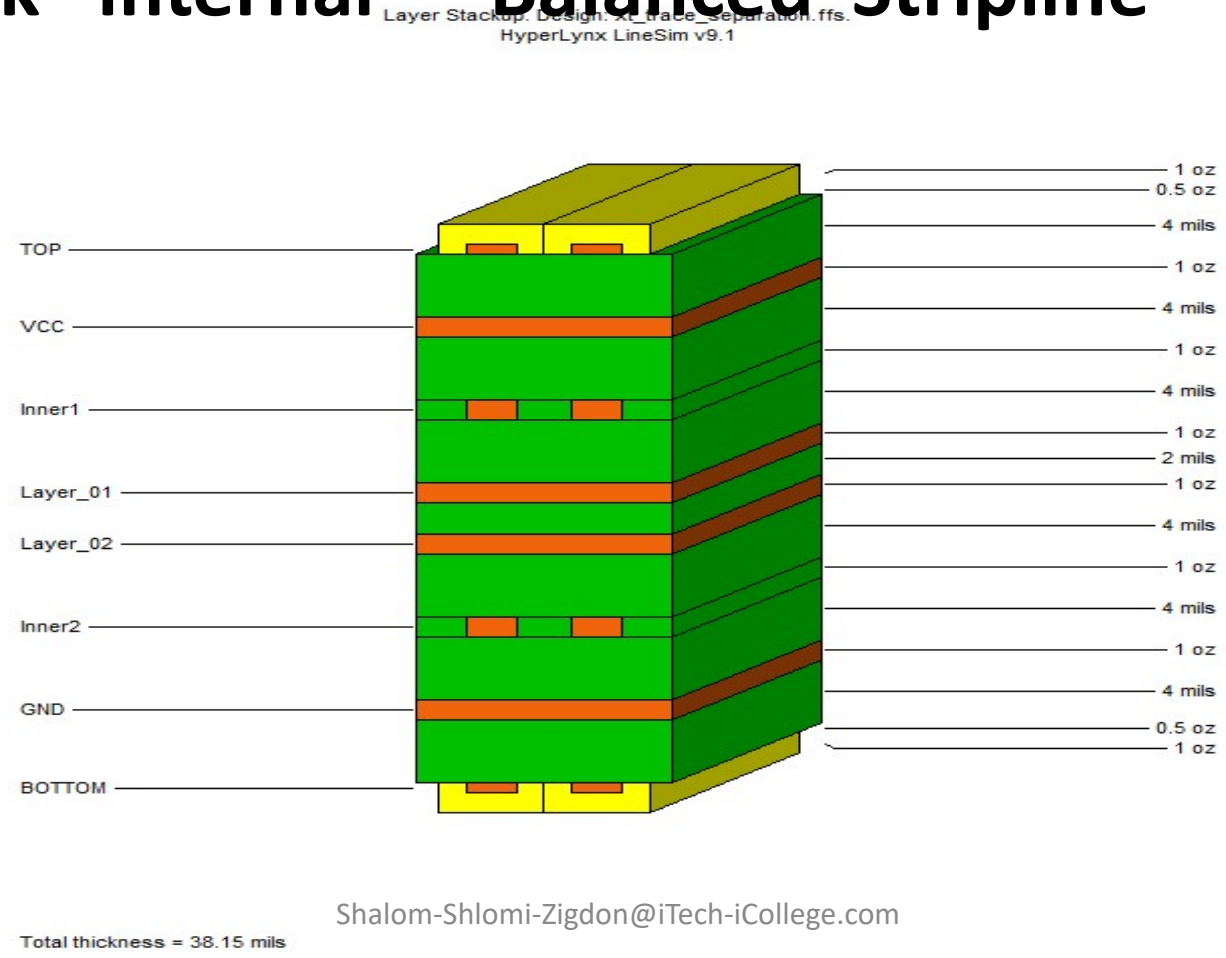
	1	2	3
1	165.191	-14.786	-0.510
2	-14.786	167.044	-14.786
3	-0.510	-14.786	165.191

Inductance Matrix [nH/m]:

	1	2	3
1	291.977	26.132	3.240
2	26.132	291.042	26.132
3	3.240	26.132	291.977



Crosstalk internal Balanced Stripline h=4

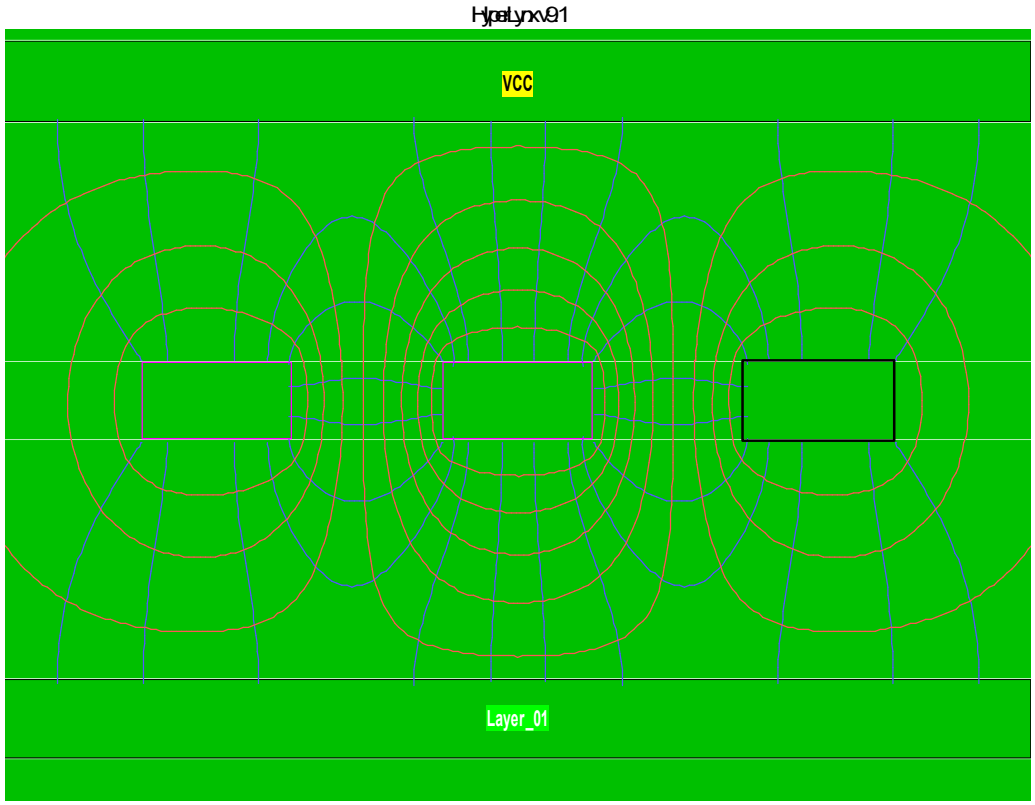


Capacitance Matrix [pF/m]:

	1	2	3
1	175.853	-21.920	-0.061
2	-21.920	180.051	-21.920
3	-0.061	-21.920	175.852

Inductance Matrix [nH/m]:

	1	2	3
1	276.330	34.172	4.356
2	34.172	274.045	34.172
3	4.356	34.172	276.330



Crosstalk internal Balanced Stripline
4/4/4/4/4 h=12 + - +

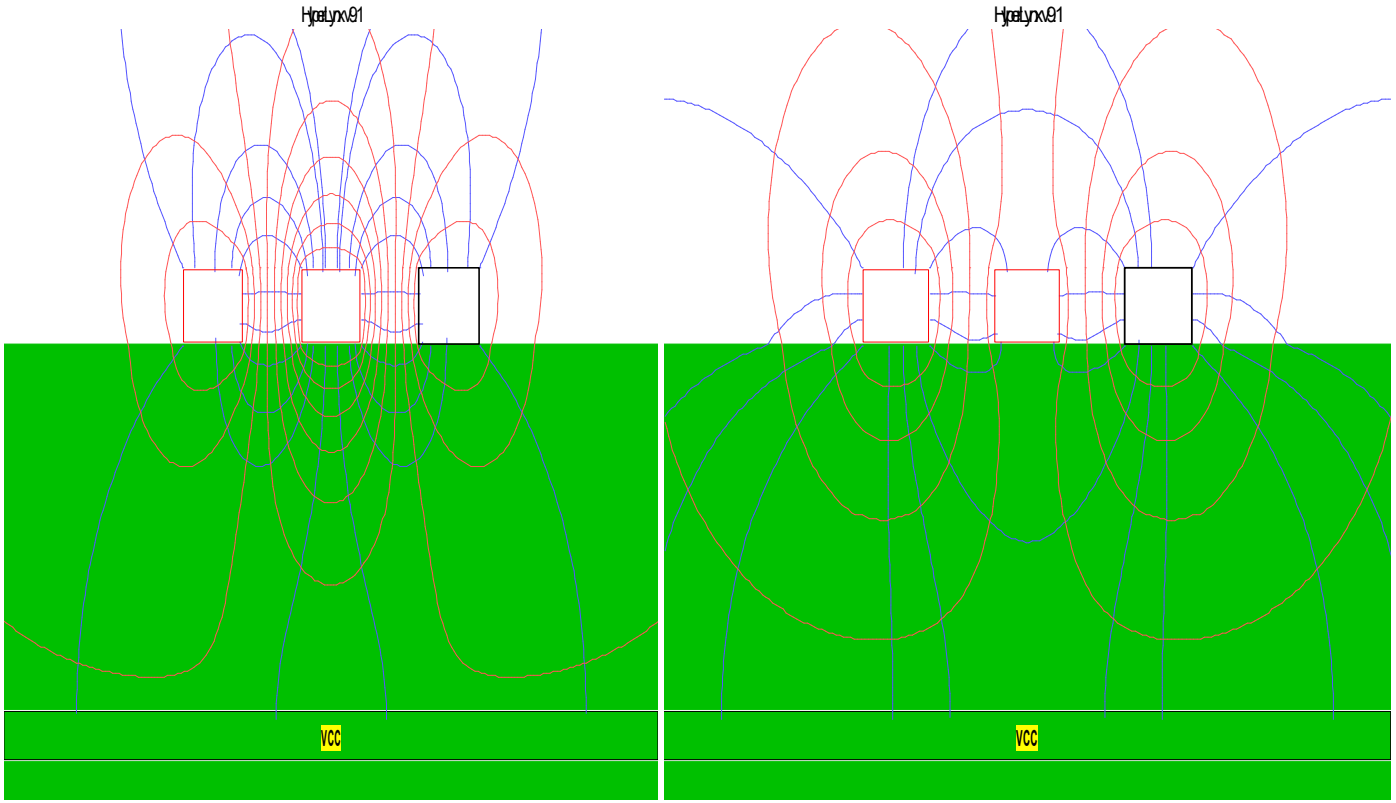
External Crosstalk Microstrip h=12

Capacitance Matrix [pF/m]:

	1	2	3
1	67.875	-21.558	-2.044
2	-21.558	75.553	-21.558
3	-2.044	-21.558	67.875

Inductance Matrix [nH/m]:

	1	2	3
1	491.742	215.819	117.573
2	215.819	482.961	215.819
3	117.573	215.819	491.742



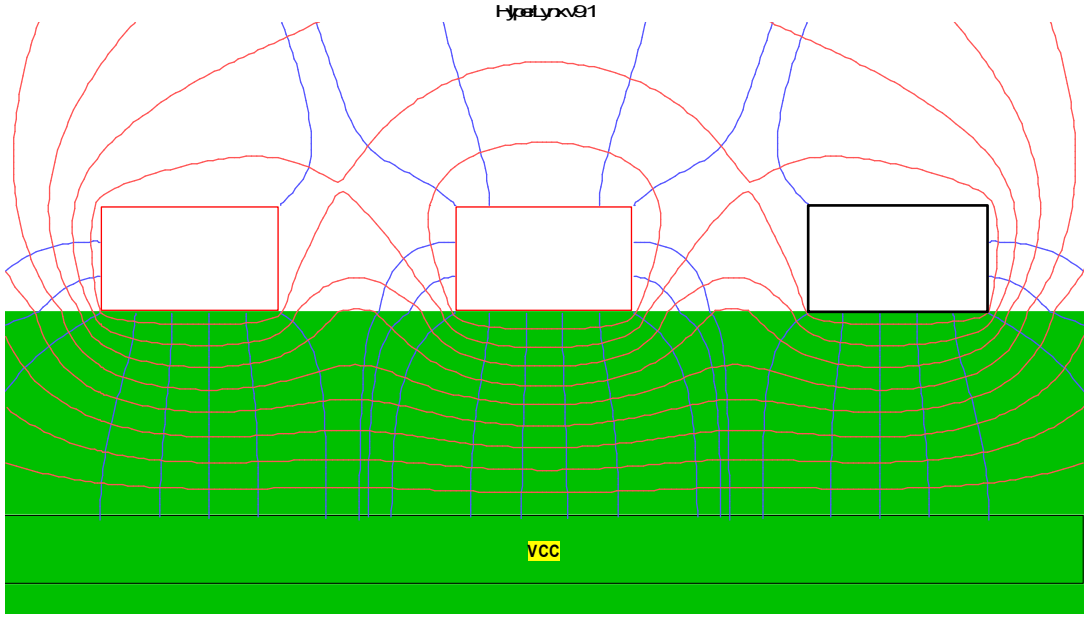
External Crosstalk h=4 Microstrip + + +

Capacitance Matrix [pF/m]:

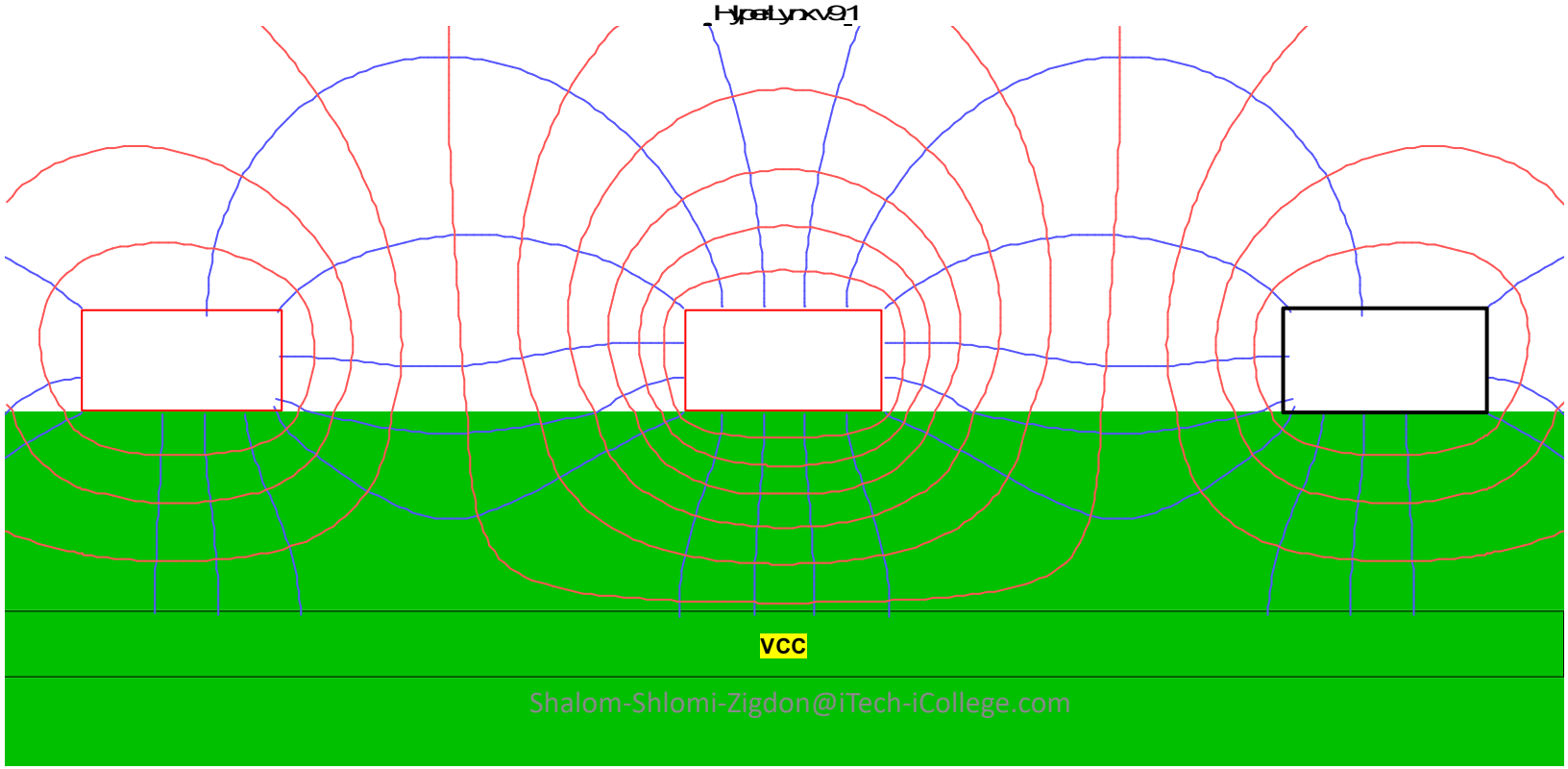
	1	2	3
1	89.707	-5.104	-0.611
2	-5.104	90.167	-5.104
3	-0.611	-5.104	89.707

Inductance Matrix [nH/m]:

	1	2	3
1	346.080	51.467	15.526
2	51.467	344.436	51.467
3	15.526	51.467	346.080

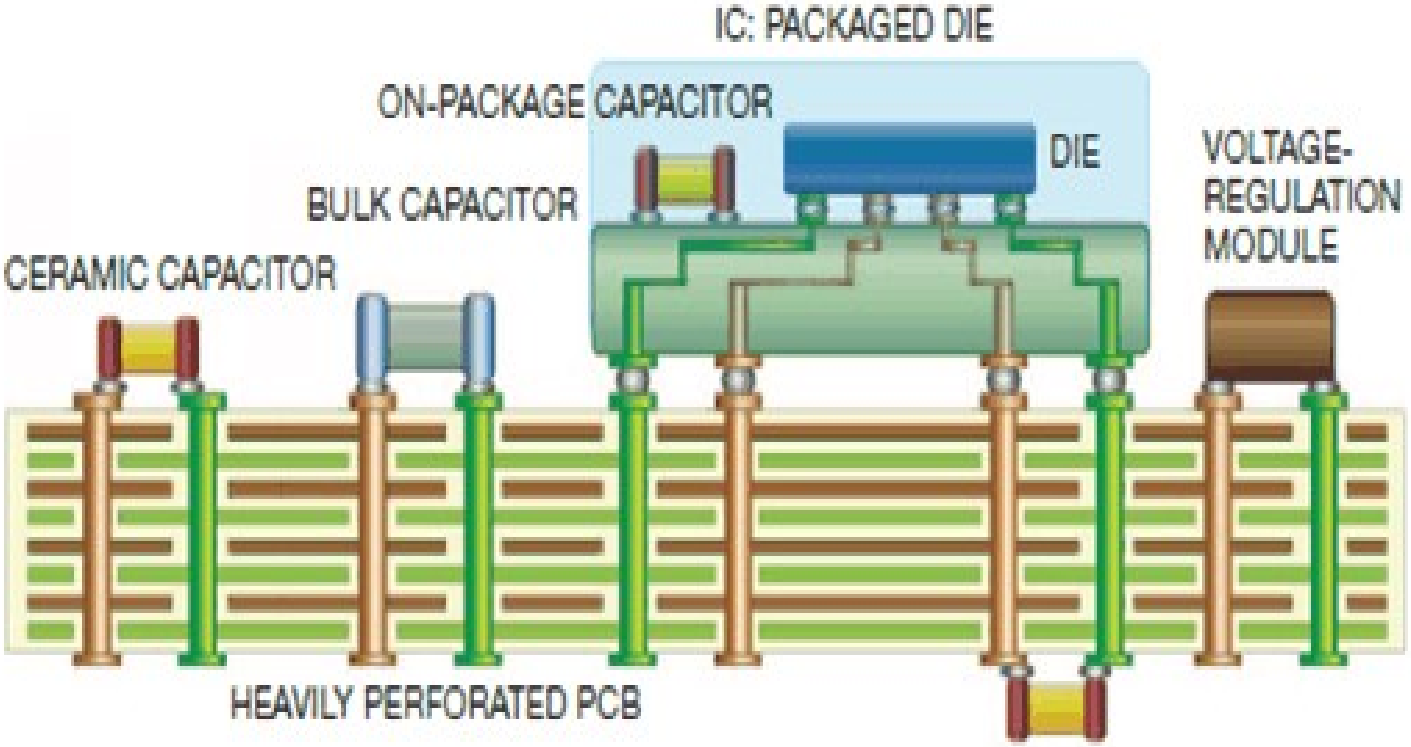


Microstrip - External Layers
EMI Radiation and External Crosstalk
preferred h=< 4 mill



More Power Layers – Better PI

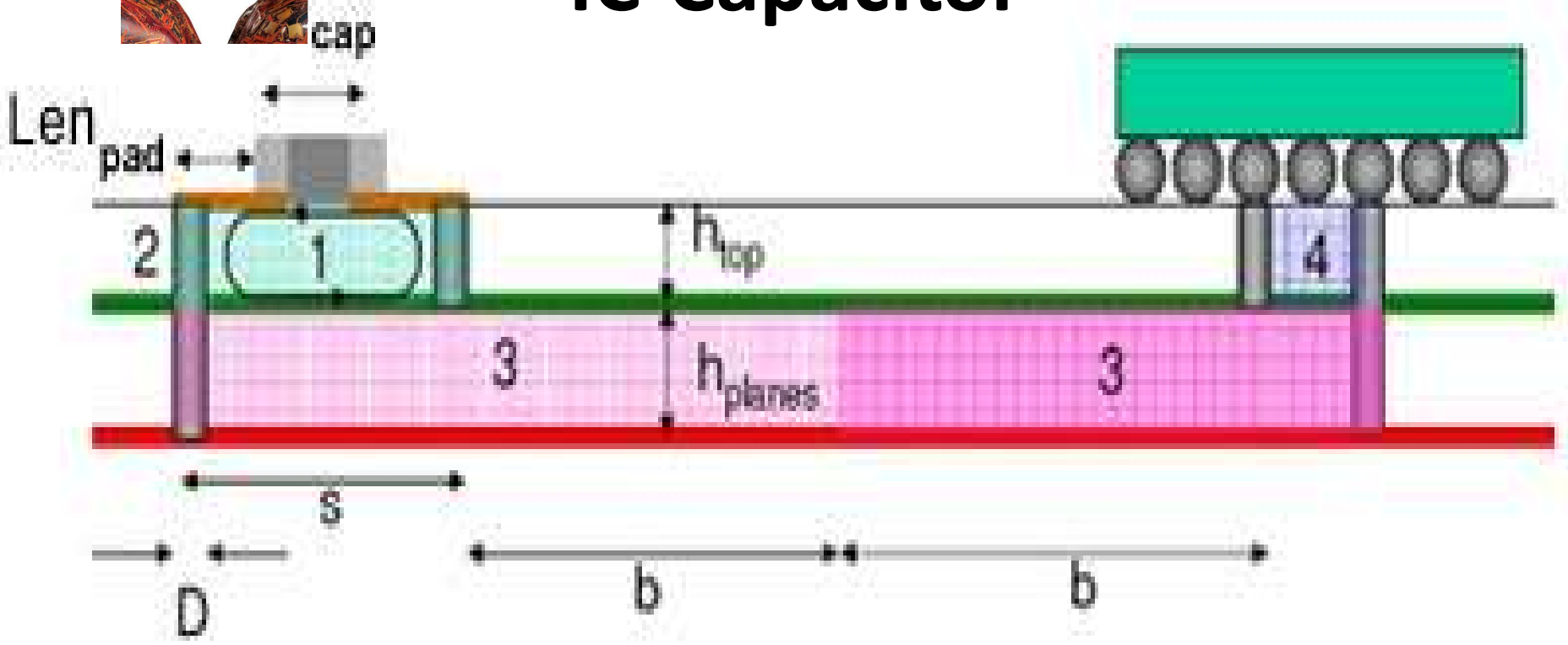
PDN World controlled by Capacitors and Capacitance



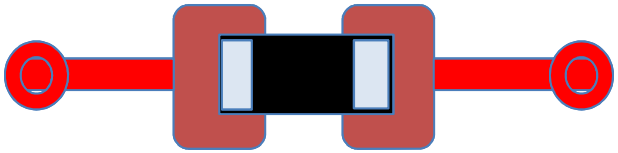
Shalom-Shlomi-Zigdon@iTech-iCollege.com

EDI CON 2018
Electronic Design Innovation Conference & Exhibition
October 17-19 2018
Santa Clara Convention Center
Santa Clara, CA

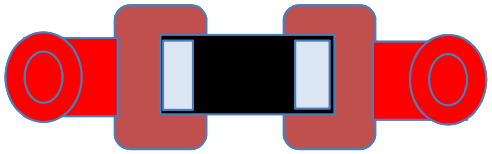
Minimize the Loop Area
IC-Capacitor



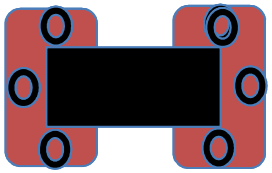
Power Conductors rules for EMC & SI



Worst long & Thin Conductor
Higher Self-Inductance >> EMI



Better Short & Wide Conductor
Minimize Self-Inductance



Preferred 3 Vias act as 3 Inductors in Parallel result as 1/3 Self Induction

Choose and Calculate Bypass/Decoupling Capacitors

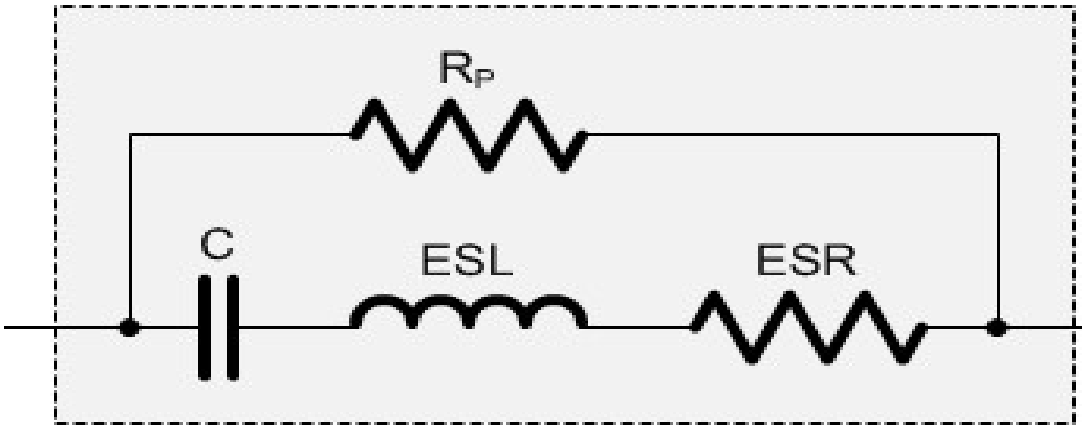
All capacitors shares a common electrical module with 4 main components

1. Capacitance
2. Spark gap [DC Working Volatge much larger than nominal voltage]
3. ESR Equivalent Serious Resistance [contacts, leads, charging and discharging causes heat]
4. ESL Equivalent Serial Inductance [due to self inductance of leads, current loops inside the package]

High Frequency noise – ESL most important

$$z_c = x_L + x_c + R \; = J2\pi F\text{L} + 1/\text{j}2\pi\text{FC} + \text{R}$$

The Real Capacitor



The decoupling capacitor is an obstacle for the high-frequency components of the return current because the associated inductance makes the equivalent impedance of the capacitor too high

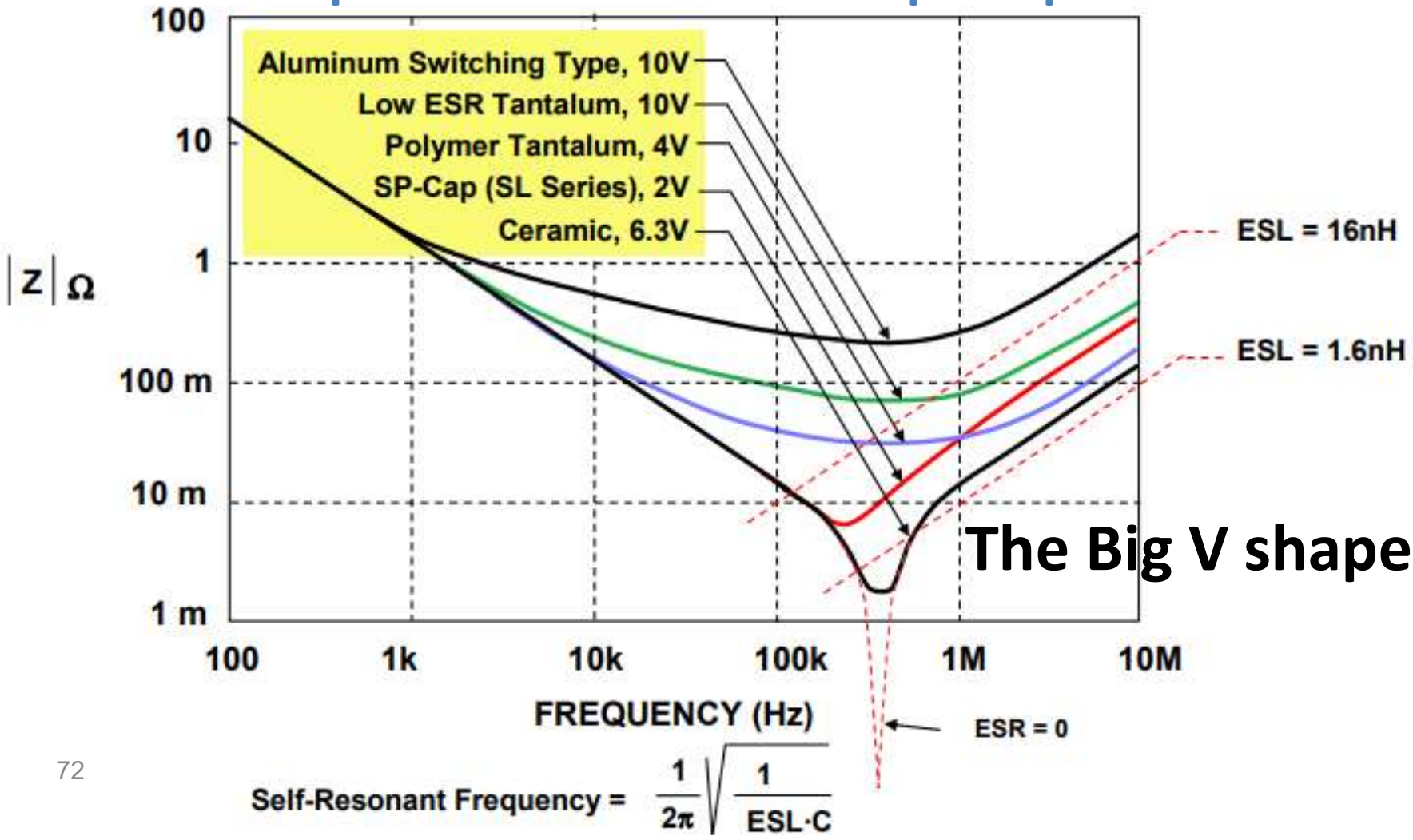
$$SRF = \frac{1}{2\pi\sqrt{ESL \times C}}$$

$$Z = \frac{Voltage \times \max VoltageRipple}{TransientCurrent}$$

$$z_c = x_L + x_c + R \; = J2\pi F\text{L} + 1/\text{j}2\pi\text{FC} + \text{R}$$

requency	***impedance***
Low	Capacitive
Self-Resonance	Resistive
High	Inductive

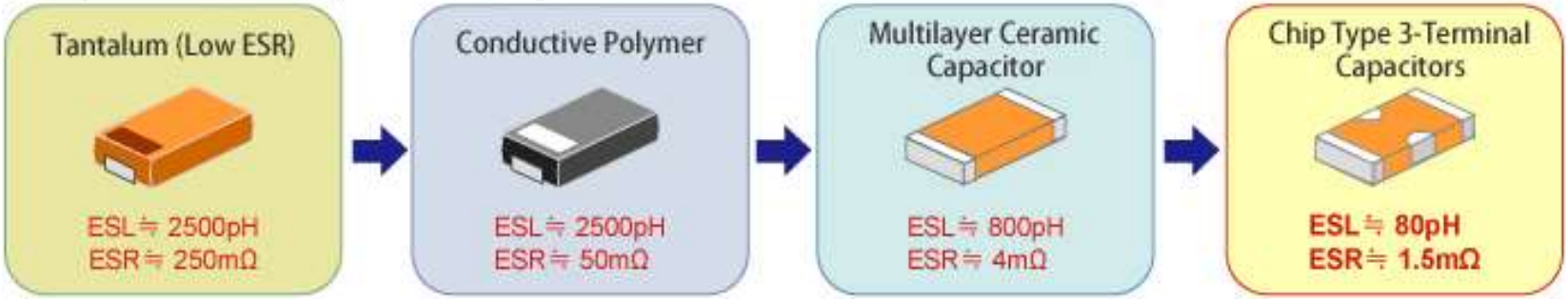
Impedance of Various 100µF Capacitors



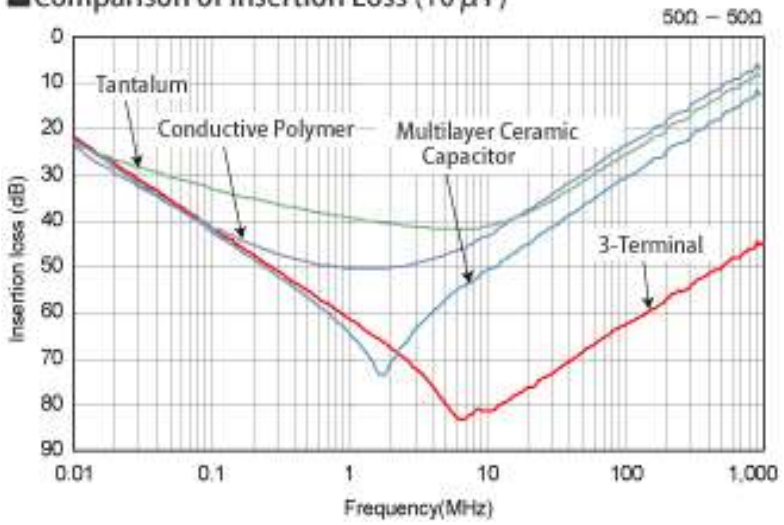
The Big V shape

ESL & ESR 10uF 6.3 V

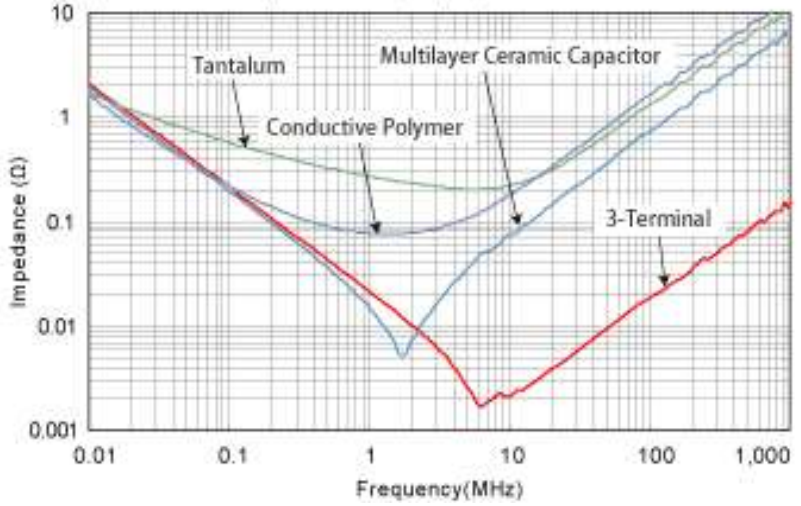
Example of ESL & ESR Comparison with 10 μF / 6.3V



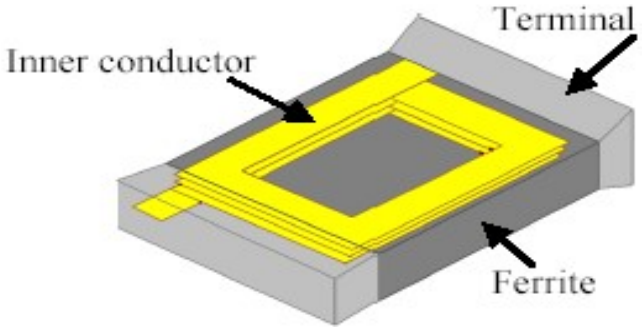
■Comparison of Insertion Loss (10 μF)

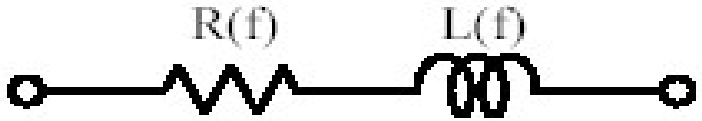


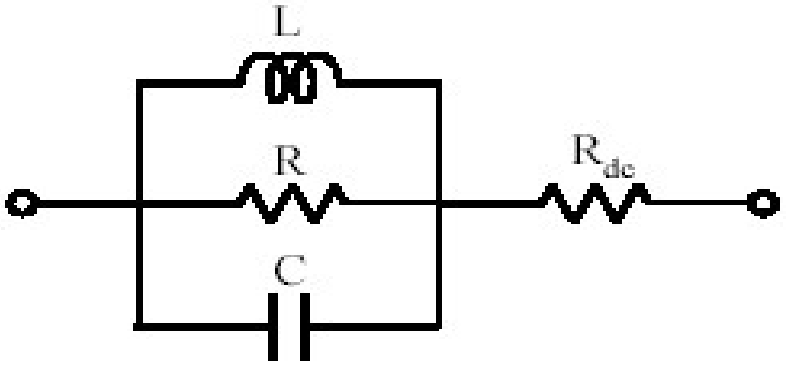
■ Comparison of Impedance (10 μF)



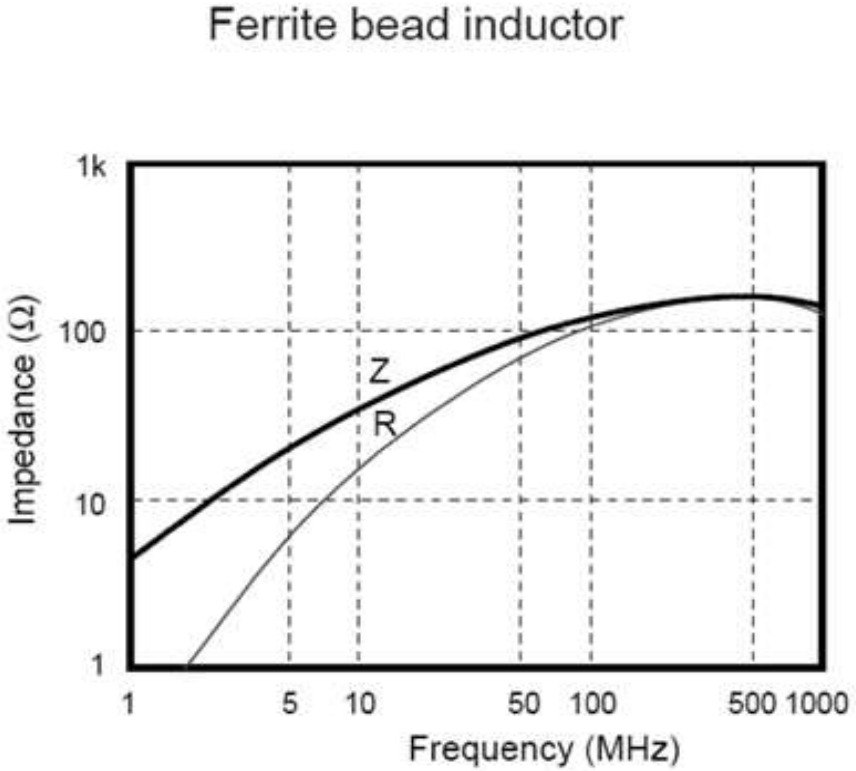

Wire
Ferrite


Terminal
Inner conductor
Ferrite


R(f)
L(f)


L
R
R_{dc}
C

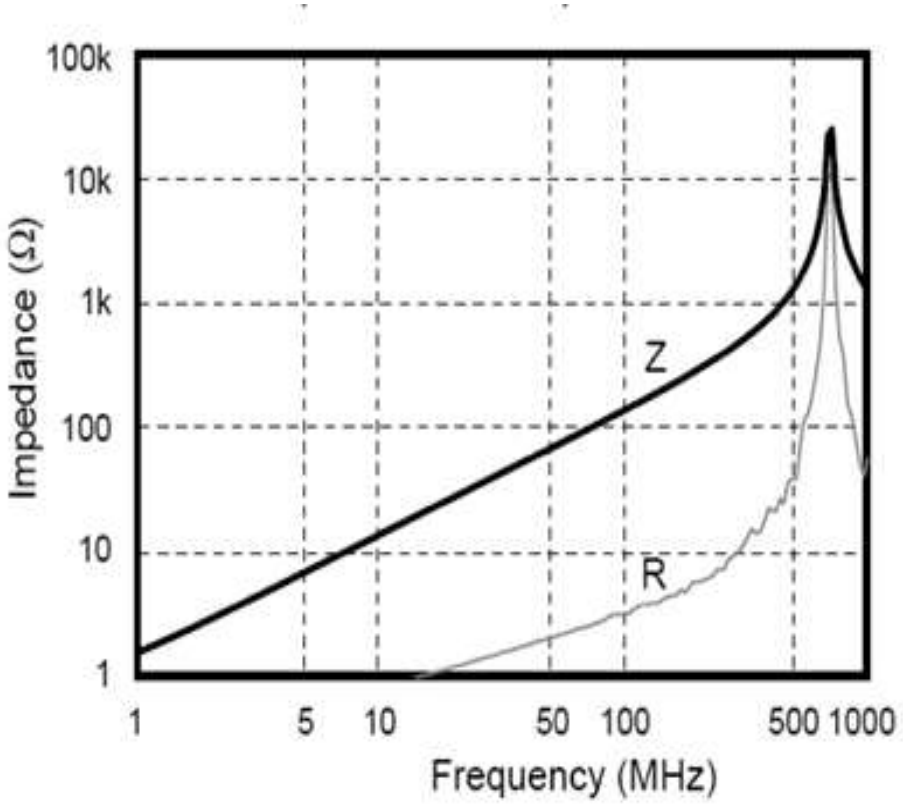
Practical Ferrite Bead



Resistance is dominant.

(The loss is high.)

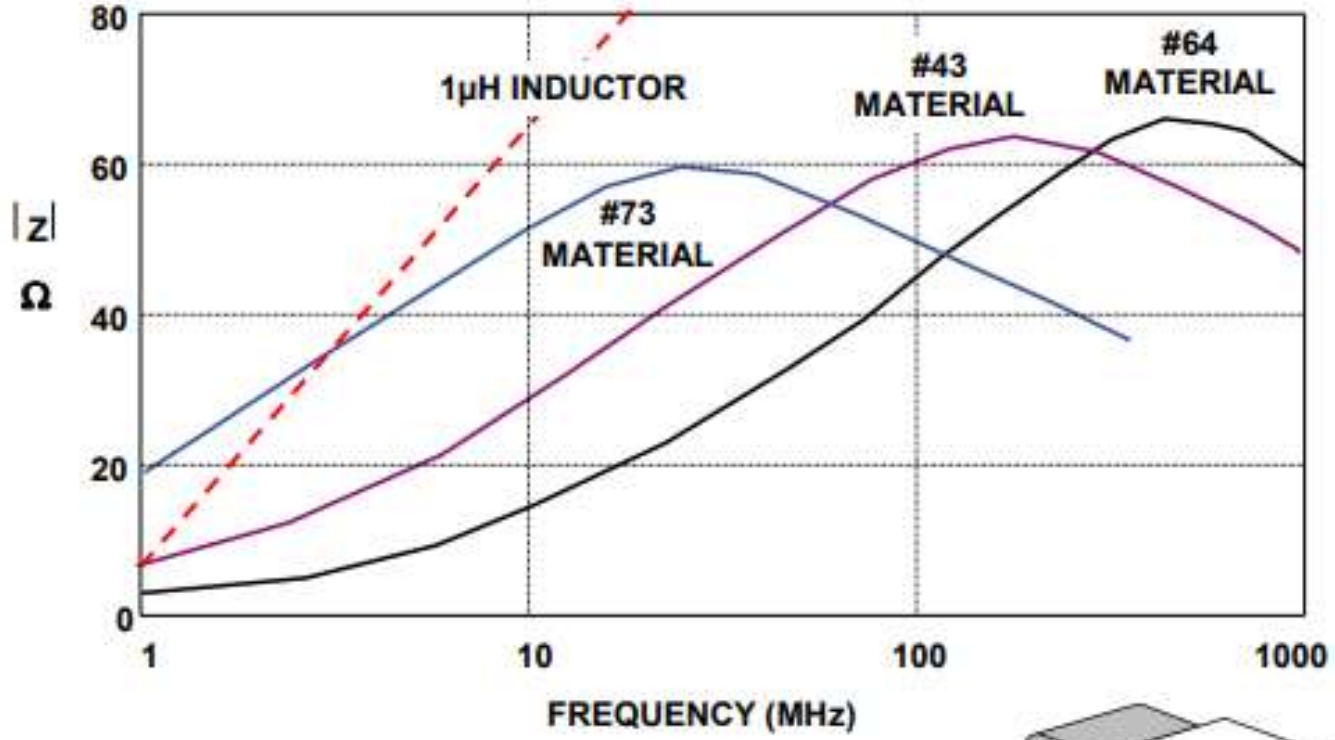
Practical Inductor



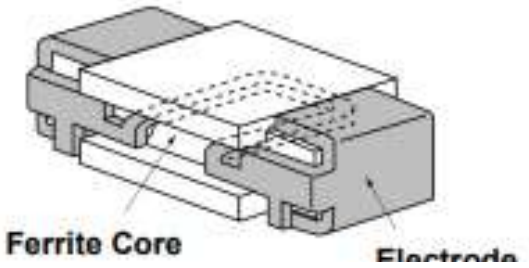
Resistance is small.

(The loss is low, i.e. "Q" is high.)

Ferrite Bead Impedance Compared to a 1µH Inductor

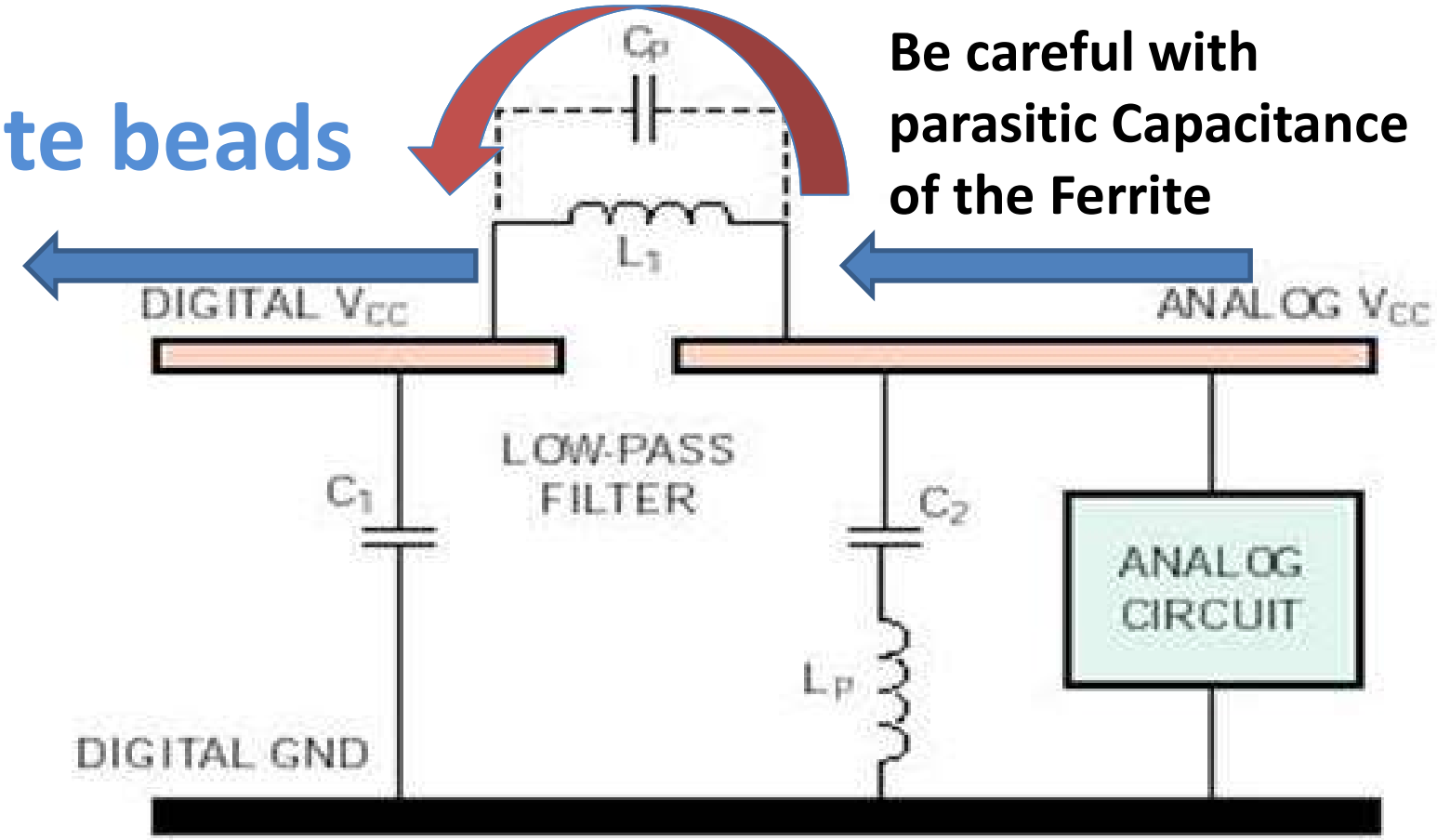


Courtesy: Fair-Rite Products Corp, Wallkill, NY
(http://www.fair-rite.com)



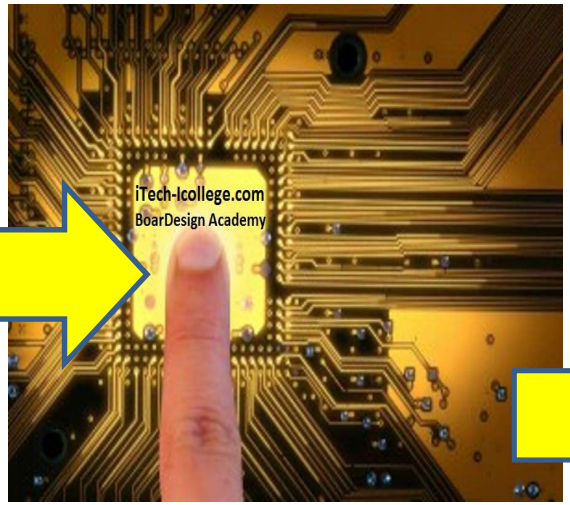
Ferrite beads

Be careful with parasitic Capacitance of the Ferrite



Drawing: courtesy EDN Magazine

Synergy

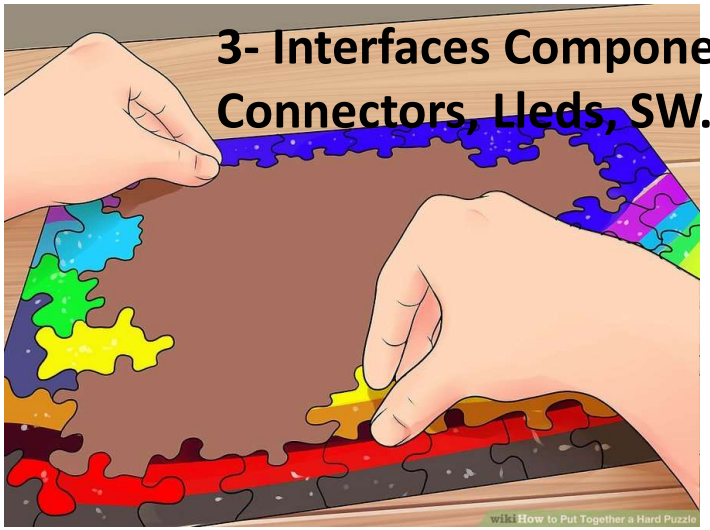


Build a Team Work
For Brain Storming

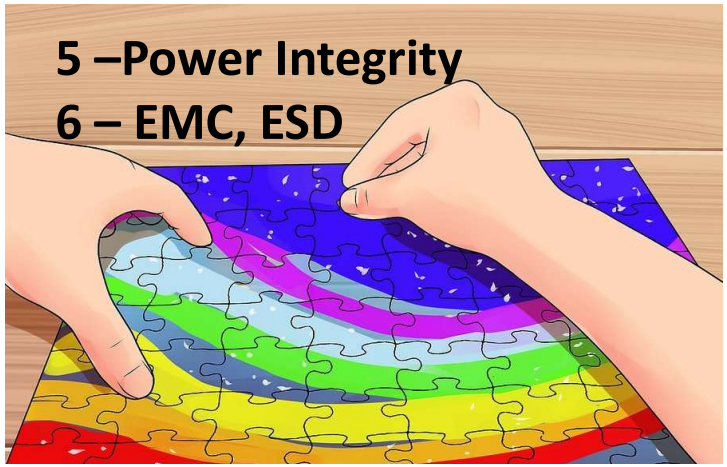
Development = Electronics + Mechanics + Thermal Management
+ Engineering/PCB/Technologist
Better be a part of a Team
Than a group of people doing Team Work

PLACEMENT Order RULES

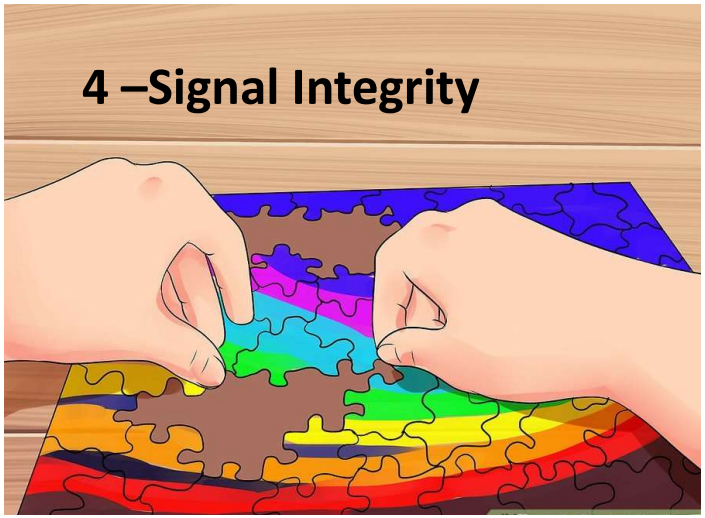
1- Mechanical Outline & Holes
2- Thermal Management



3- Interfaces Components Connectors, Lleds, SW.'s

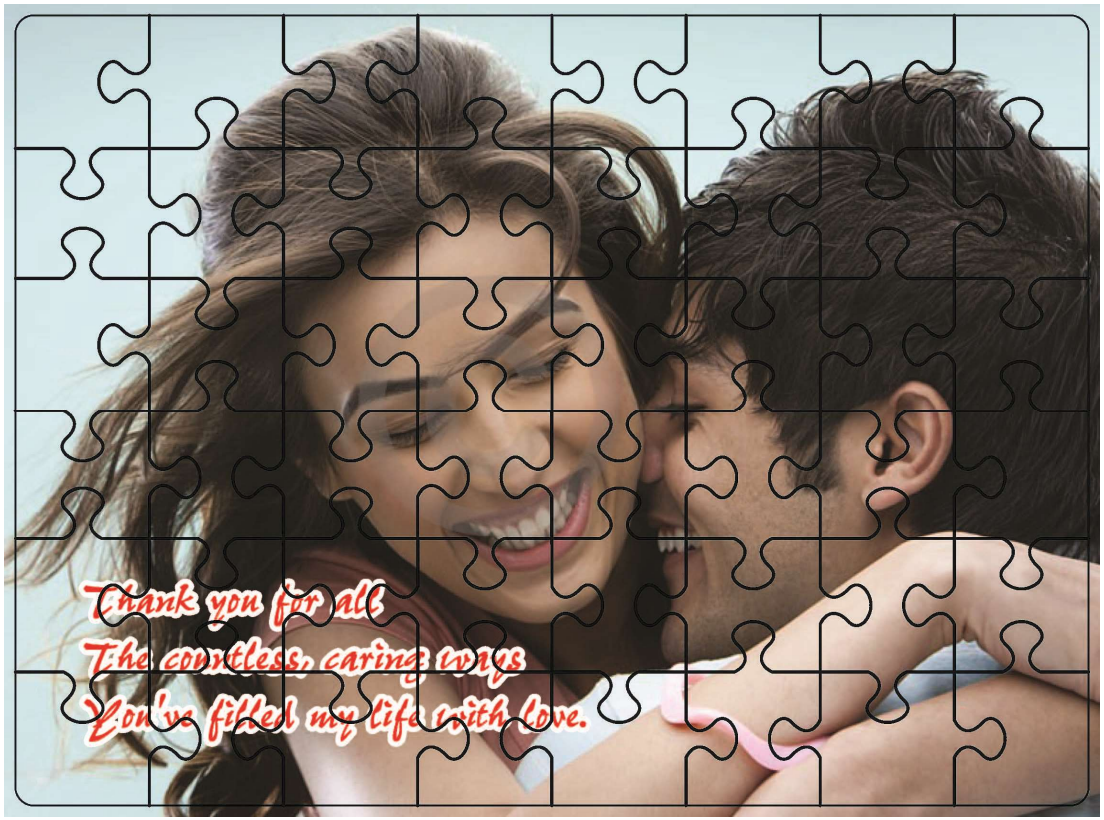


5 –Power Integrity
6 – EMC, ESD



4 –Signal Integrity

PLACEMENT RULES



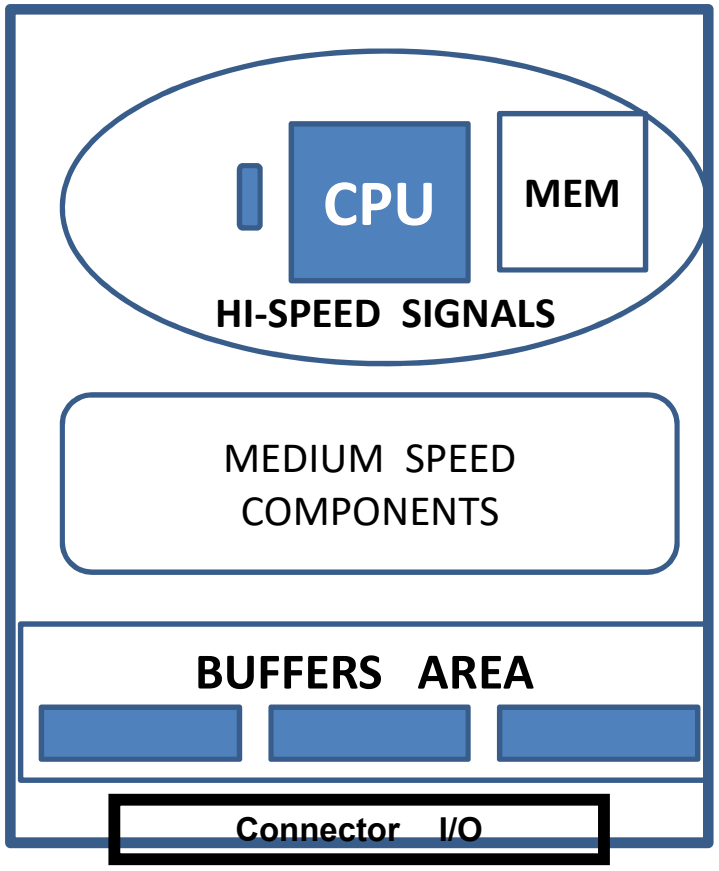
High-Speed Board Start with microP/microC in the middle, far away from the I/O Connectors

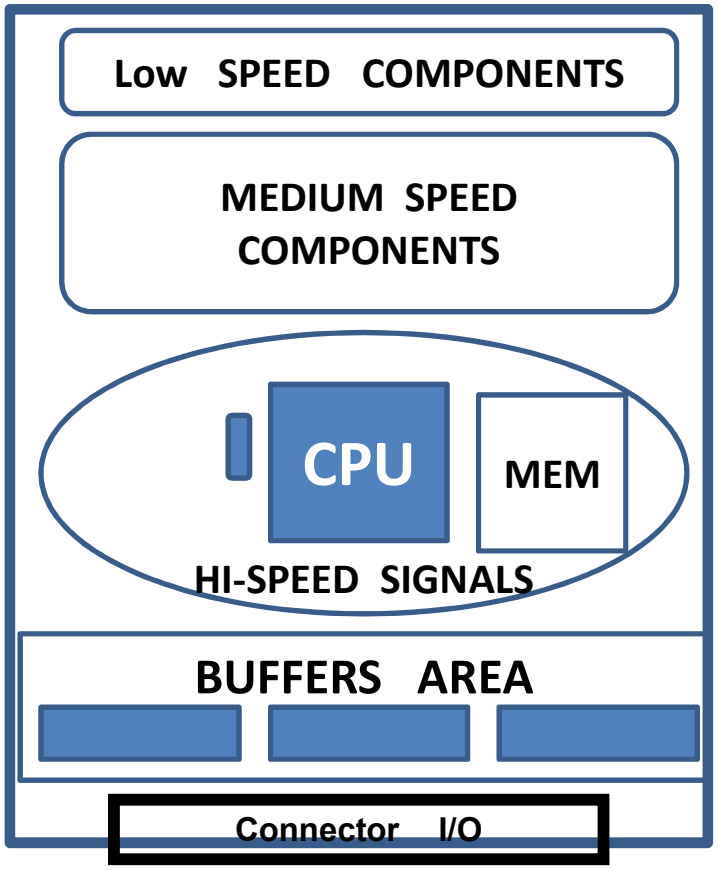
PLACEMENT RULES

No microP/microC?

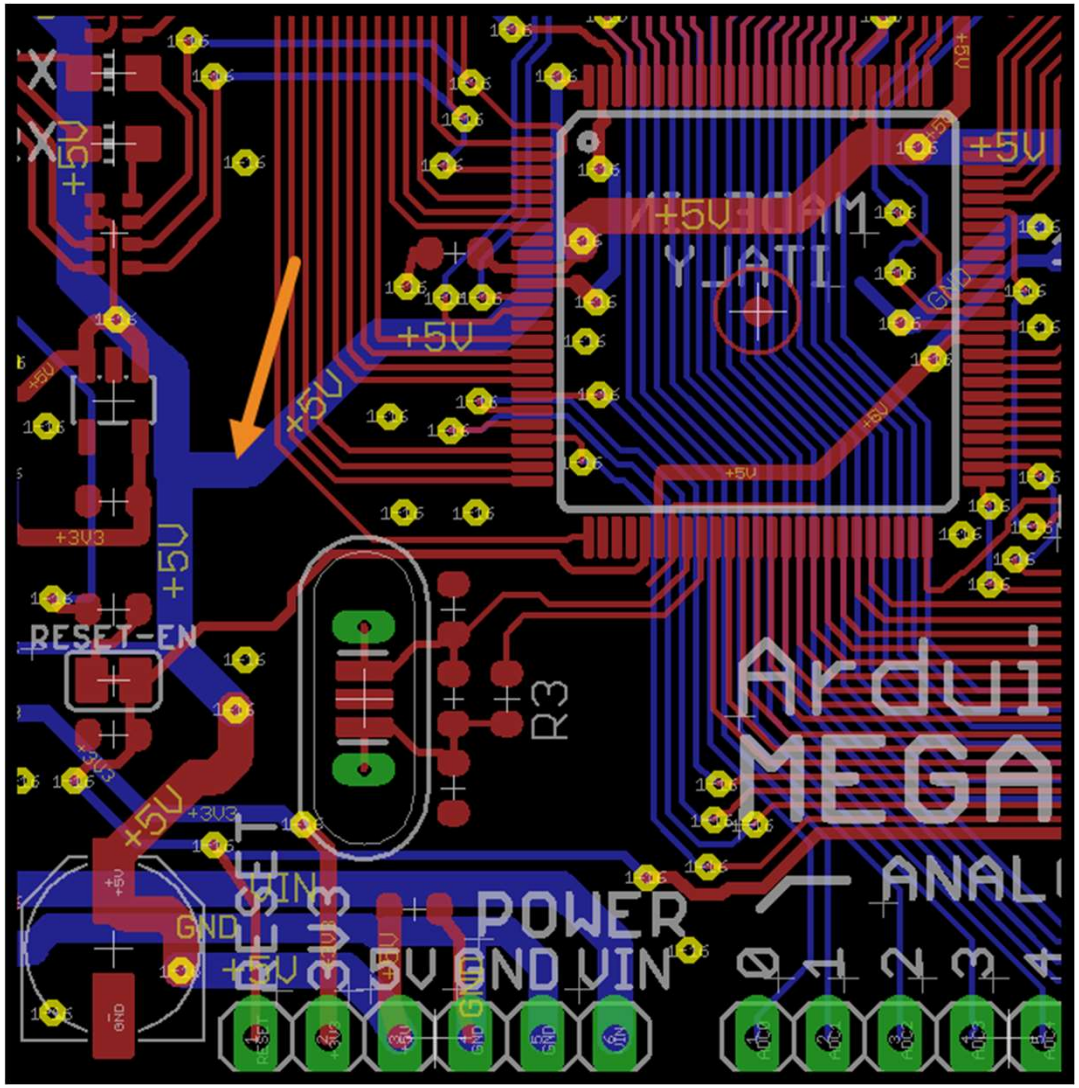
Place outside the PCB Outline each Group according the Schema pages

PCB Placement of Digital

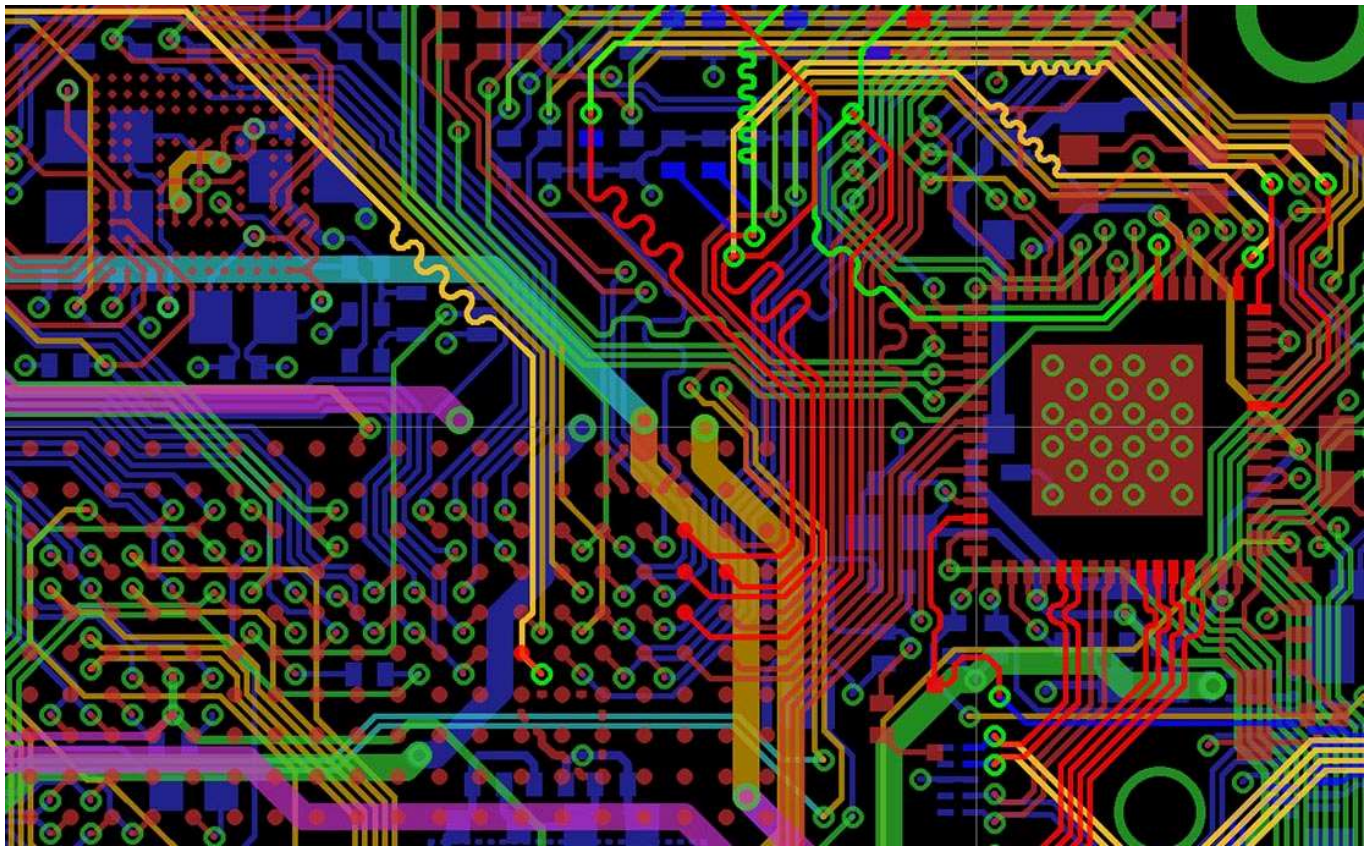




Design Your Power and Ground Traces Wider

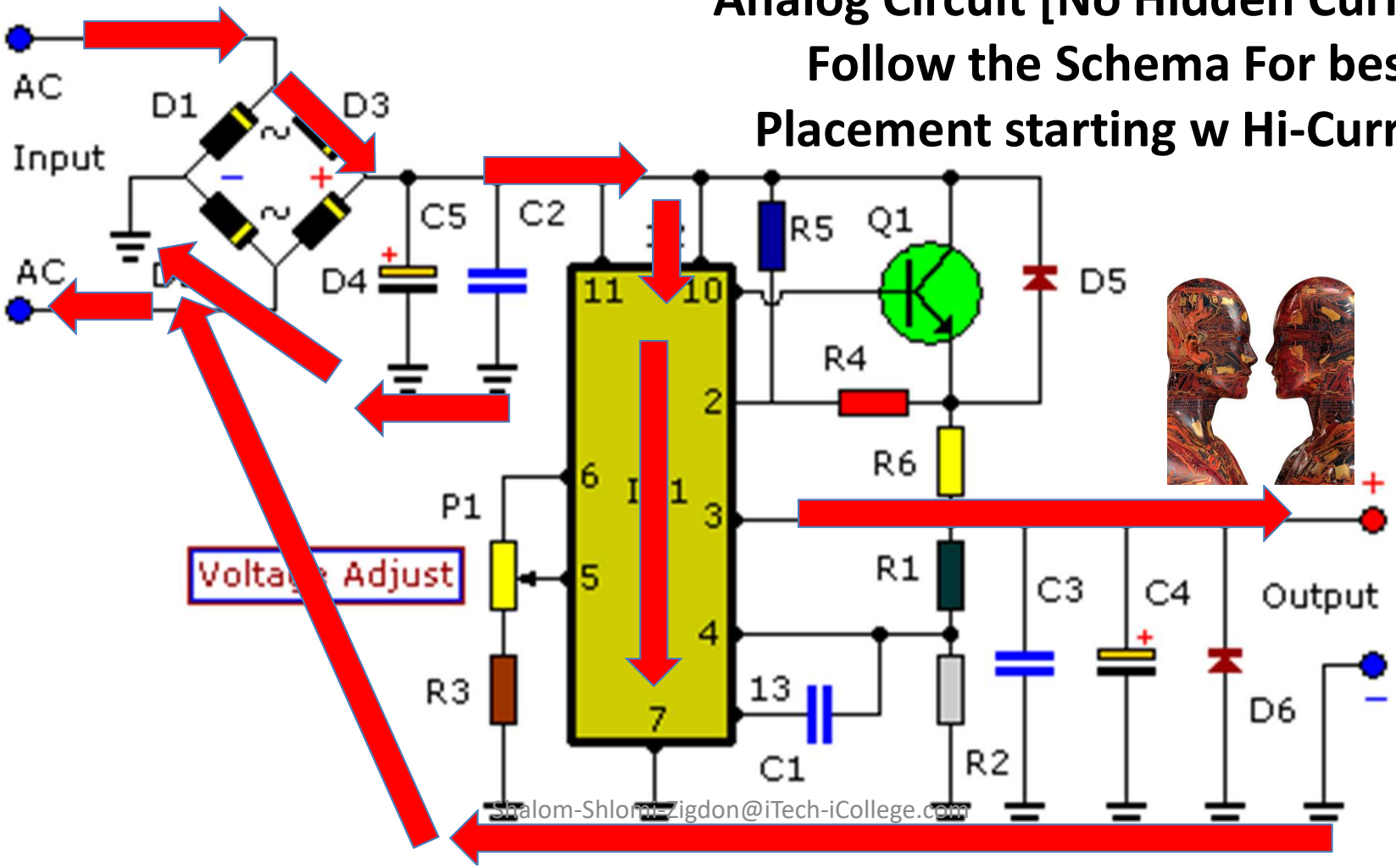


Traces Matching for DATA/Add



PLACEMENT RULES

Analog Circuit [No Hidden Currents]
Follow the Schema For best Placement starting w Hi-Current



PLACEMENT RULES – Analog Circuit

1. Identufy the Critical Path
2. Start with the High-Current Conductors, During Placement
3. Calculate width according to Current and added Temperature allowed as short as possible
4. Rout from pin to pin **WITHIN** the group on **External layers**
5. Rout **BETWEEN groups** will be done on **INNER layers**
6. Order of placement depends on number of Component pins on the Critical Path

Comparing High Current Conductors in External Layers vs. Internal Layers

IPC-2221

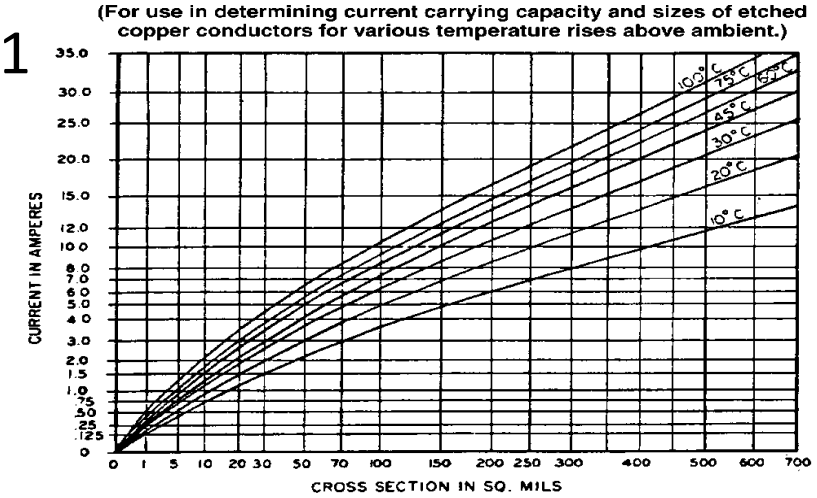


Figure A External Conductors

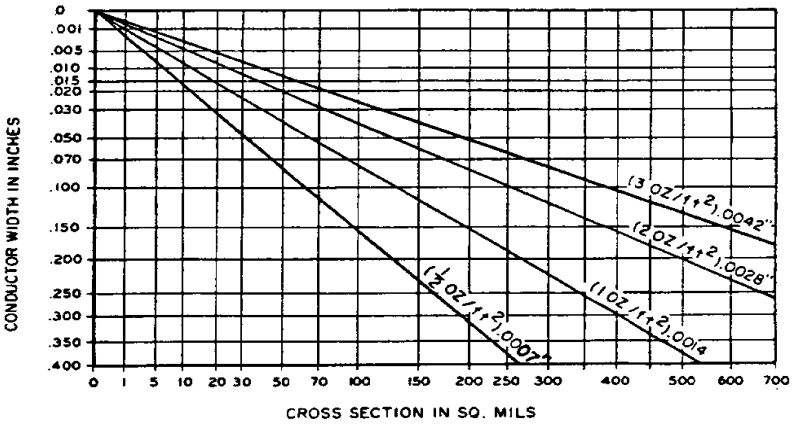


Figure B Conductor width to cross-section relationship

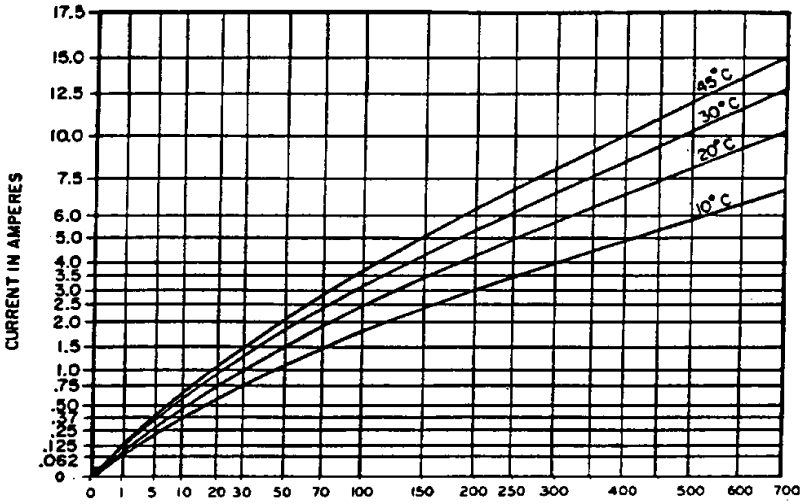


Figure C Internal Conductors

$$I = k\Delta T^{0.44} A^{0.725}$$

k = 0.048 for External traces

k = 0.024 for Internal traces

Figure B Conductor width to cross-section relationship

Current vs. Cross-Section of Conductor – External Layers

IPC-2221

Figure 6-4a

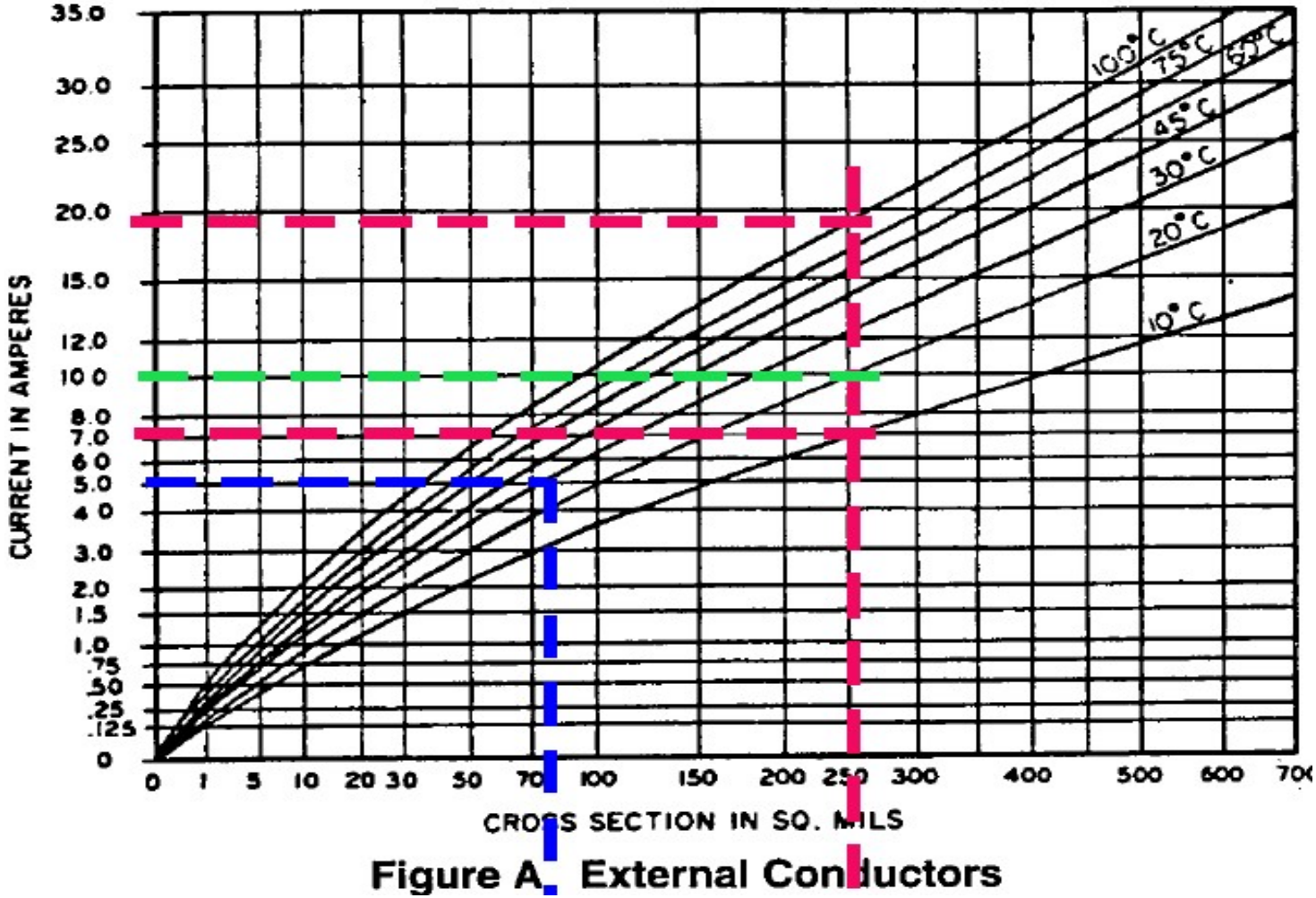
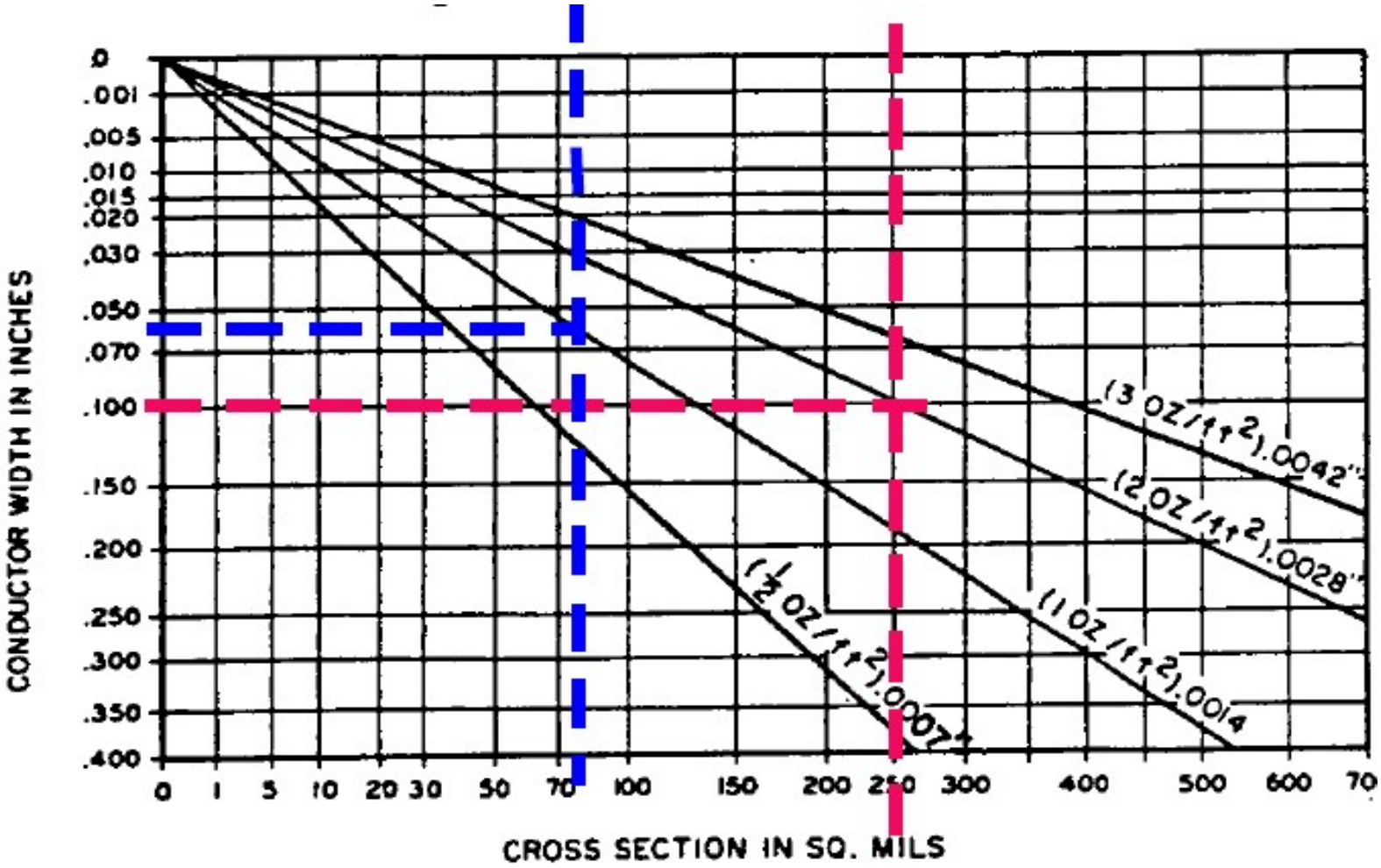


Figure A External Conductors

Conductor Width vs. Cross-Section of Conductor – External Layers

IPC-2221

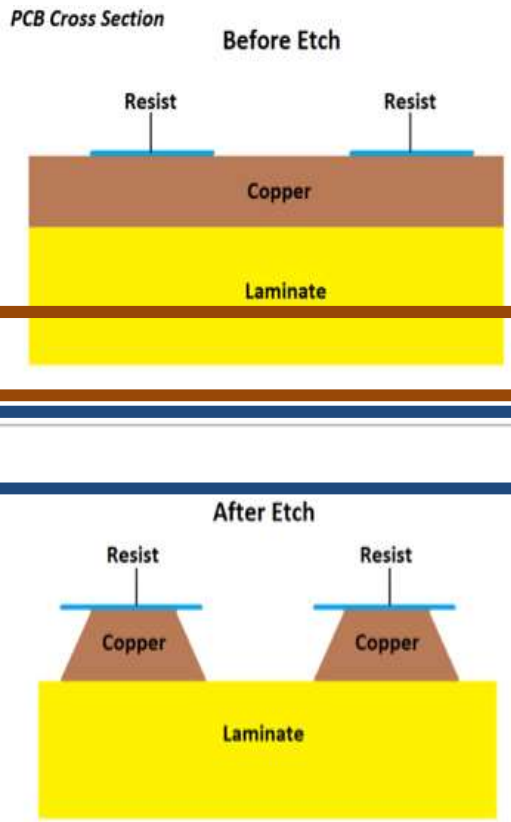
Figure 6-4b



Thicknesses After Processing Internal Layer Foil

IPC-2151

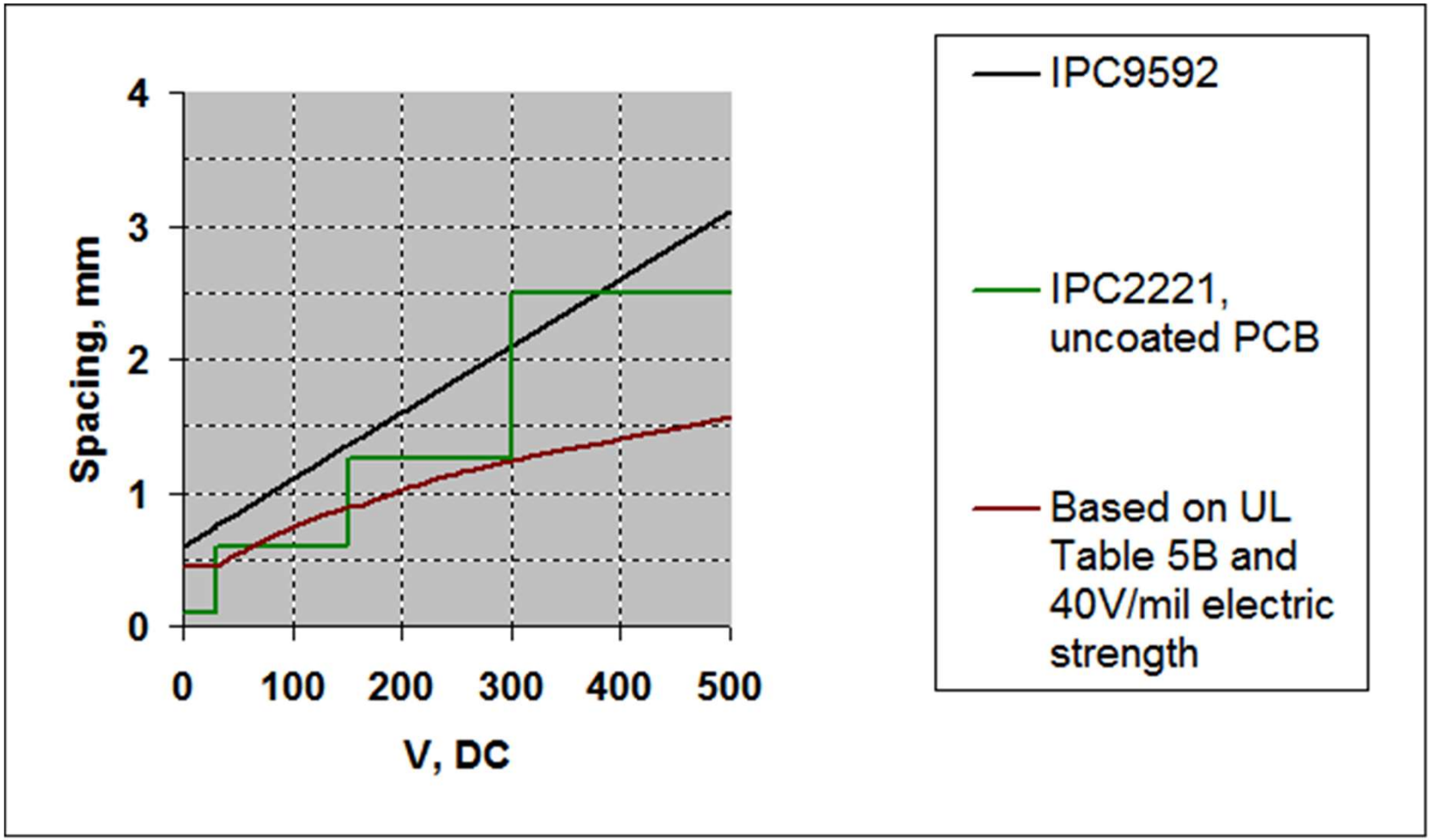
Copper Foil	Minimum	
1/8 oz	3.5 µm	0.000138 in
¼ oz	6.0 µm	0.000236 in
3/8 oz	8.0 µm	0.000315 in
½ oz	12.0 µm	0.000472 in
1 oz	25.0 µm	0.000984 in
2 oz	56.0 µm	0.002205 in
3 oz	91.0 µm	0.003583 in
4 oz	122.0 µm	0.004803 in



External Layer Foil Thickness After Plating

Copper Foil	Minimum	
1/8 oz	20 µm	0.000787
¼ oz	20 µm	0.000787
3/8 oz	25 µm	0.000984
½ oz	33 µm	0.001299
1 oz	46 µm	0.001811
2 oz	76 µm	0.002992
3 oz	107 µm	0.004213
4 oz	137 µm	0.005394

Conductors clearance vs voltage

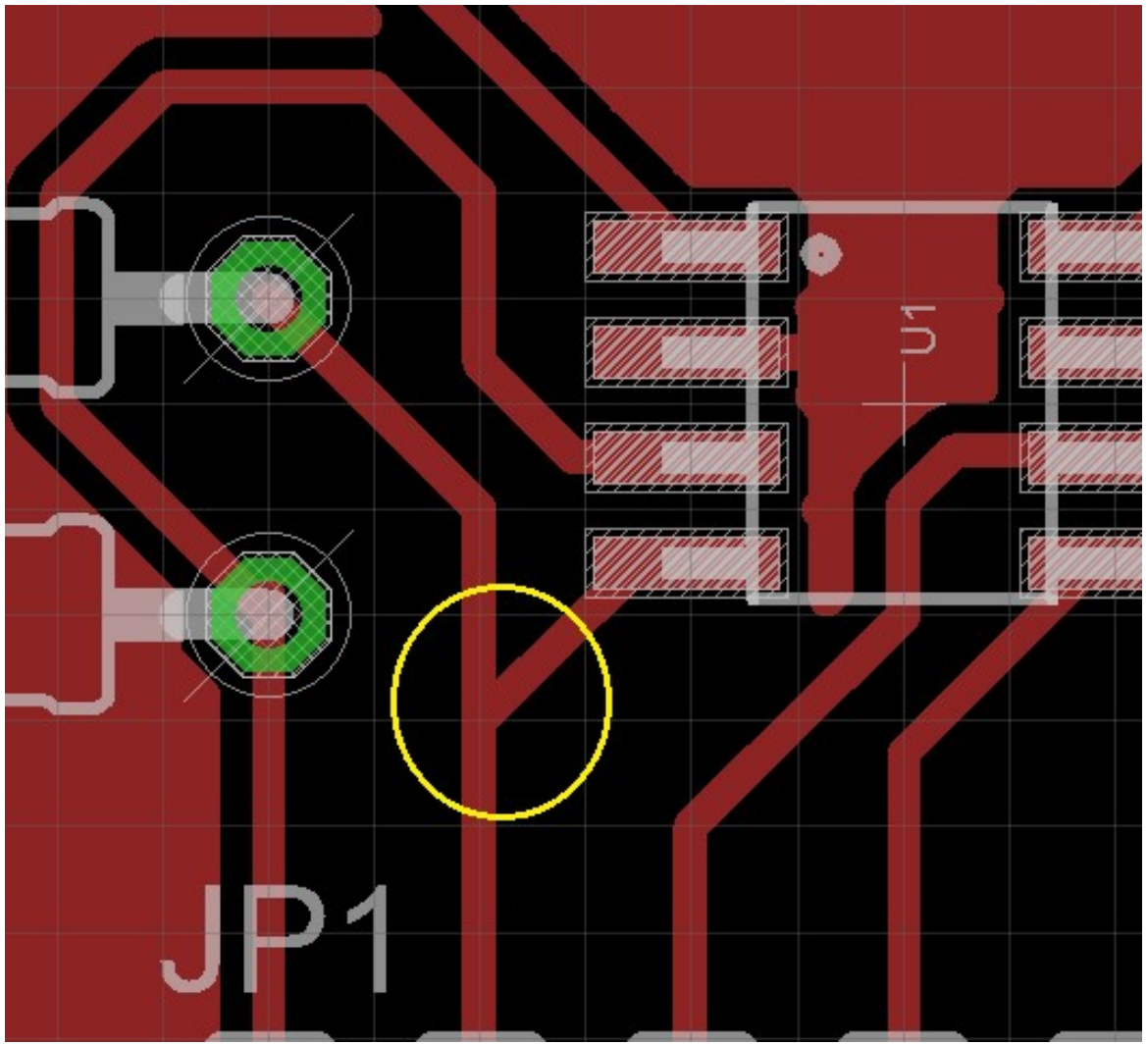


IPC-2221A

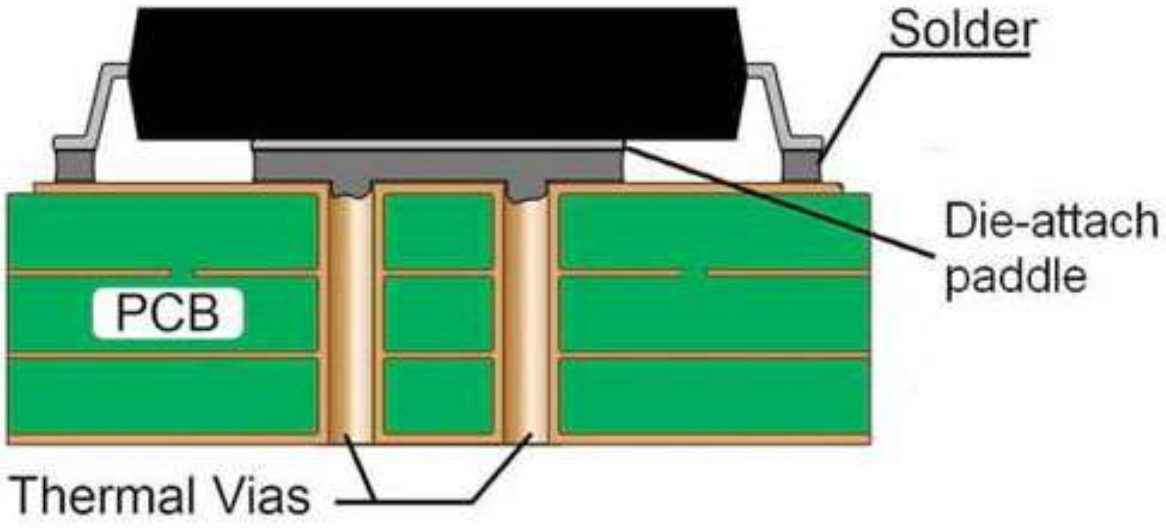
Table 6-1 Electrical Conductor Spacing

Voltage Between Conductors (DC or AC Peaks)	Minimum Spacing						
	Bare Board				Assembly		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.0197 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]
16-30	0.05 mm [0.0197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.0197 in]	0.13 mm [0.00512 in]	0.25 mm [0.00984 in]	0.13 mm [0.00512 in]
31-50	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	0.6 mm [0.024 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.4 mm [0.016 in]	0.13 mm [0.00512 in]
51-100	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	1.5 mm [0.0591 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.5 mm [0.020 in]	0.13 mm [0.00512 in]
101-150	0.2 mm [0.0079 in]	0.6 mm [0.024 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
151-170	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
171-250	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	6.4 mm [0.252 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
251-300	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	12.5 mm [0.4921 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]
301-500	0.25 mm [0.00984 in]	2.5 mm [0.0984 in]	12.5 mm [0.4921 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]	1.5 mm [0.0591 in]	0.8 mm [0.031 in]
> 500 See para. 6.3 for calc.	0.0025 mm /volt	0.005 mm /volt	0.025 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt

Acid Traps



Thermal Vias in Thermal Pad to Remove Heat



Datasheet or Mechanical or Thermal Analyzer Engineer

Mechanical Issue – Vibration Design
IPC-2221 Chapter 5

level of vibration transmitted to the board. Particular attention should be given to printed boards subjected to random vibration.

The following criteria should be used as guidelines for determining if the level of vibration to which the boards will be subjected is a level which would require complex vibration analysis of the board:

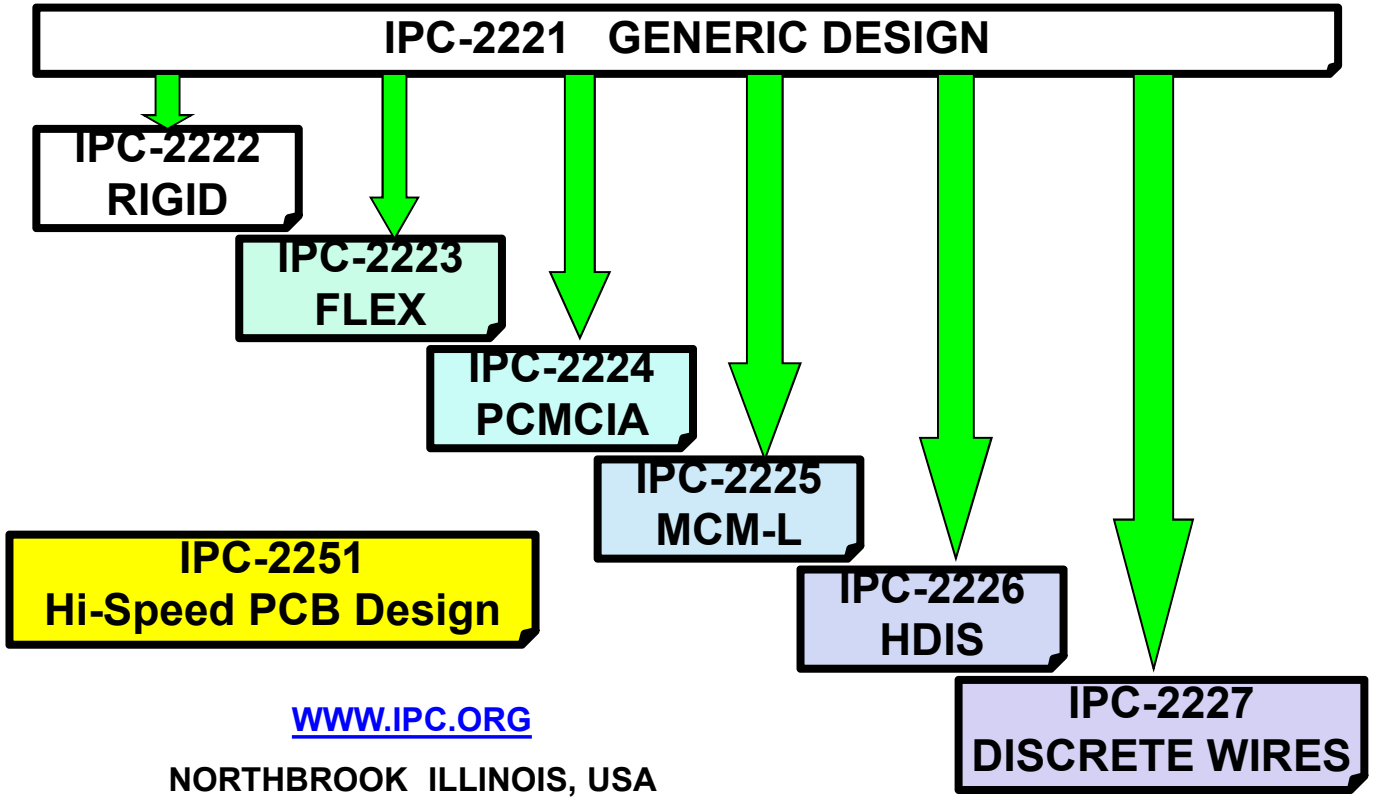
- The random spectral density is at, or above, $0.1G^2/Hz$ in the frequency range of 80 to 500 hertz or an unsupported board distance of greater than 76.2 mm.
- A sinusoidal vibration level at, or above, 3 Gs at a frequency of 80 to 500 Hz.

5.3.2 Part Support All parts weighing 5.0 gm, or more, per lead **shall** be supported by specified means (see 8.1.12), which will help ensure that their soldered joints and leads are not relied upon for mechanical strength.

The reliability of printed boards that will be subject to shock and vibration in service require consideration of the following criteria:

- The worst-case levels of shock and vibration environment for the entire structure in which the printed board assembly resides, and the ultimate level of this environment that is actually transmitted to the components on the board. (Particular attention should be given to equipment that will be subjected to random vibration.)

IPC the Institute for Interconnecting and Packaging Electronic Circuits



WWW.IPC.ORG

NORTHBROOK ILLINOIS, USA

Start with the End
Choose the PCB Manufacturer before starting PCB Layout

To get the best Layers Construction for:

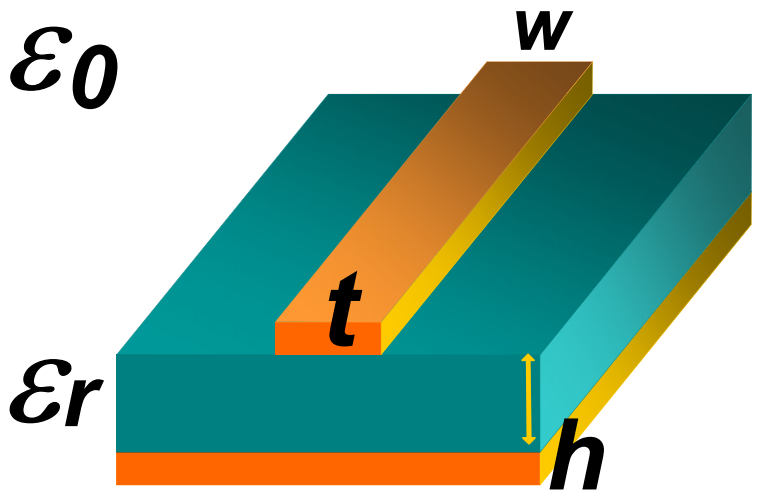
Impedance Control calculating with the **real Dielectric Constant** of the Laminates exist in **storage** Exact Dielectric Constant & Loss Tangent for each thickness of the Dielectric Core/Prepreg

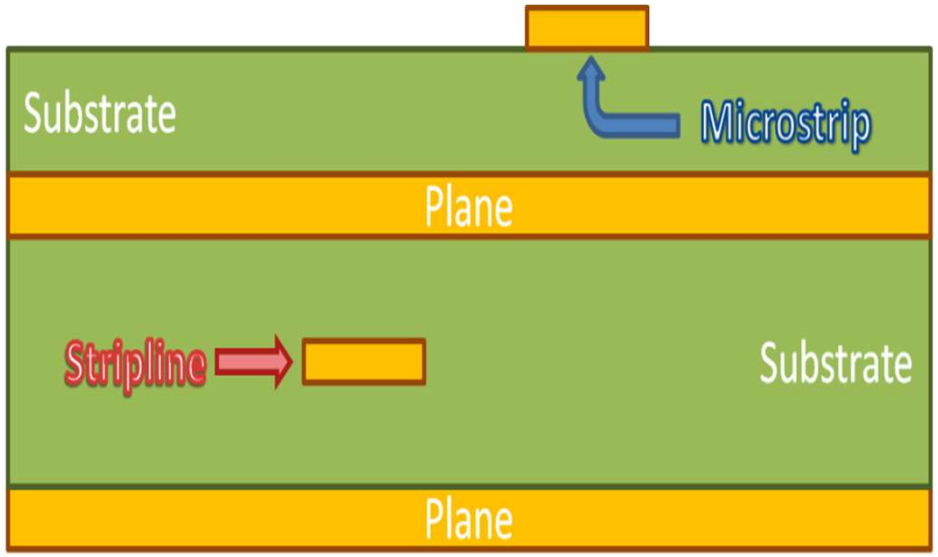
Using the minimum TH Via's diameter to improve Power Integrity

Copper Balance to eliminate disconnections pins-pads

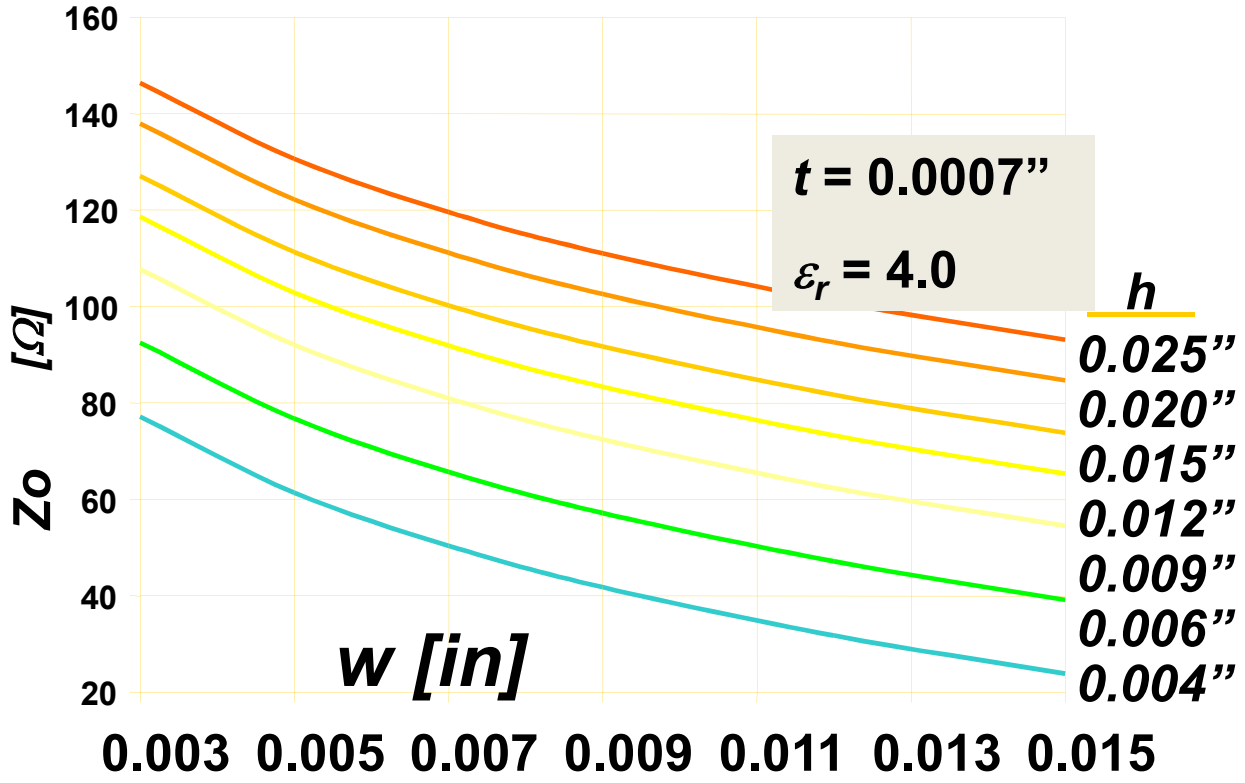
due to **Bow & Twist Effect**

The Finished Thickness influence the Impedance





$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \ [\Omega]$$

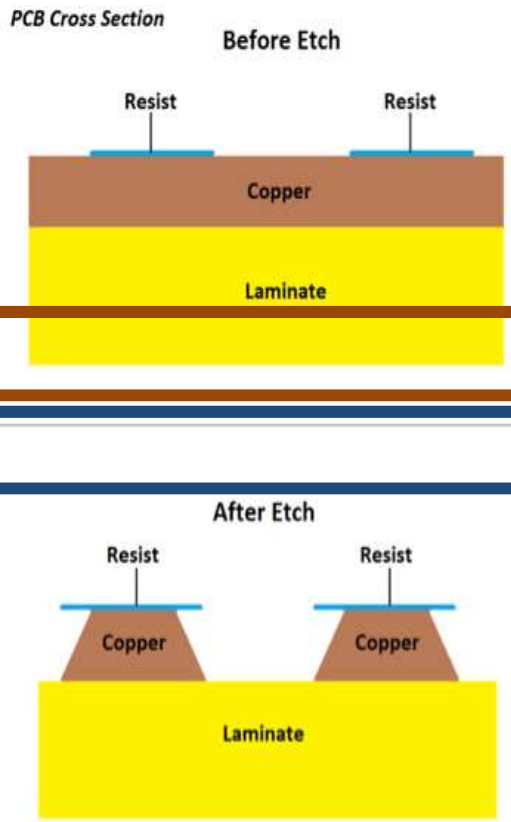


Surface Microstrip Impedance

Thicknesses After Processing Internal Layer Foil

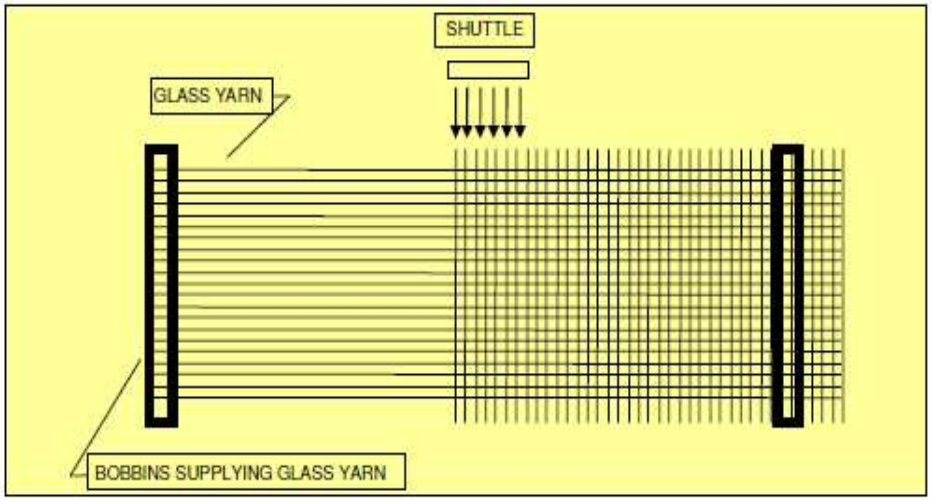
IPC-2151

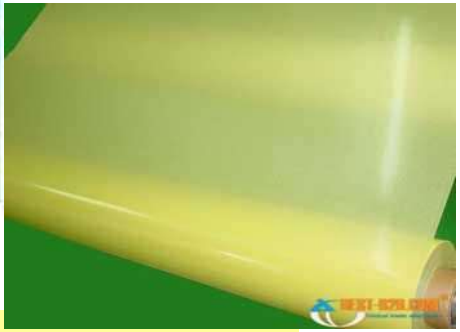
Copper Foil	Minimum	
1/8 oz	3.5 µm	0.000138 in
¼ oz	6.0 µm	0.000236 in
3/8 oz	8.0 µm	0.000315 in
½ oz	12.0 µm	0.000472 in
1 oz	25.0 µm	0.000984 in
2 oz	56.0 µm	0.002205 in
3 oz	91.0 µm	0.003583 in
4 oz	122.0 µm	0.004803 in

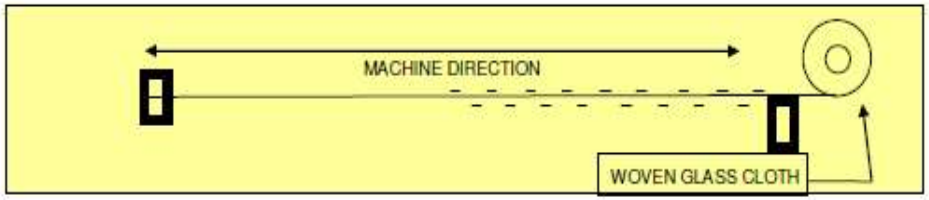


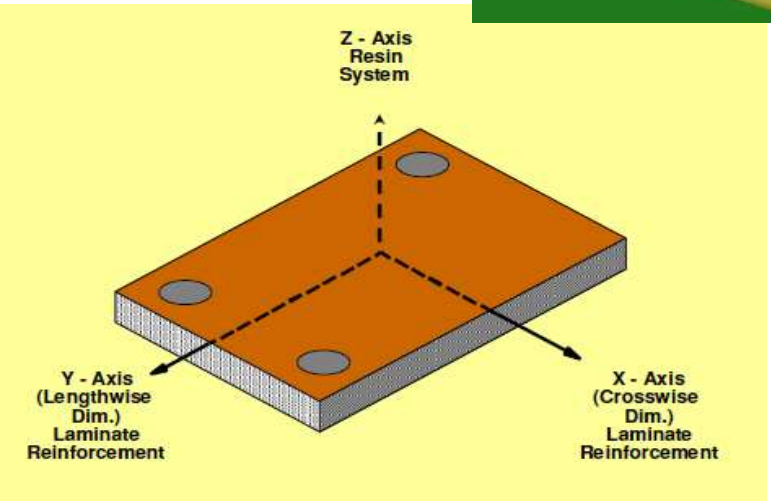
External Layer Foil Thickness After Plating

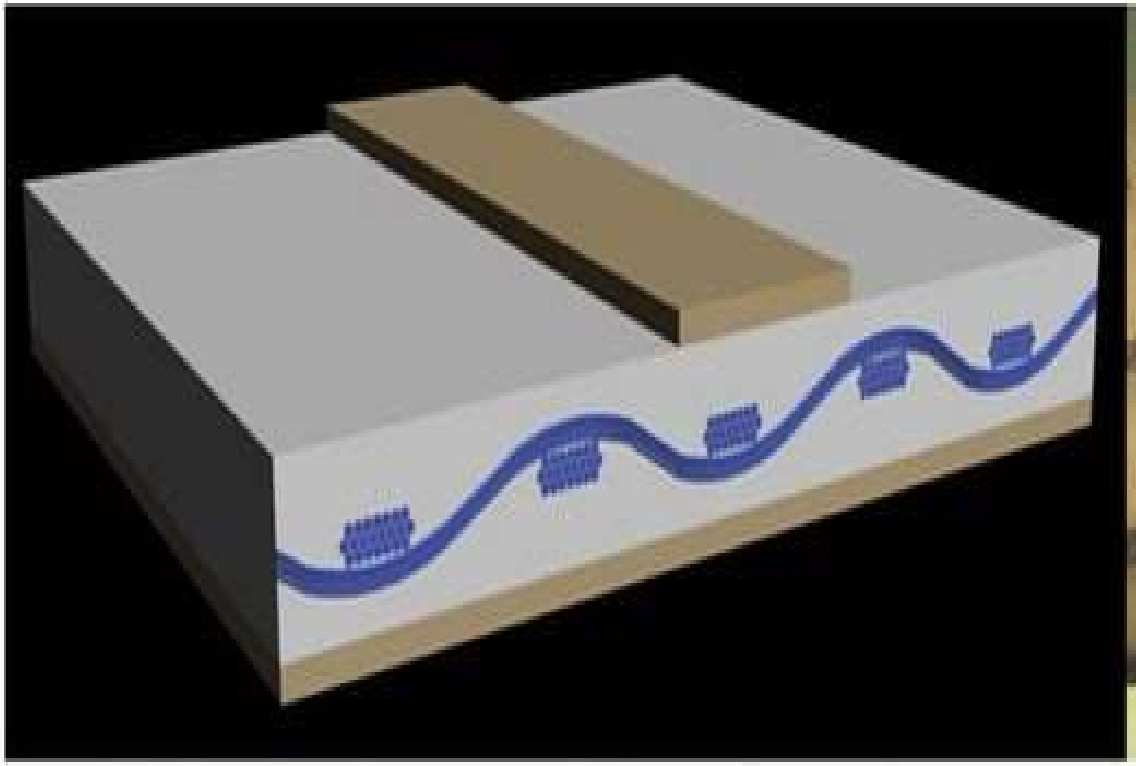
Copper Foil	Minimum	
1/8 oz	20 µm	0.000787
¼ oz	20 µm	0.000787
3/8 oz	25 µm	0.000984
½ oz	33 µm	0.001299
1 oz	46 µm	0.001811
2 oz	76 µm	0.002992
3 oz	107 µm	0.004213
4 oz	137 µm	0.005394


SHUTTLE
GLASS YARN
BOBBINS SUPPLYING GLASS YARN




MACHINE DIRECTION
WOVEN GLASS CLOTH

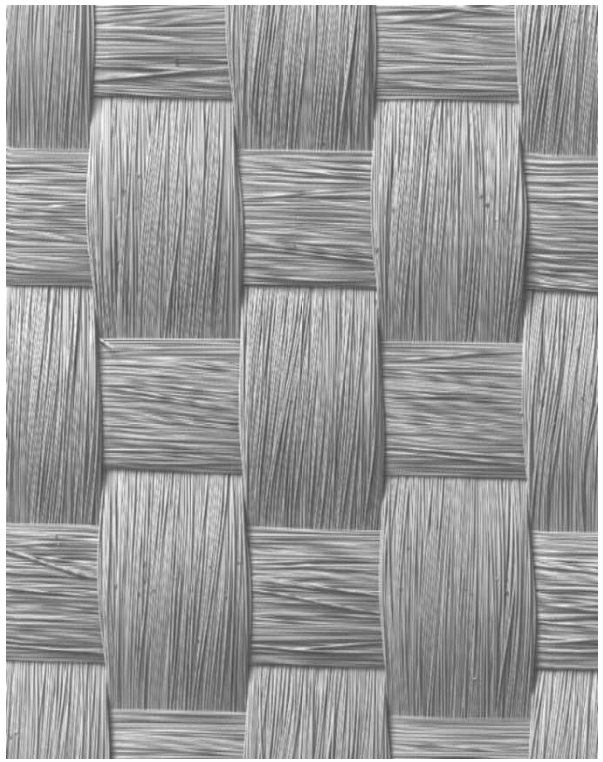

Z - Axis
Resin
System
Y - Axis
(Lengthwise
Dim.)
Laminate
Reinforcement
X - Axis
(Crosswise
Dim.)
Laminate
Reinforcement



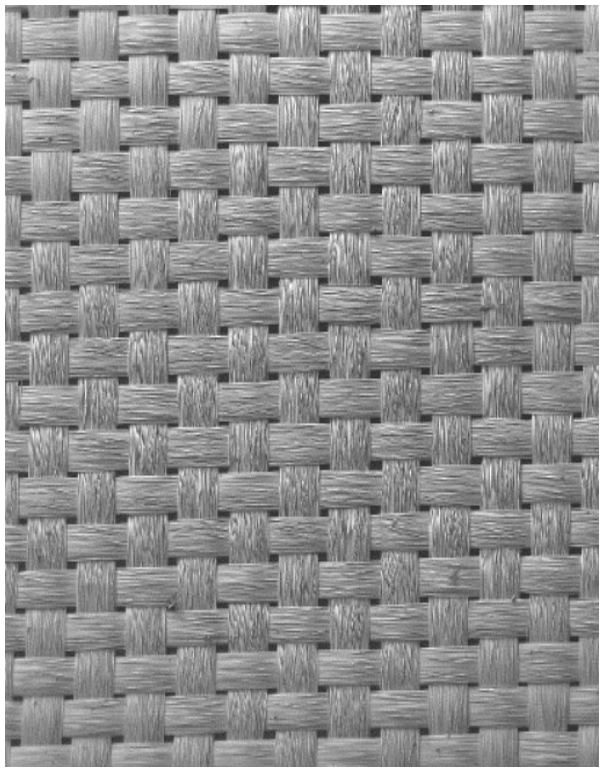
3D drawing of a microstrip transmission line

Cross-section of a microstrip

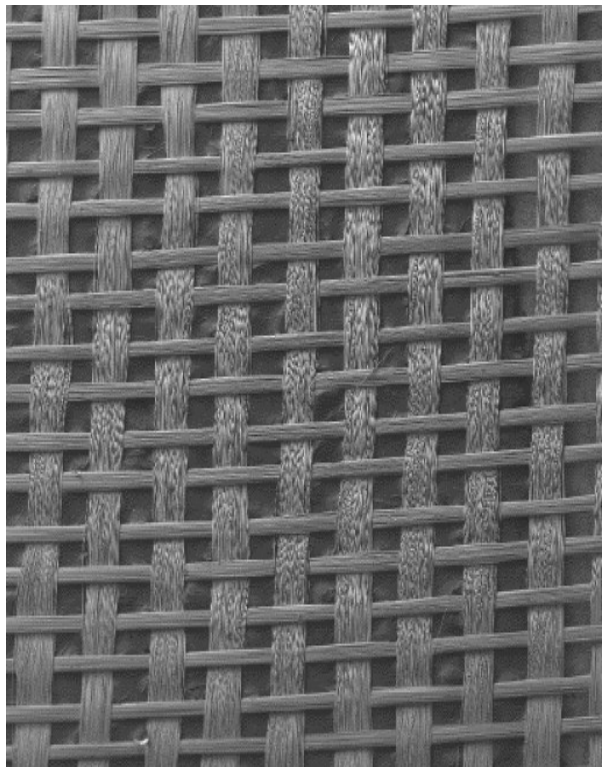
7628



2116



1080



Fiber-glass Woven types

Dielectric Material Selection

The key parameters to consider :

- the dielectric constant Dk=εr
- the loss tangent Df [Dissipation Factor]
- the glass transition temperature (Tg)
- the fiber weave characteristics
- the dielectric breakdown voltage (DBV)

Typical Dielectric Materials Used for PCB Design

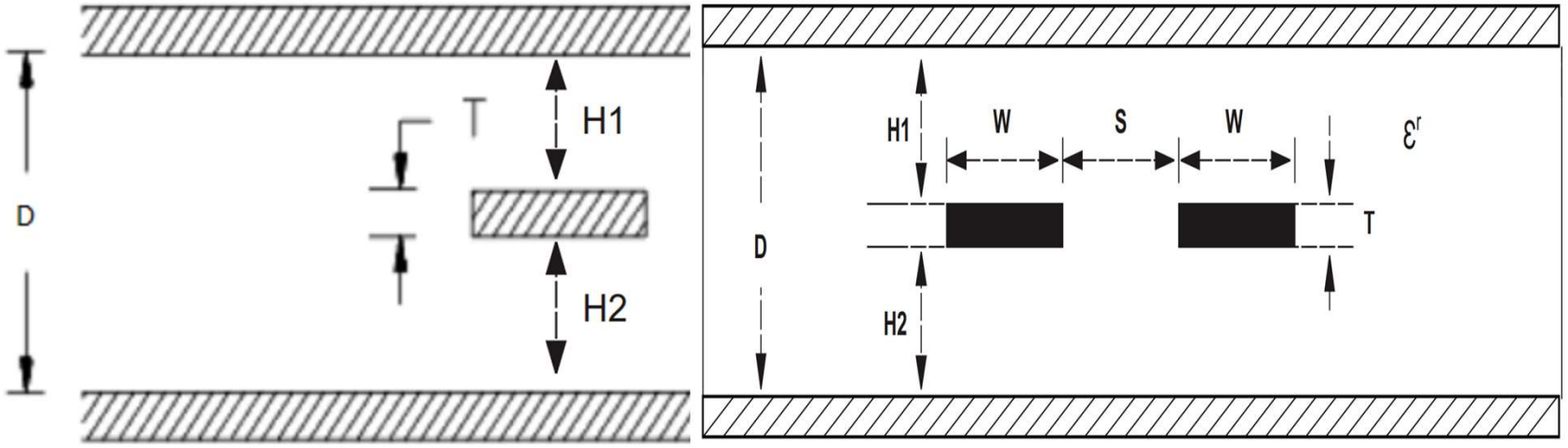
Material Name	Relative Dielectric Constant	Loss Tangent	Highest Data Sheet Frequency (GHz)
Generic FR4	4.50	0.015	N/A
Megtron 4	3.80	0.005	1
TU-872LK	3.80	0.009	10
FR408HRIS	3.37	0.0092	10
EM-888	3.80	0.008	10
EM-888K	3.20	0.006	10
Nelco N4000-13	3.70	0.008	10
Nelco N4000-13 Si	3.30	0.007	10
Megtron 6	3.63	0.004	12
Rogers 4003C	3.38	0.0027	10
Rogers 4350B	3.48	0.0037	10
Taychon 100G	3.02	0.0021	10
Megtron 7 (Low Dk Glass)	3.35	0.002	12
I-Speed	3.63	0.0071	10
I-Speed IS	3.27	0.0064	10

Example Stackup to Achieve 50Ω Single-Ended Impedance

Dielectric Material	ε_r	Trace Thickness (T)	W (mil)	D (H1+H2+T) (mil)	Single-Ended Trace Impedance (ohms)
Generic FR4	4.50	0.6	3	8.6	~50
I-Speed IS	3.27	0.6	3	7.1	~50

Example Stackup to Achieve 100Ω Differential Trace Impedance

Material	ε_r	Trace Thickness (T)	W (mil)	Spacing (S)	D (H1+H2+T) (mil	Differential Trace Impedance (ohms)
Generic FR4	4.5	0.6	3	10	8.6	~100
I-Speed IS	3.27	0.6	3	10	7.1	~100



X19516-092717

Differential Edge-Coupled Centered Stripline

Loss Tangent (Df)

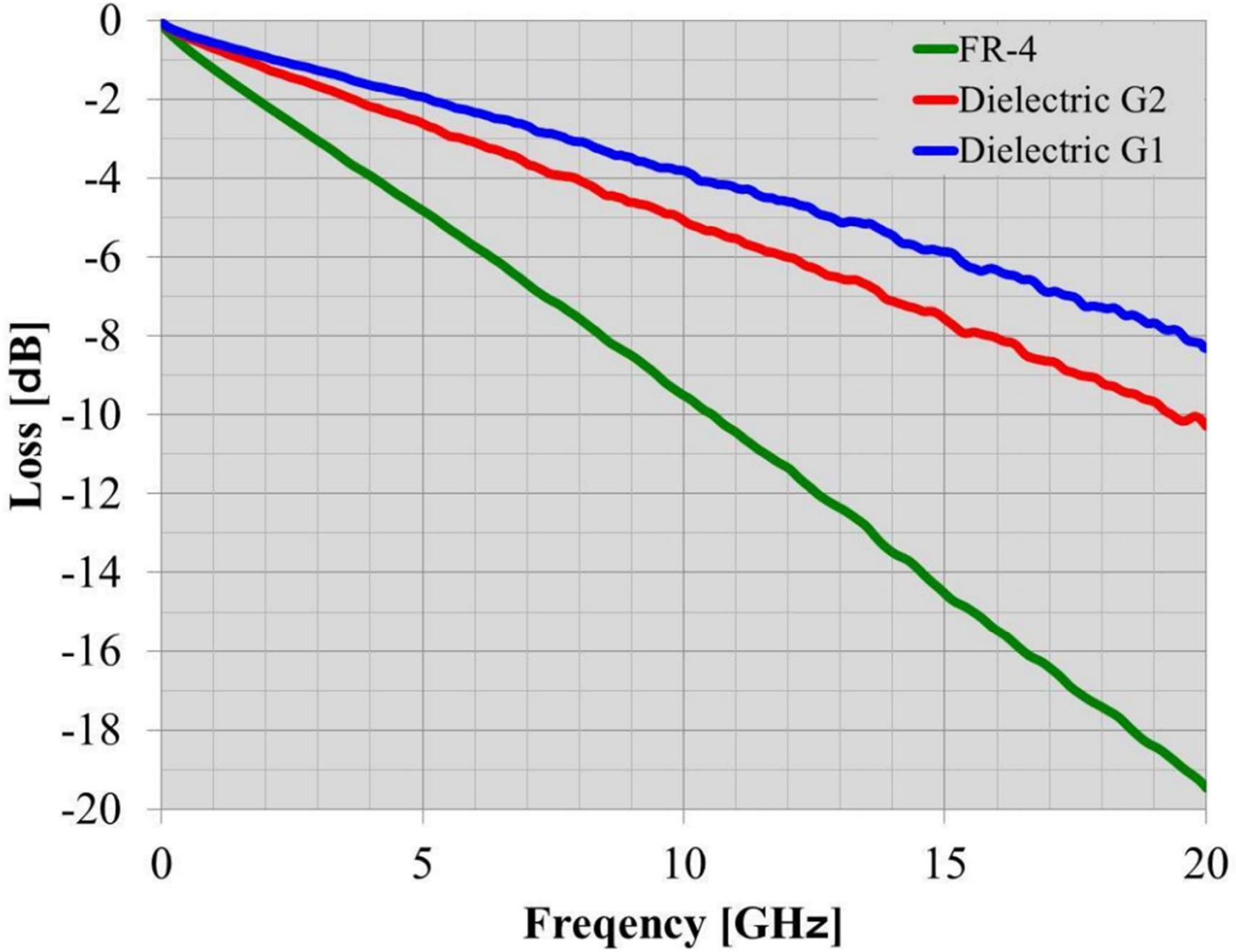
a measure of the amount of RF energy absorbed by the laminate.

The loss tangent is a combination of the resin system has & the fiberglass cloth.

Similar to Dk, the loss tangent tan(δ) or Df also varies with frequency and is dependent on the composition of the glass-to-resin ratio

$$\text{Attenuation [dB/in]} = 2.3 \times f \times Df \times \text{rsq } \varepsilon_r$$

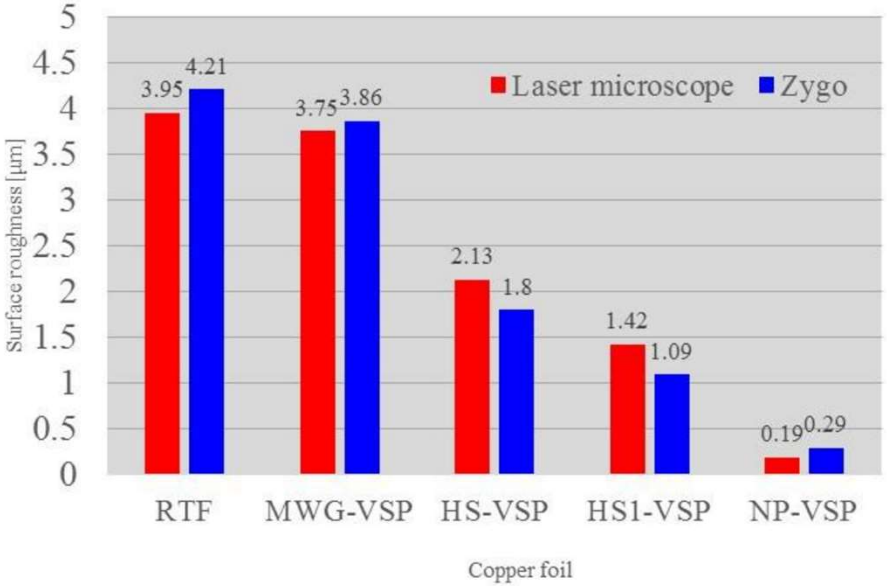
- **f is the sine wave frequency in GHz**
- **Df is the loss tangent**
- **ε_r is the relative permittivity**

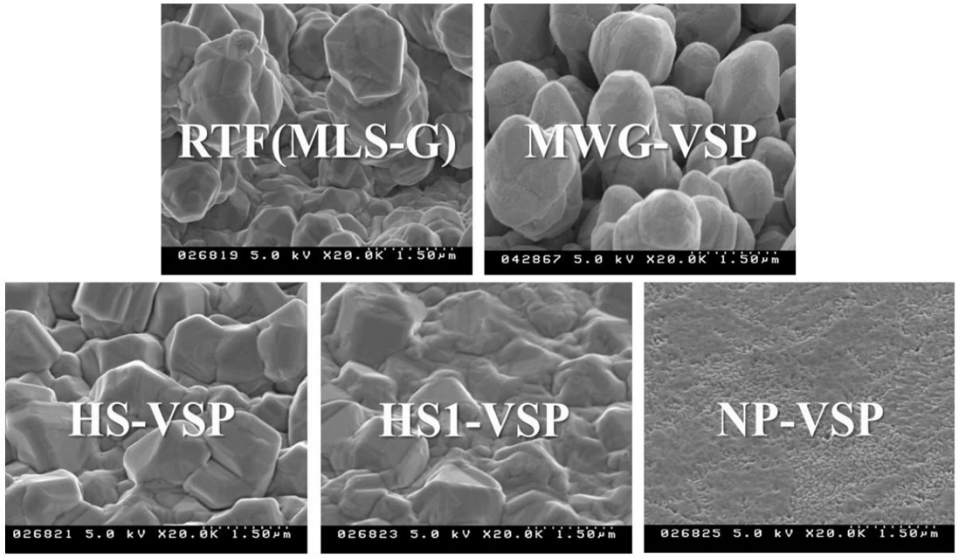

0
-2
-4
-6
-8
-10
-12
-14
-16
-18
-20
Loss [dB]
0
5
10
15
20
Freqency [GHz]
FR-4
Dielectric G2
Dielectric G1

Picking a dielectric material with low Dk and low Df is recommended for the best signal integrity

the **dielectric loss** is the **dominant** loss mechanism to be concerned with
when designing a PCB for high-speed applications.

types of copper foil – different Roughness





Roughening treatment is applied to surface of copper foils by depositing copper nodules

Tg Glass Transition Temperature

the **temperature** at which a **resin's CTE** [coefficient of thermal expansion] changes to a much larger value than it has at lower temperatures.

The Z-Axis CTE is 4 times the x/y-Axis CTE

PCB with 14+ Layers >>>> De-Lamination [popcorn]

IPC-2221

Environmental Property	Material					
	FR-4 (Epoxy E-glass)	Multifunctional Epoxy (E-glass)	High Performance Epoxy (E-glass)	Bismalaimide Triazine/ Epoxy	Polyimide (E-glass)	Cyanate Ester
Thermal Expansion xy-plane (ppm/°C)	16 - 19	14 - 18	14 - 18	~15	8 - 18	~15
Thermal Expansion z-axis below T_g[3] (ppm/°C)	50 - 85	44 - 80	~44	~70	35 - 70	81
Glass Transition Temp. T_g (°C)	110 - 140	130 -160	165 - 190	175 - 200	220 - 280	180 - 260
Flexural Modulus (x 10^{10} Pa)						
Fill[1]	1.86	1.86	1.93	2.07	2.69	2.07
Warp[2]	1.20	2.07	2.20	2.41	2.89	2.20
Tensile Strength (x 10^8 Pa)						
Fill[1]	4.13	4.13	4.13	3.93	4.82	3.45
Warp[2]	4.82	4.48	5.24	4.27	5.51	4.13

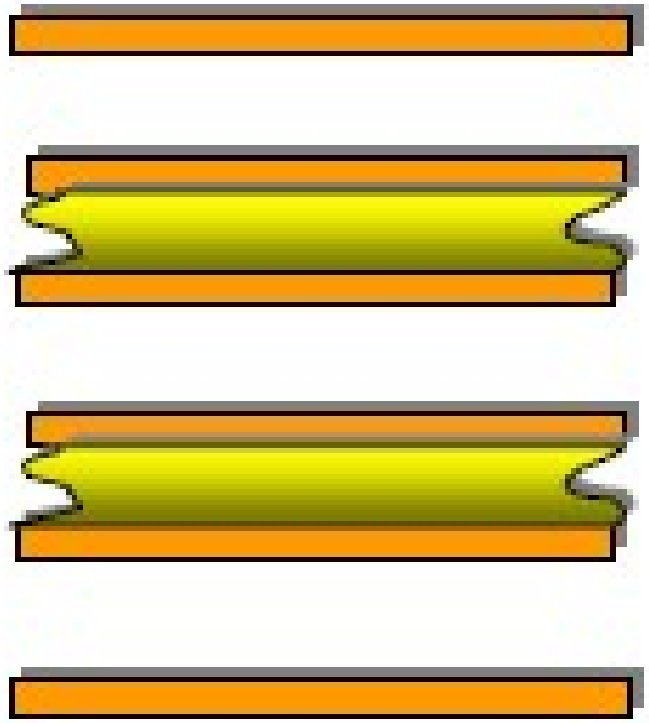
[1] Fill - yarns that are woven in a crosswise direction of the fabric.
[2] Warp (cloth) - yarns that are woven in the lengthwise direction of the fabric.
[3] Z-axis expansion above T_g can be as much as four times greater. For FR-4 it is 240-390 ppm. Contact supplier for specific values of the other materials.

Layers Construction

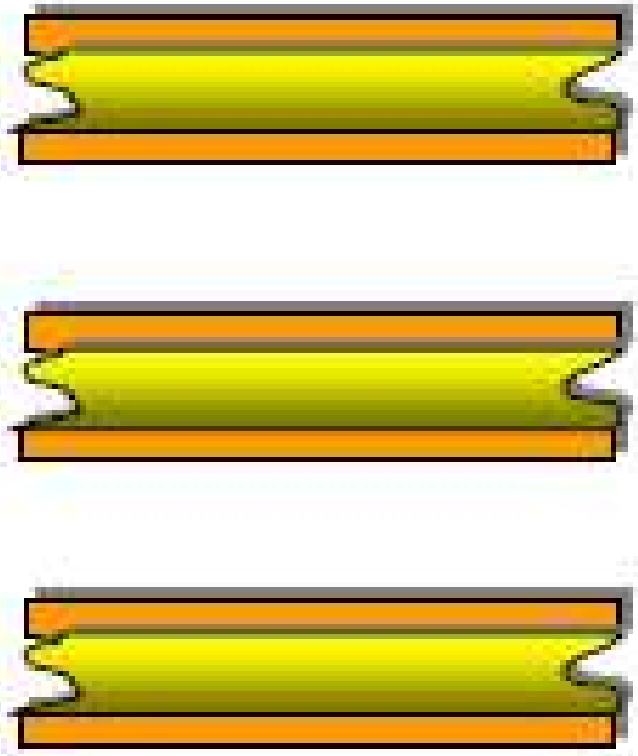
- Manufacturer recommendation PCB Layers Construction is very real Design
- Impedance calculation calculated with the real PCB Materials in storage
- Exact Dielectric Constant, Loss Tangent for each thickness of the Dielectric Cores/Prepreg

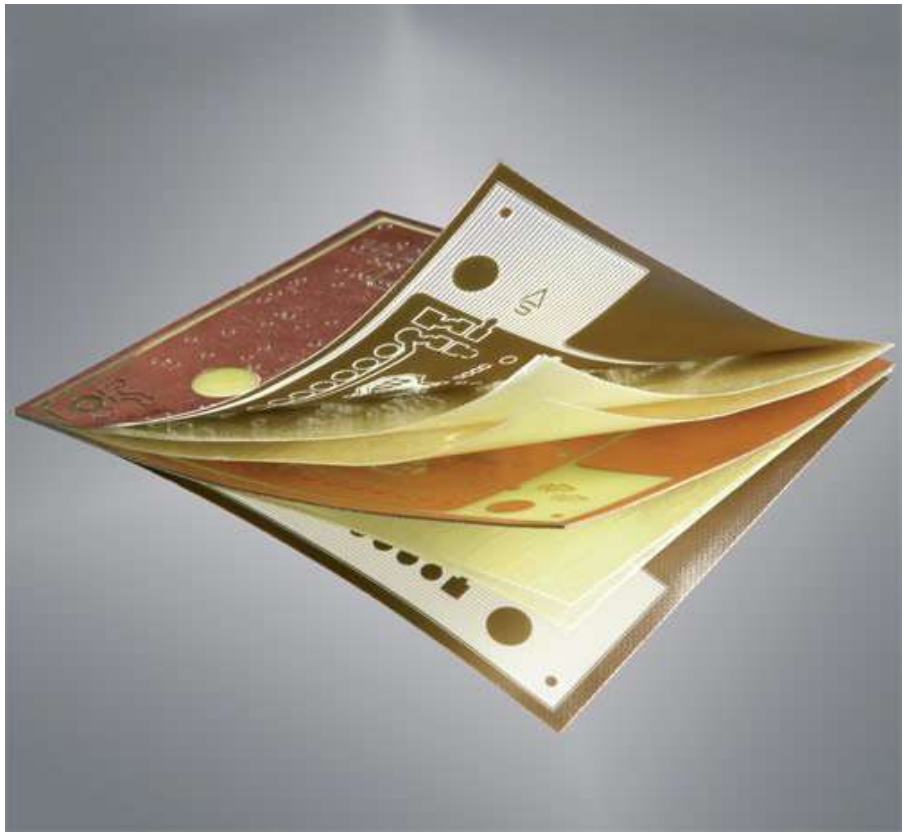
Foil vs Core Construction

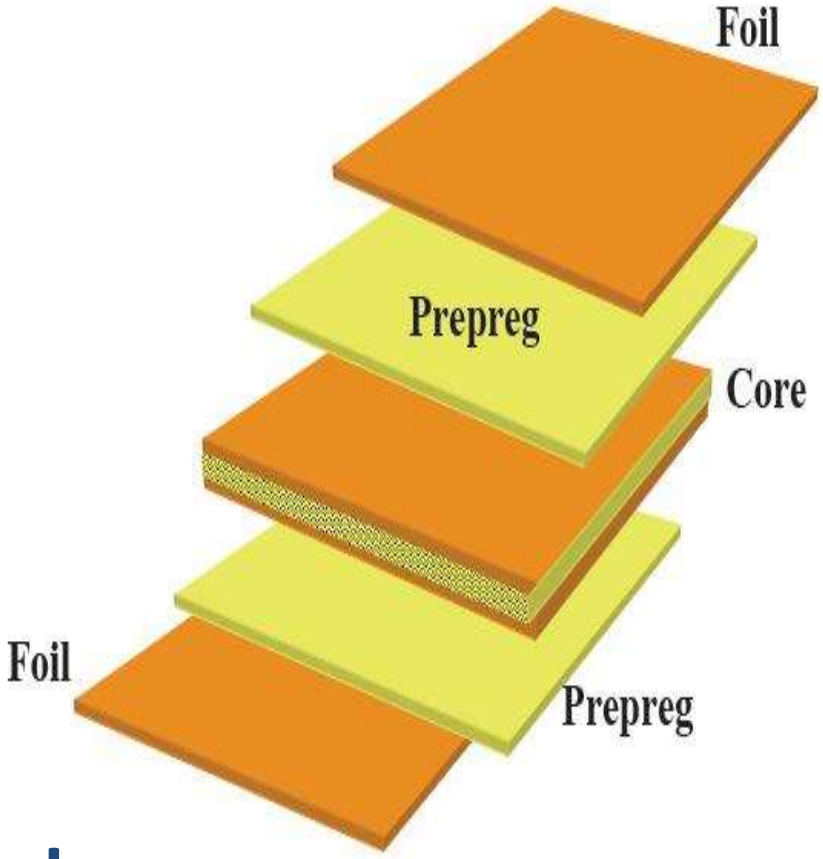
Foil Construction



Core Construction



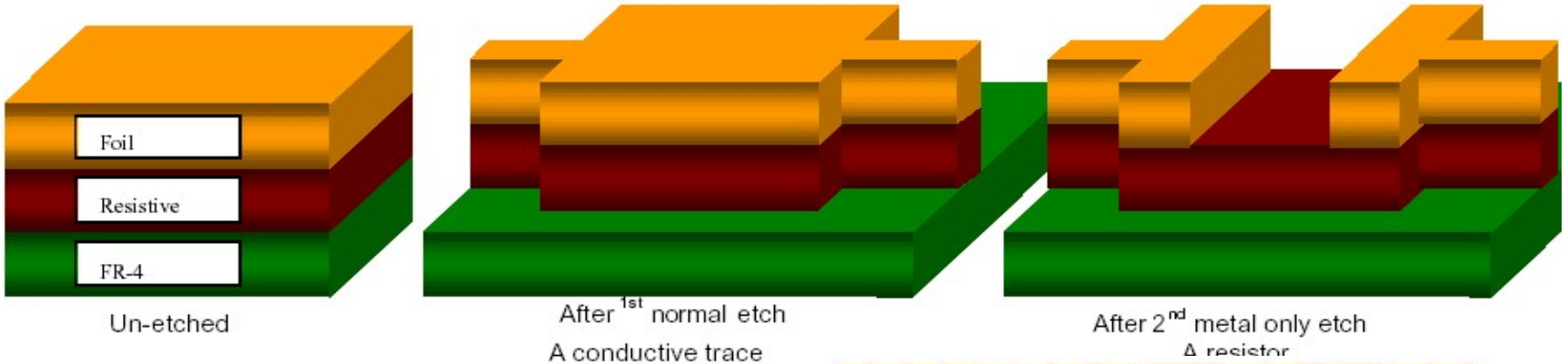


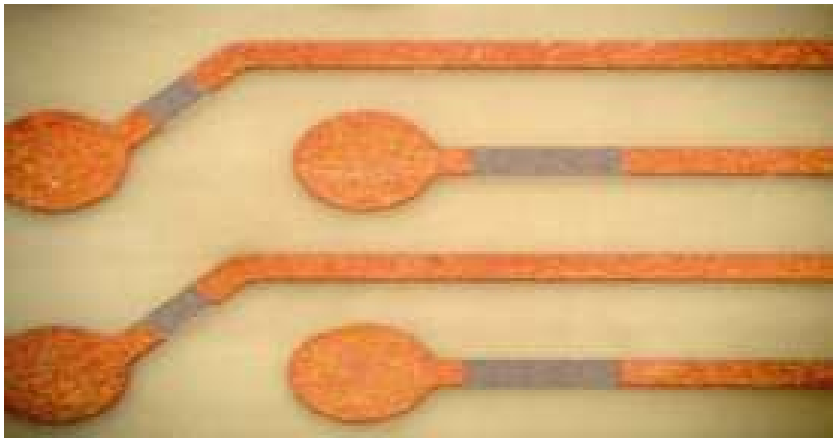


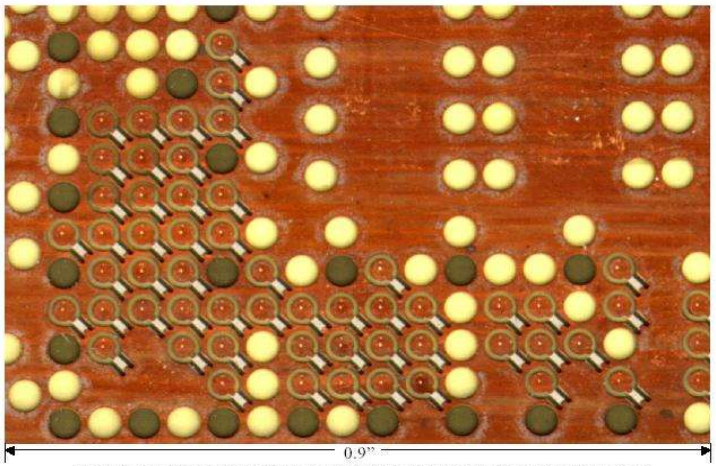
Conclusion – Start with the End

Get advice from your Manufacturer before PCB Layout

Embedded Resistors use as Terminations



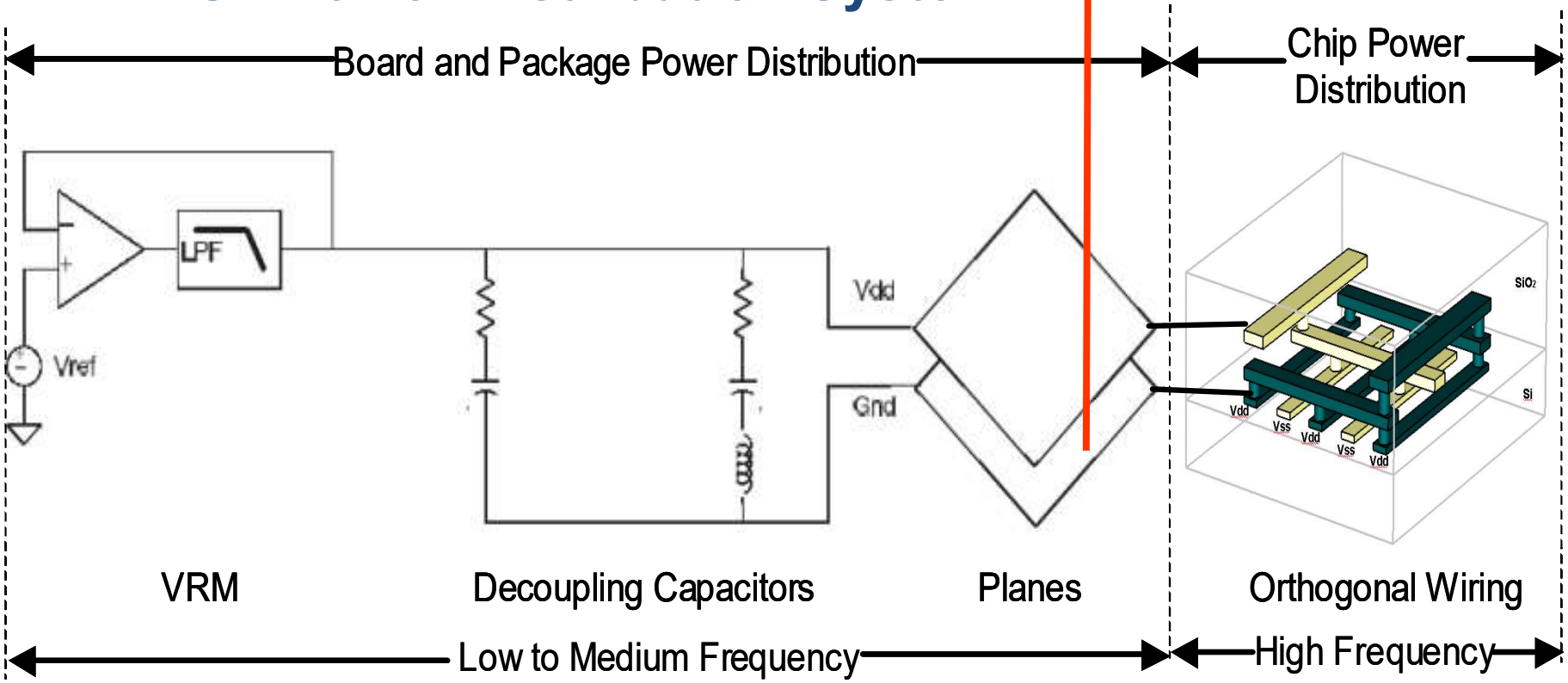




BURIED RESISTOR APPLICATION-TERMINATION UNDER BGA PACKAGE FOR SERVER

Package & Board ⟵ | ⟶ Chip

PDS= Power Distribution System



Voltage Regulator Module

Make a decision which is preferred for this PCB

Signal Integrity vs. Power Integrity

Conflicts

Diameter of Vias

Larger vs. Smaller

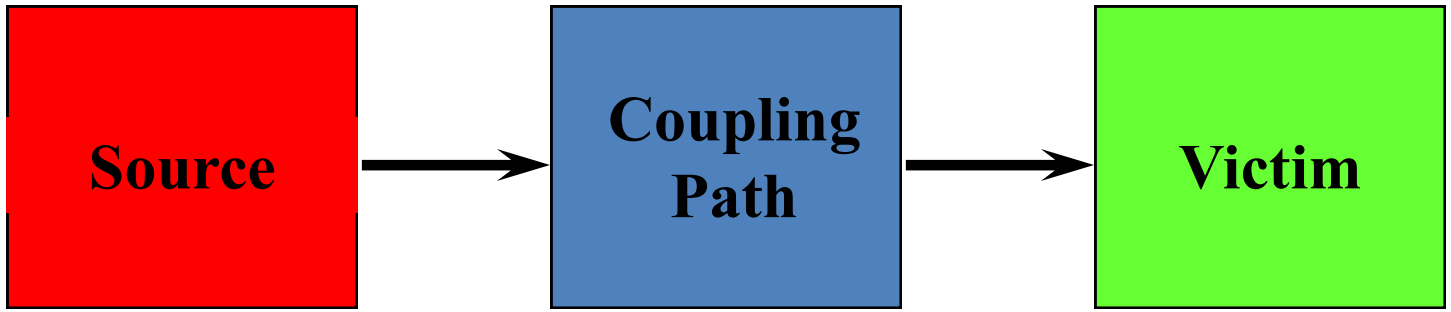
minimize Via Inductive reduce Power planes self Inductance

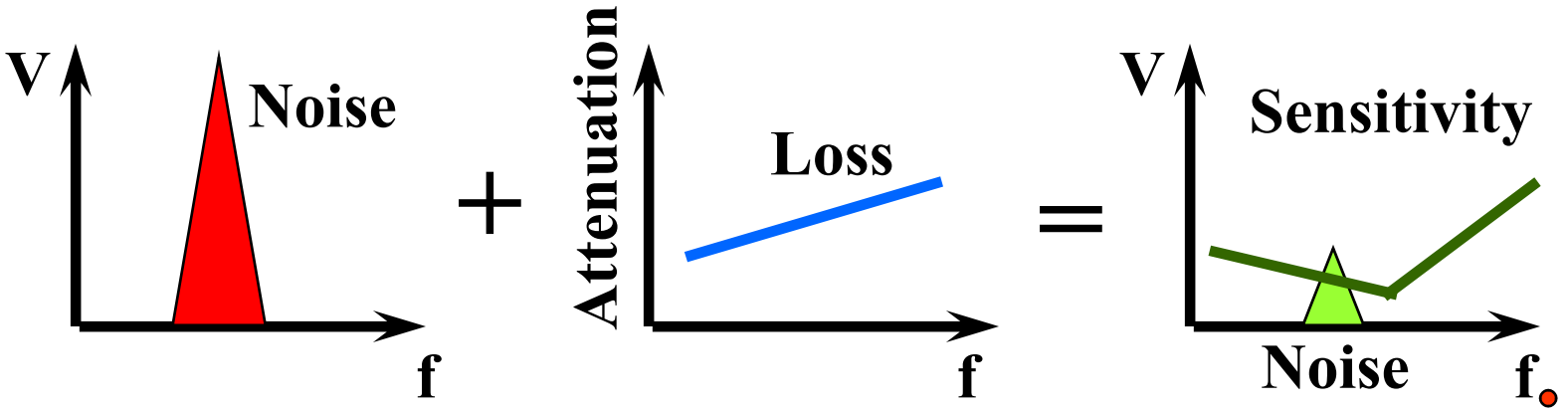
PCB Layout Design for EMC Compliance

to reduce the cost and the time for EMC requirements

[Mil-Std-461, FCC, EN/CE Directive]

EMI Building Blocks





Interference Modes in electronics

1. Intra System-Inside the unit

2. Inter System – to and from the environment

- Sources of High Frequency radiation:
  - Digital electronics, especially clocks
  - local oscillators of receivers
  - spurious emissions from transmitters
  - switching operations
  - switching Mode Power supplies-SMPS
- High frequency radiating elements
  - PCB Traces
  - Return Current Path Loops
  - Cables
  - Antennas

EMI Main Consideration

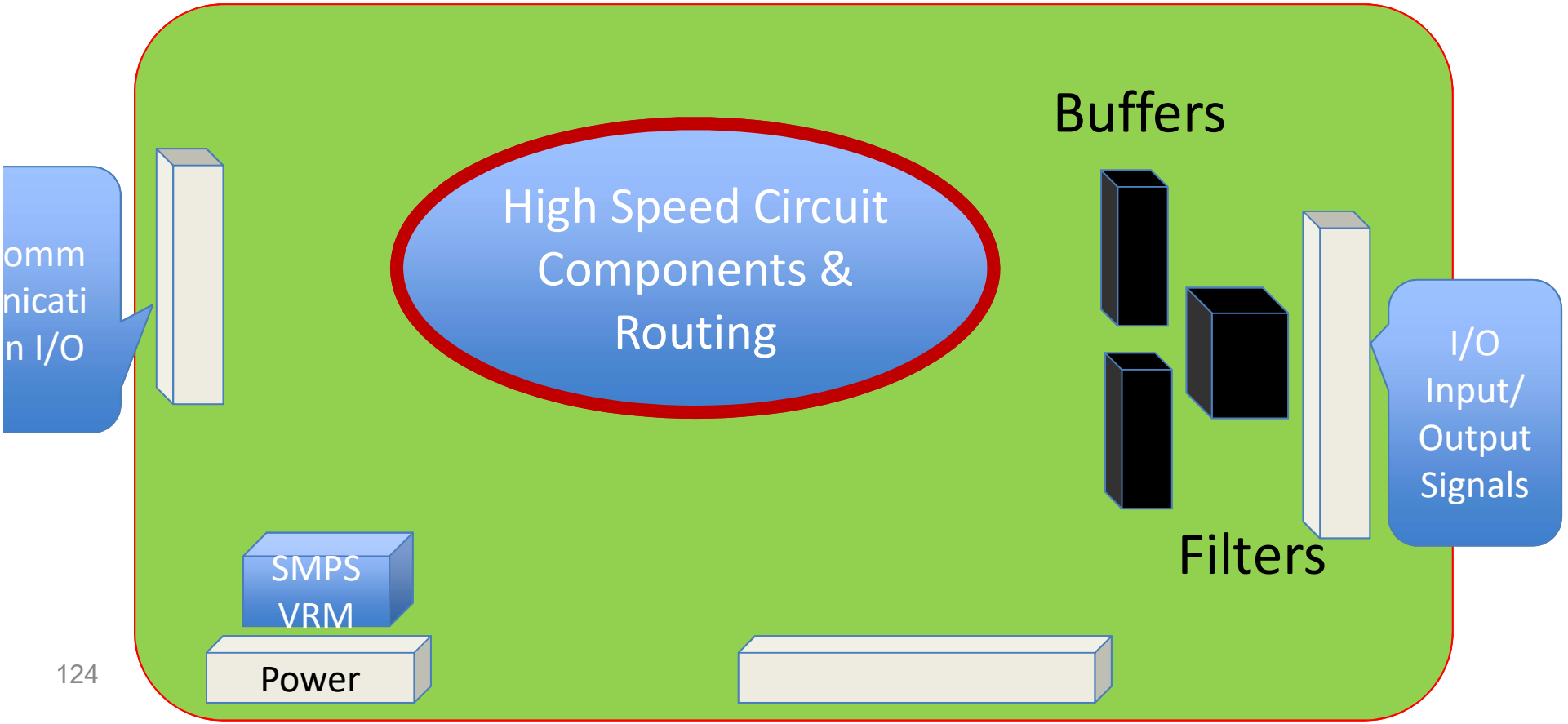
PCB Layout

1. Signal + Current Return Loop Area
2. High Current Loop Area
3. Impedance Control
4. Signal Termination
5. Decoupling/Bypassing Capacitor
6. Power Distribution
7. Grounding
8. Surge Suppression

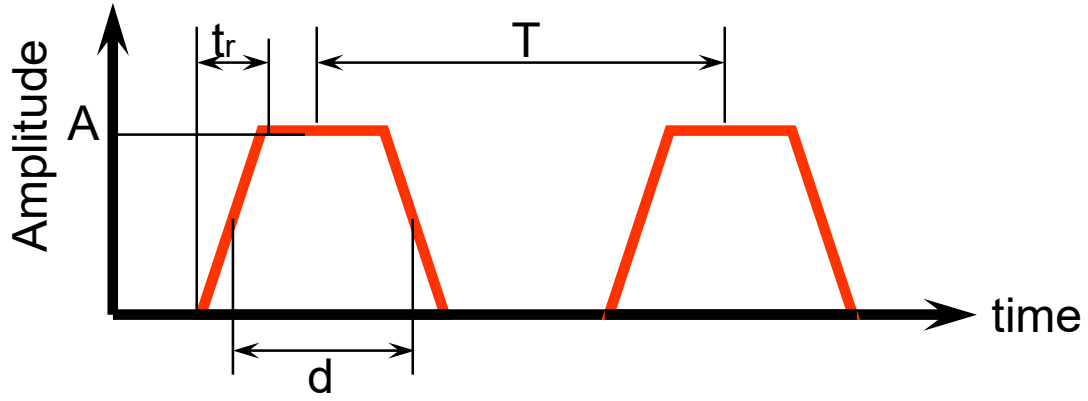
System Level

1. Filtering
2. Cabling
3. Shielding
4. Bonding

Placement for EMC Control



Spectrum of a Clock Pulse Train

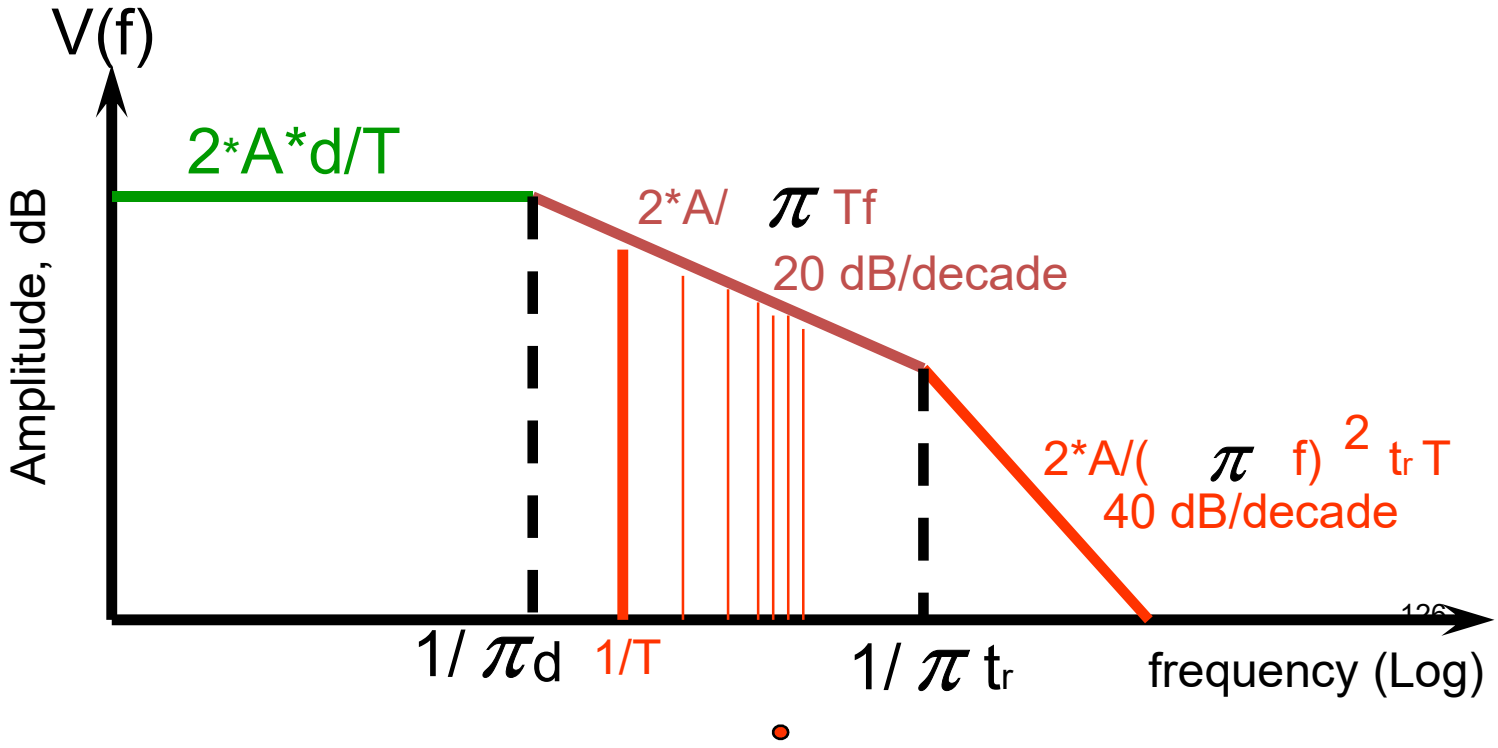


$$v(f)=\frac{A\cdot d}{T}+\frac{2\cdot A\cdot d}{T}*\sum_{n=1,2,3}\frac{\sin\left(n\cdot\pi\cdot d/T\right)}{n\cdot\pi\cdot d/T}\cdot\frac{\sin\left(n\cdot\pi\cdot t/T\right)}{n\cdot\pi\cdot t/T}$$

125

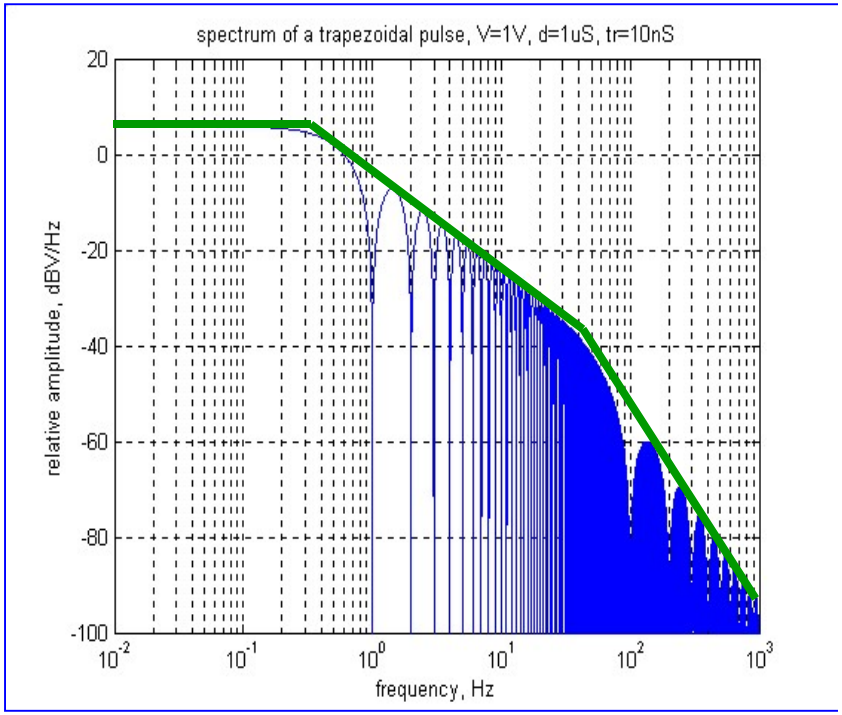
Fourier series of discrete frequencies

Spectrum of a Clock Pulse Train



Pulse Spectra

- Pulse spectra can be described by 3 segments in the Log Amplitude and Frequency plane:
  - Low frequency, up to f_1, determined by d
  - Medium frequency, up to f_2 , determined by t_r
  - High frequency, above f_2
- Clock spectra contains clock harmonics



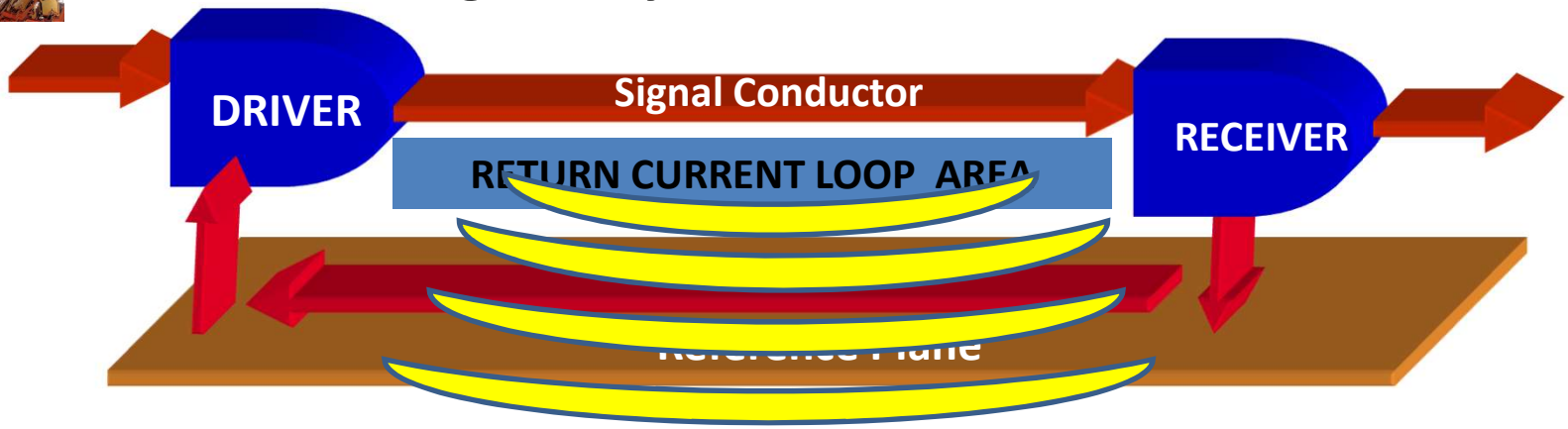
127

Any loop Generates Radiation – "Antenna"

$$E_{(V/m)} = 1.3 f^2_{(MHz)} * A_{(cm^2)} * \frac{I_{(amps)}}{R_{(meters)}}$$

Minimize the dielectric thickness between

Signal Layers and Power Planes



Wide Conductor Advantages

Greater Characteristic Capacitance to GND Plane

Minimize Characteristic Impedance

Minimize self inductance of the conductor

Minimize EMI radiation

Minimize Crosstalk by mutual Inductance between conductors

Minimize conductor Resistance [a must for 10Gbps]

Noisy Circuit

place in the middle of PCB noisy/susceptible components Away from any I/O Connectors and Power Supply Circuits.

- uP, uC, FPGA
- Oscillators
- Crystal
- Clock Dividers
- Data & Address Busses
- SWPS Switching Mode Power Supply
- Transformators, Common Mode Chockes
- Non-grounded Heatsinks

Away from Sensitive Analog Circuits [microvolt – millivolt inputs from Sensors]

OP-AMP [operational amplifiers]

1. I/O Signals are Paths of EMI off The PCB
2. Avoid routing High Speed Signals beneath I/O Components
3. Ground any Heatsink to prevent Radiation of Coupled Fields

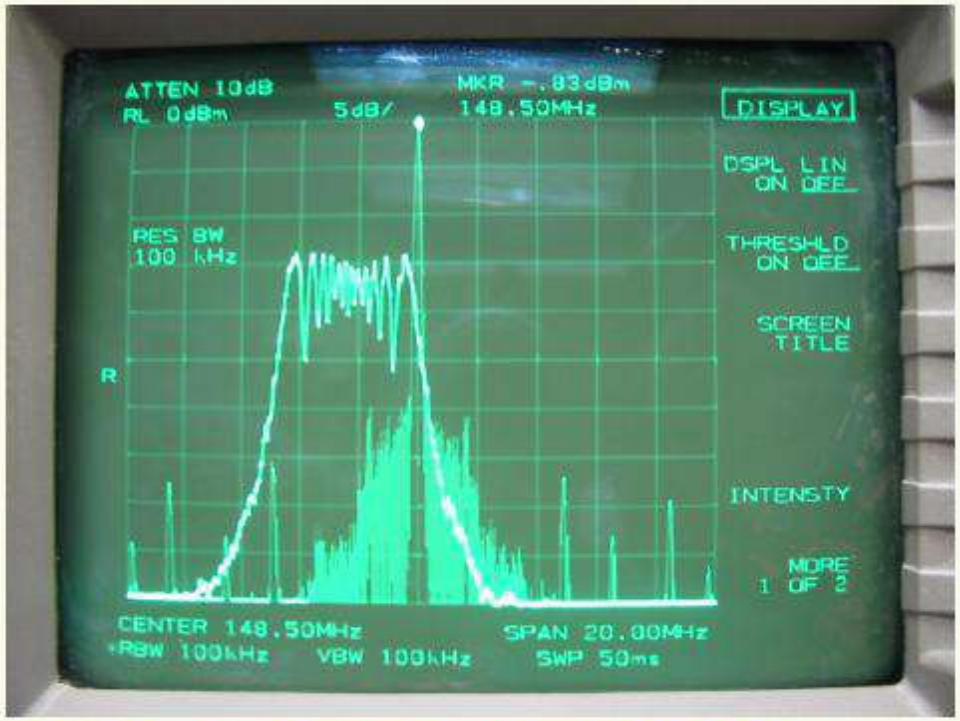
Summary of Control of Radiation Traces

- **Keep Area of radiating antenna small**
  - Place differential wires together, and twist.
  - place wires close to ground plane.
  - keep lengths short.
- **Limit High Frequency Noise Voltage and Current**
  - Use low current devices
  - Long rise/fall times.
  - low pass filtering.

Spread Spectrum Clock Generator

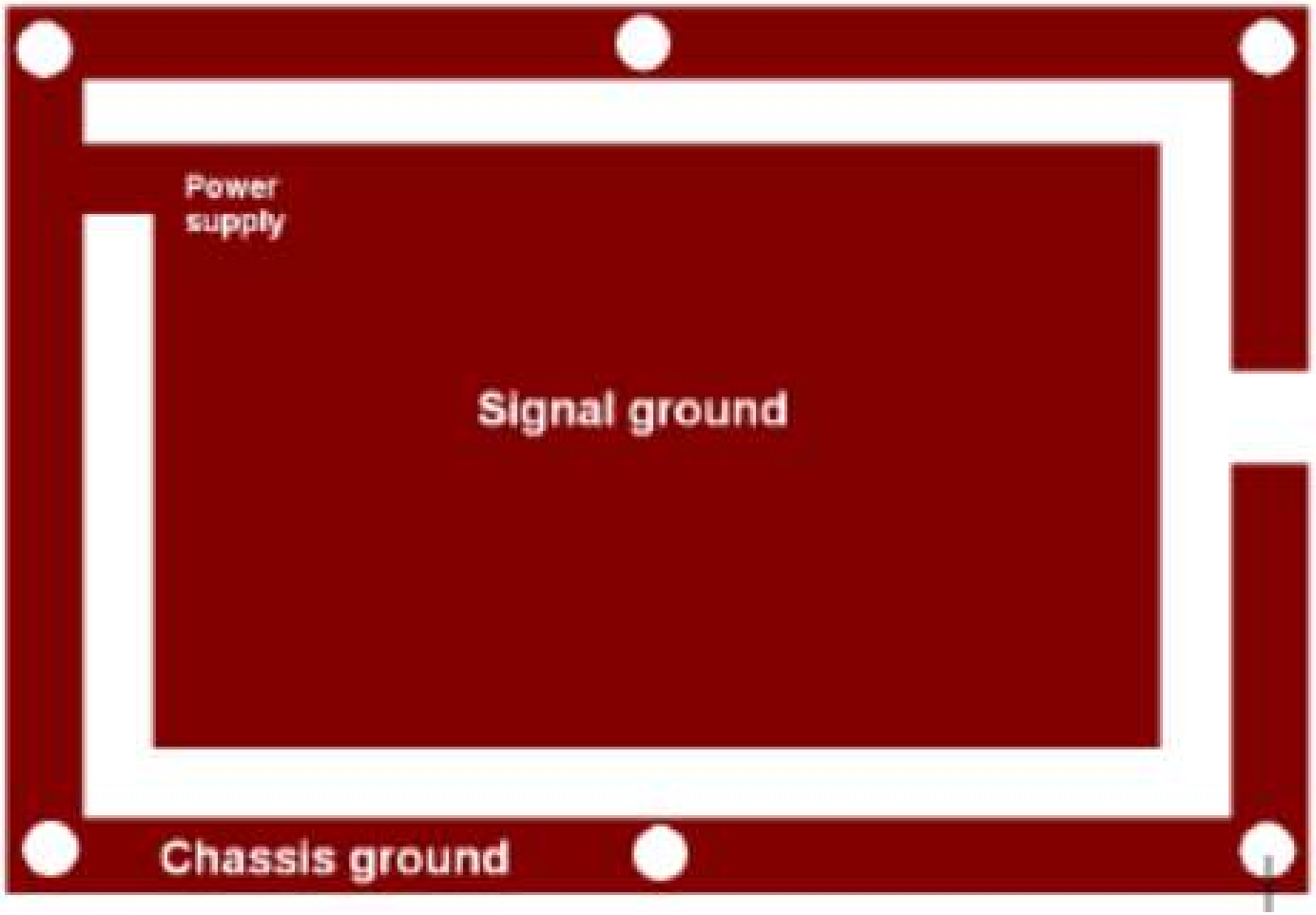
Measured Results of the SSCG

- F_m = 100 KHz.
- F_{dev} = 3.0 %.
- PPR >13 dB.
- $F_{pll} = 5.5 * F_{ref}$



Spectrum analyzer view with and without SSCG:

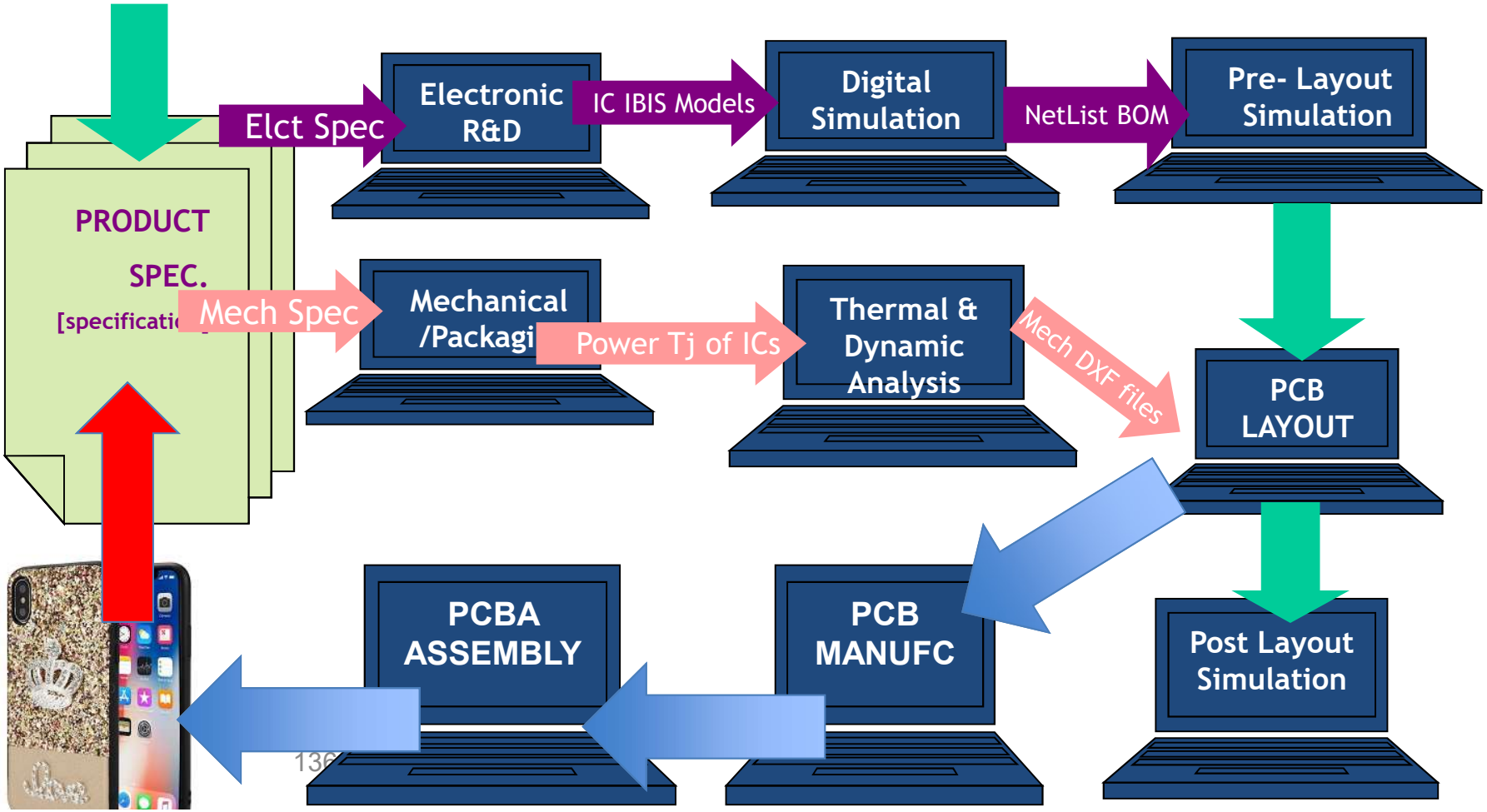
Chassis Guard for ESD



PCB Generations – SI/PI/EMC Perspective

Gen.	Situation	Conductor	Results
1	DC of DC	Short between ptp	Current/Voltage
2	AC of DC	Self-Inductance	EMI & Crosstalk
3	BGA Packages	Power Planes Inductance	Ground/Power Bounce SSN, SSO
4	Hi-Speed	Transmission Line Impedance Control	Signal = E.M. Wave Reflection Overshoot/Undershoot Distortion
5	Higher Speed Lossy line #1	Skin Effect	Conductor Resistance Varies with Frequency Attenuation
6	Lossy line #2	Conductor Environment = Dielectric Material	Dielectric Losses Attenuation
7	Multi-Giga F	Differential Pair	Via Effects

Prefered Board Design to PCB Cycle



Analog Engineers know the world is Analog
RF Engineers know the world is Analog

Hi Digital Engineer **The world is Analog**

Any “Digital world” is an illusion

The **Schema** is more “Concept” than “Fact”

The real world is the **PCB**

It is not a Paradise at all

Right the First Time?

As a **Quality management concept** that

defect prevention

is more advantageous and cost effective than

defect detection and associated rework.

It can be achieved

Balance

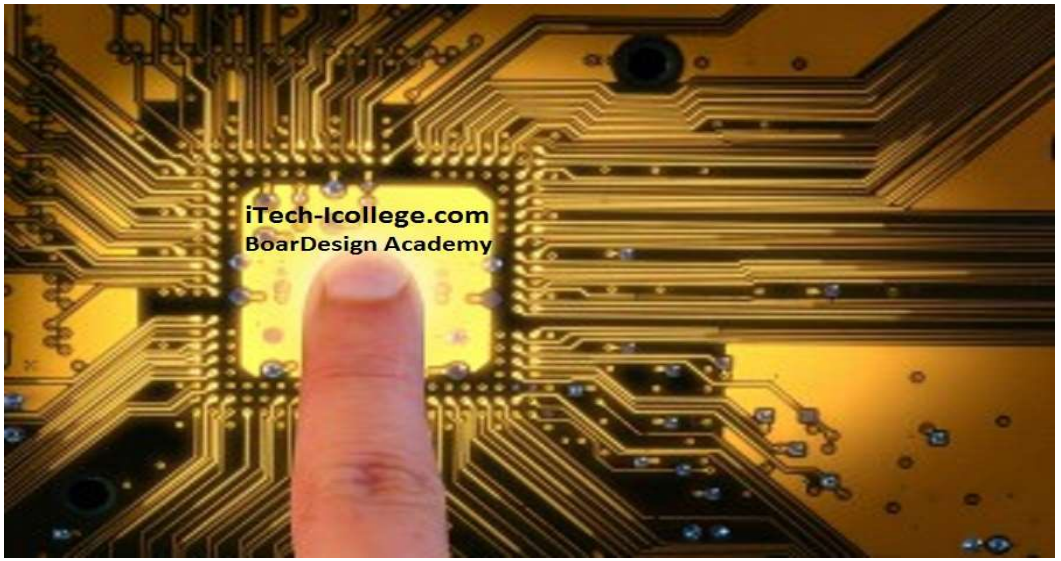
Physical - Conductor

Spiritual - Signal

Mind - You

Trust No One but YOU

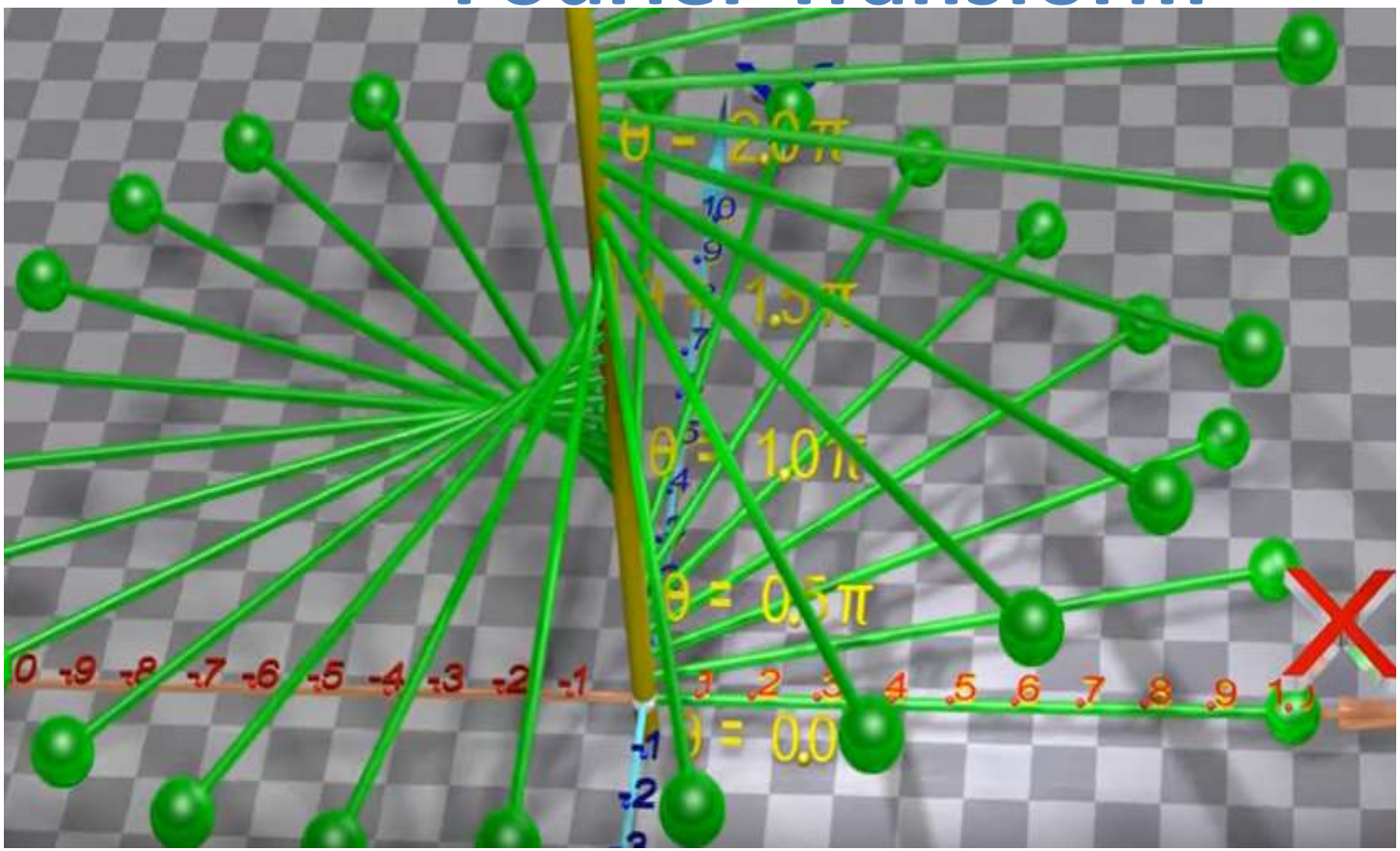
I hope I helped you a bit
Thank you very much



For Slides ask me on Email or on Website

Shalom-Shlomi-Zigdon@iTech-iCollege.com

Fourier Transform



VIDEO