Demystifying Edge Launch Connectors

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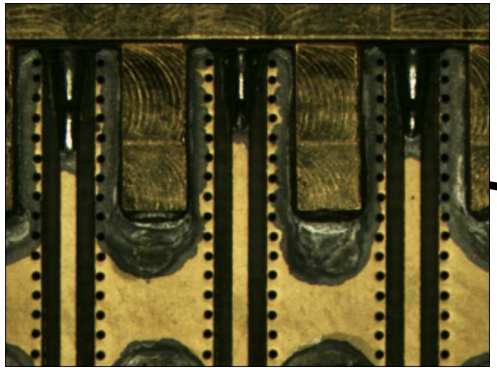
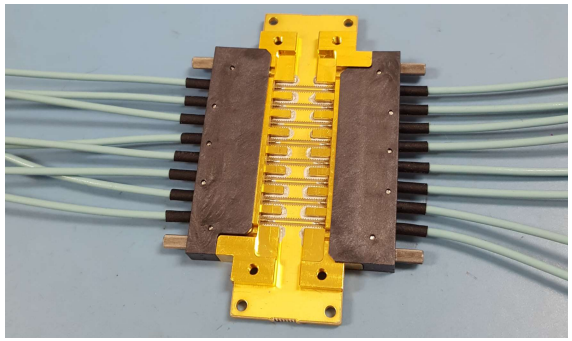
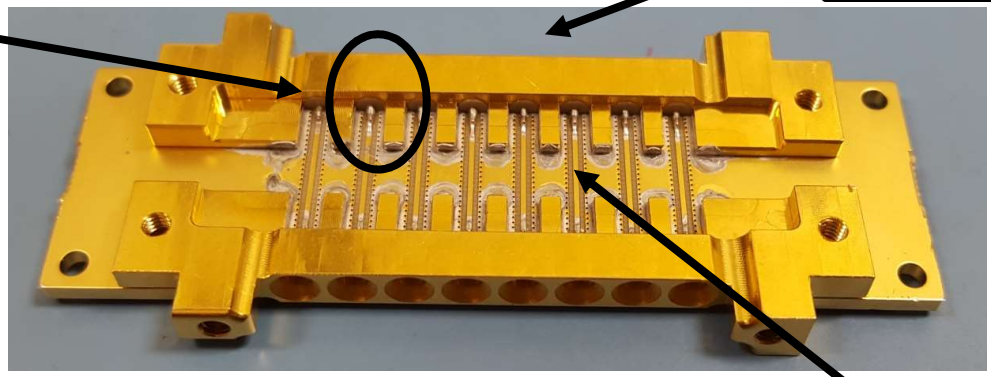
Outline

- **What is a RF edge launch connector?**
- Identify the problem
  - Field leakage
  - Ground and signal discontinuities
- Proposed Solutions
  - Matching the size of the printed circuit board (PCB) dielectric layer and connector signal pin
  - Edge platting of PCB
- Conclusion and next steps

Example 1: Typical RF edge launch connector



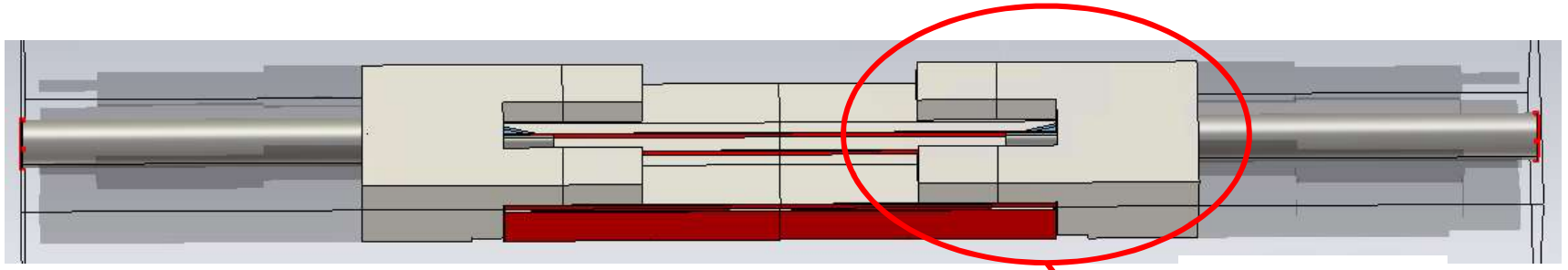


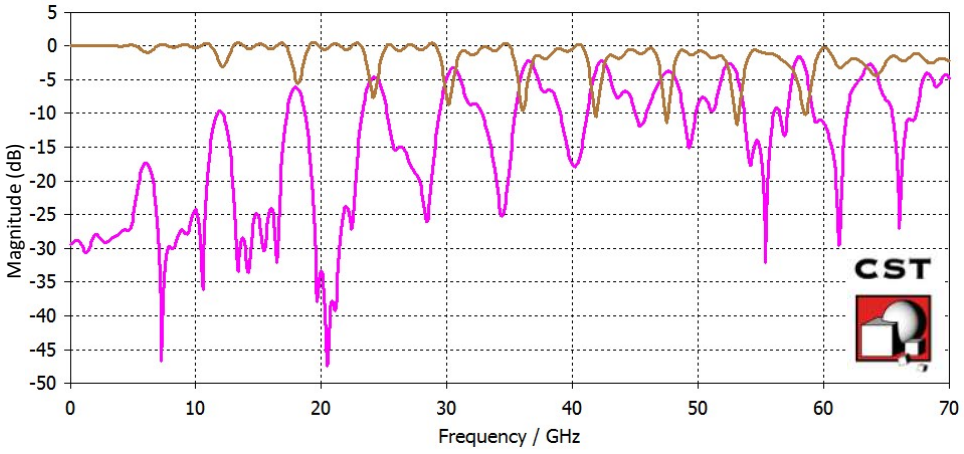


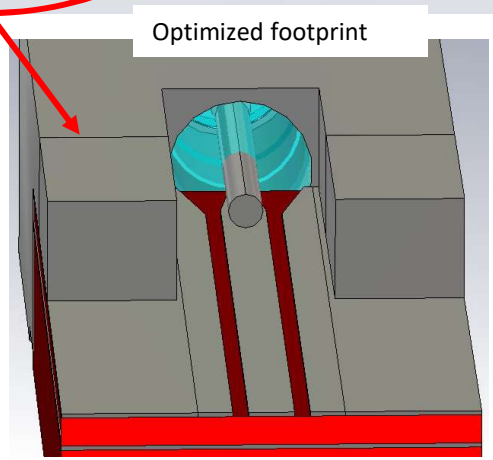
Edge Launch Connector

Printed Circuit Board (PCB)

Example 2: Typical RF edge launch connector







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- **Identify the problem**
  - **Field leakage**
  - Ground and signal discontinuities
- Proposed Solutions
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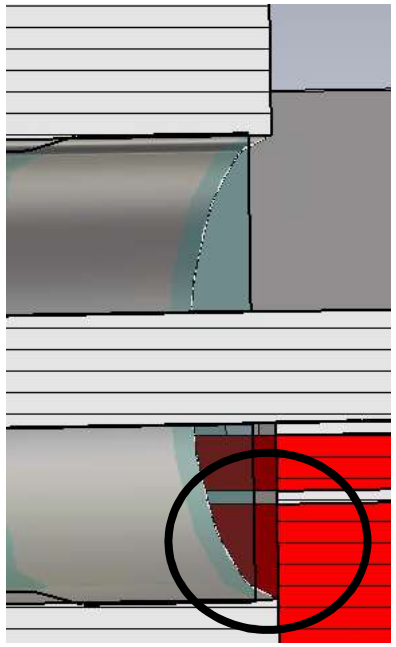
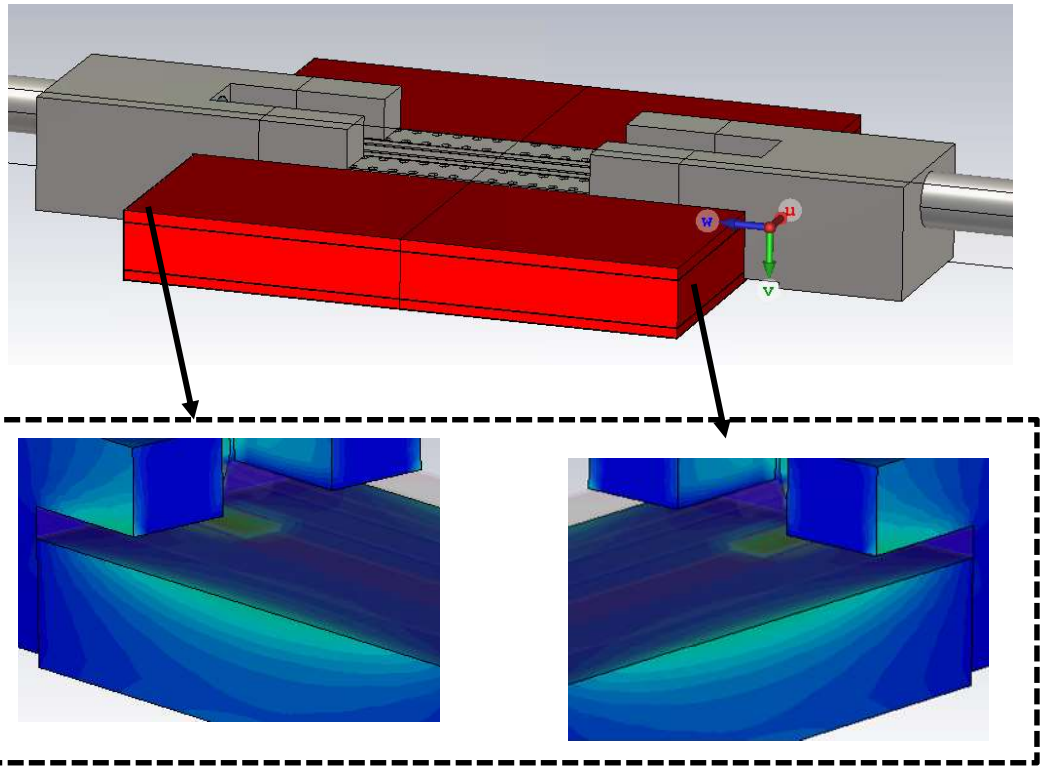
- Conclusion and next steps

Field Leakage



Internal PCB Ground not aligned to connector ground



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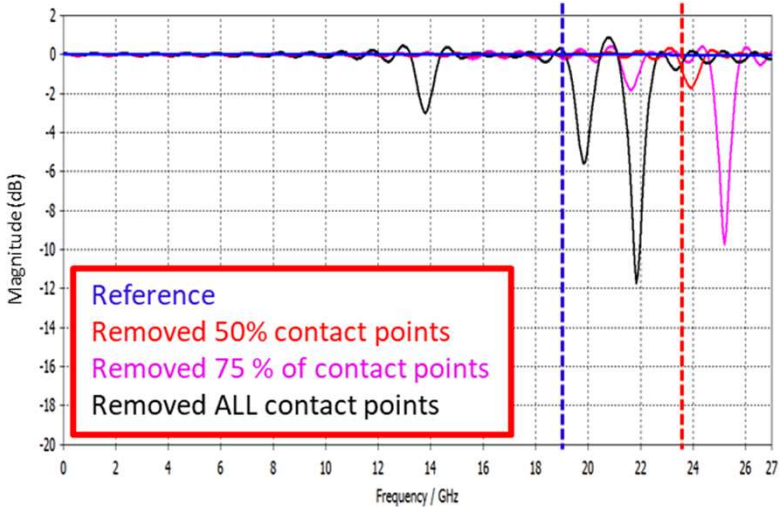
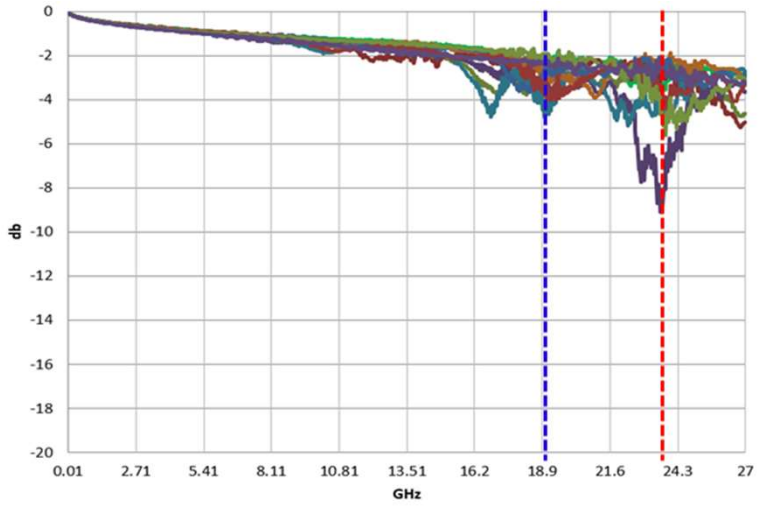
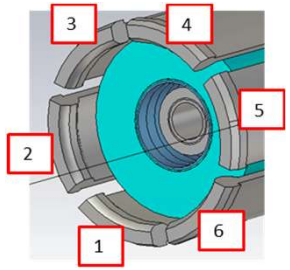
Ground Discontinuities (1)

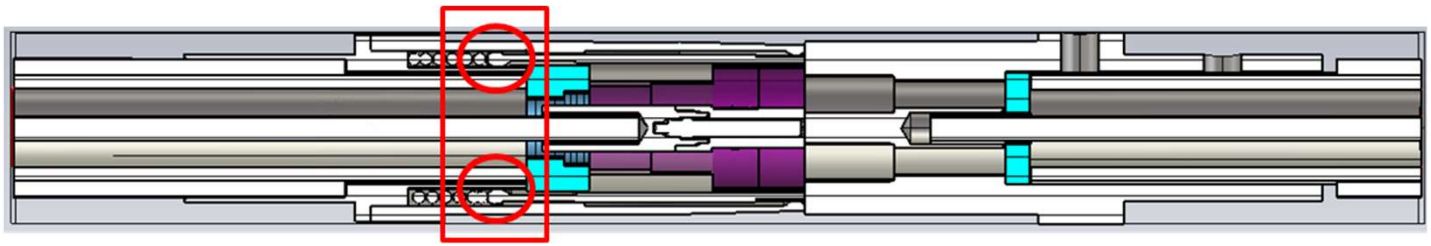
Simulated Data



Measured Data

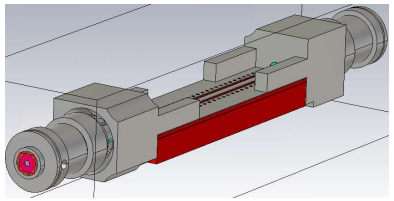


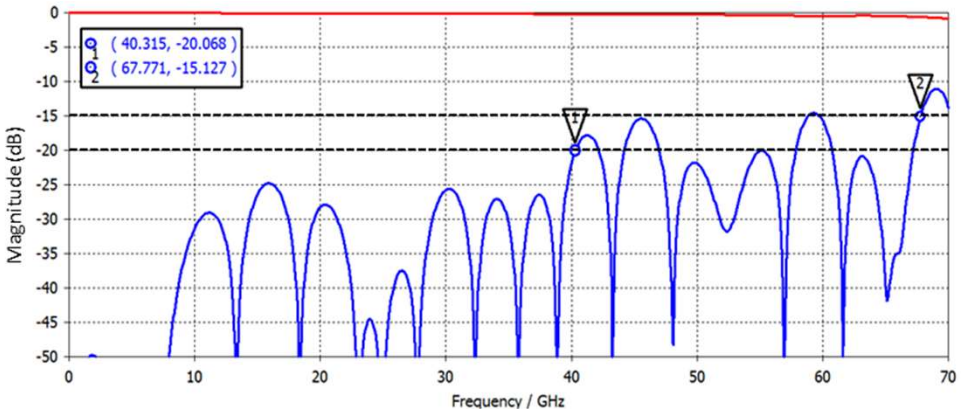


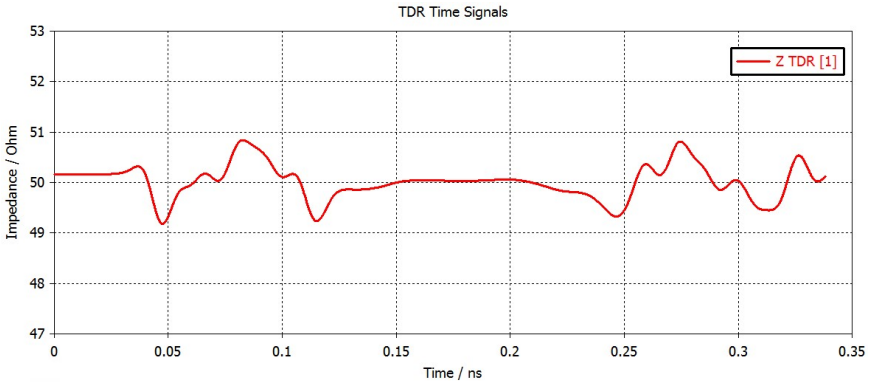


Ground Discontinuities (2)

- Assembly utilized to characterize RF edge launch interconnect
- All geometric dimensions and locations are nominal

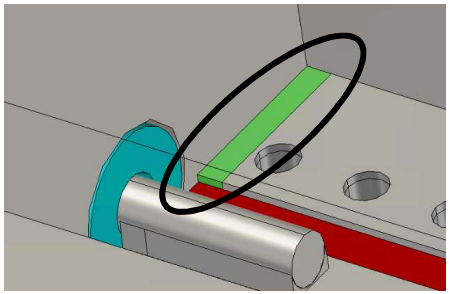


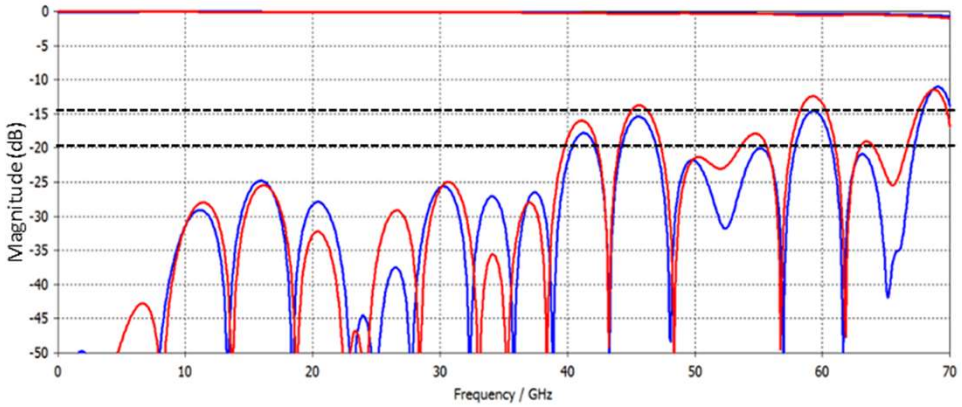


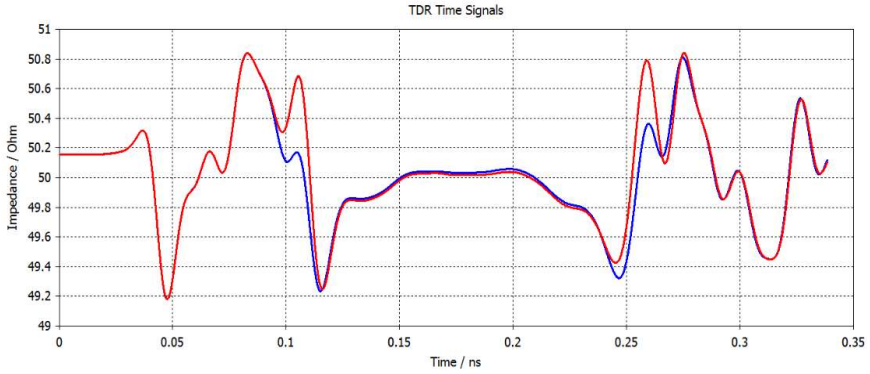


Ground Discontinuities (3)

- Co-Planar ground pulled back 0.127mm/5 mils from the edge of the board

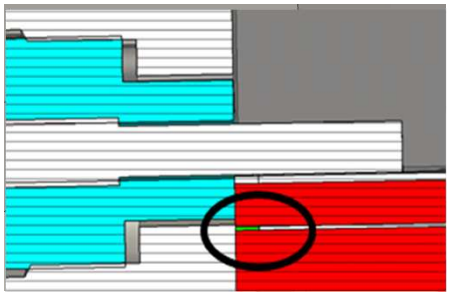


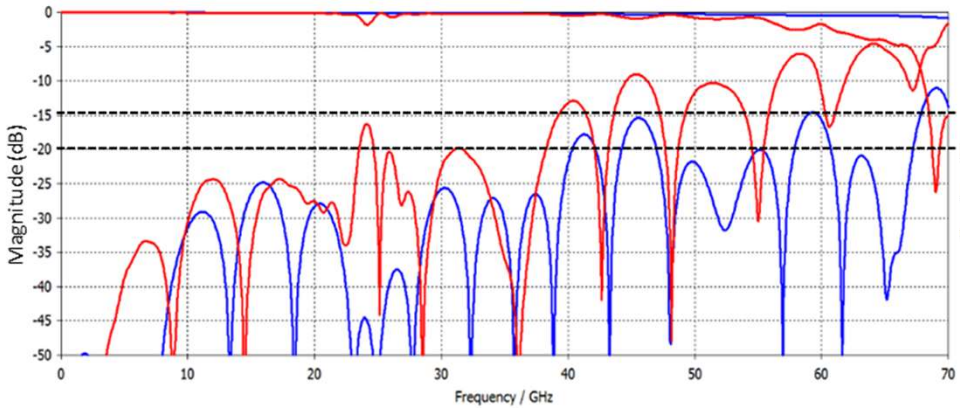


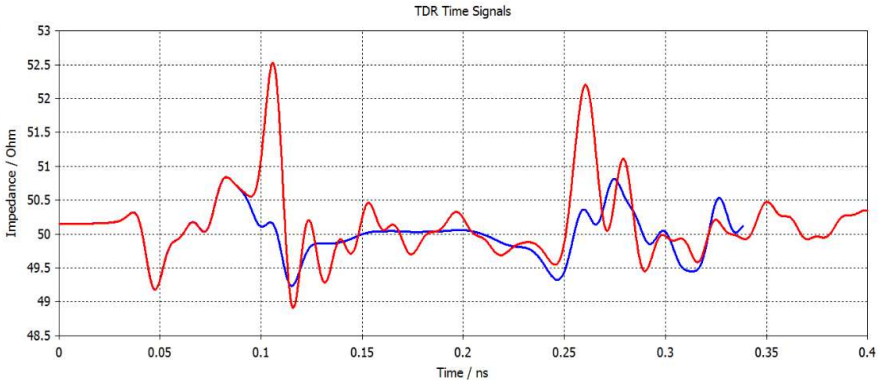


Ground Discontinuities (4)

- First internal ground plane pulled back 0.127mm/5 mils from the edge of the board

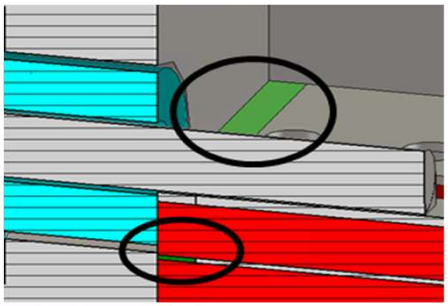


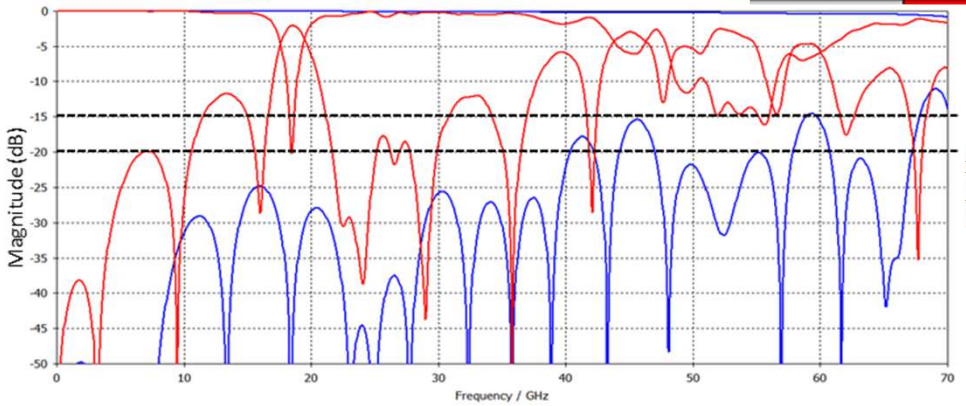


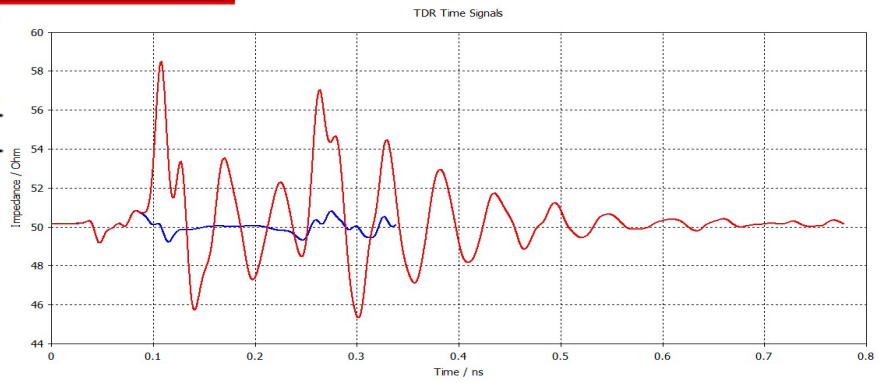


Ground Discontinuities (5)

- Top two ground plane layers pulled back 0.127mm/5 mils from the edge of the board

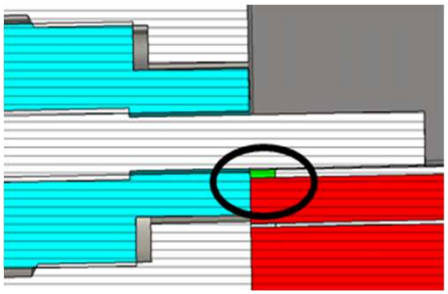


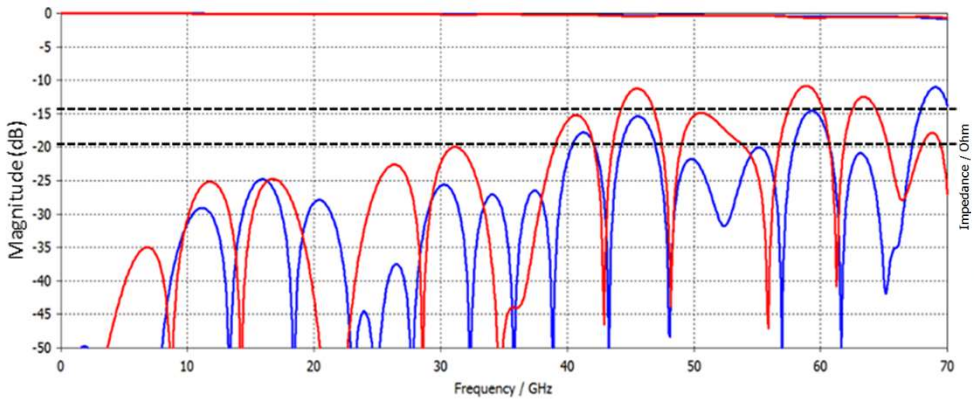


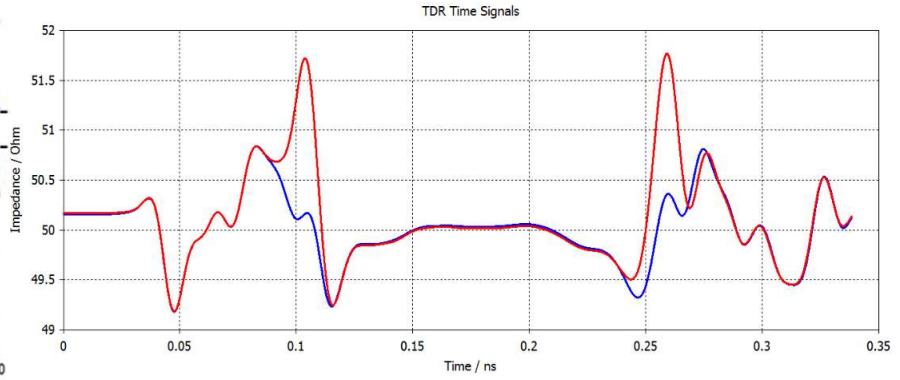


Signal Discontinuities

- Trace pulled back 0.127mm/5 mils from the edge of the board

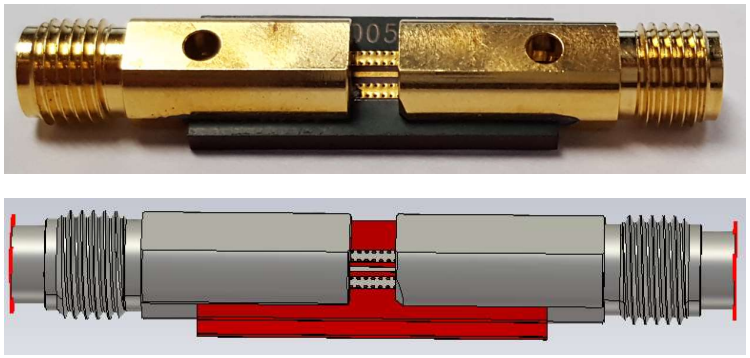




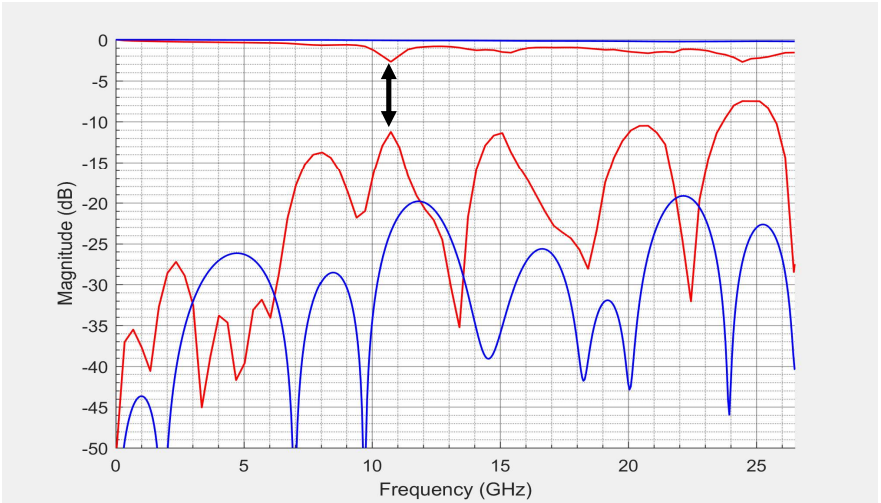


Ground Discontinuities (Example)

- Performance degraded due to ground discontinuities present at the interface w/PCB
- Connectors did not undergo the correct soldering process



Simulated Data
Measured Data



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Proposed Solutions (1)

- Match the size of the PCB dielectric layer and connector signal pin.
  - Proper ground structure alignment to prevent field leakage
- Edge platting:
  - Minimizes the ground discontinuities at the transition from the connector to the board
  - Prevents field leakage when a larger top dielectric layer on the board is not possible

Proposed Solutions (2)

- Placement of:
  - Vias → Line the co-planar structure on the board with vias to channel the fields in the direction of propagation
  - Connector → Flush against the edge of the PCB to prevent field leakage and a degradation of performance at higher frequencies (PCB edge can be milled down)

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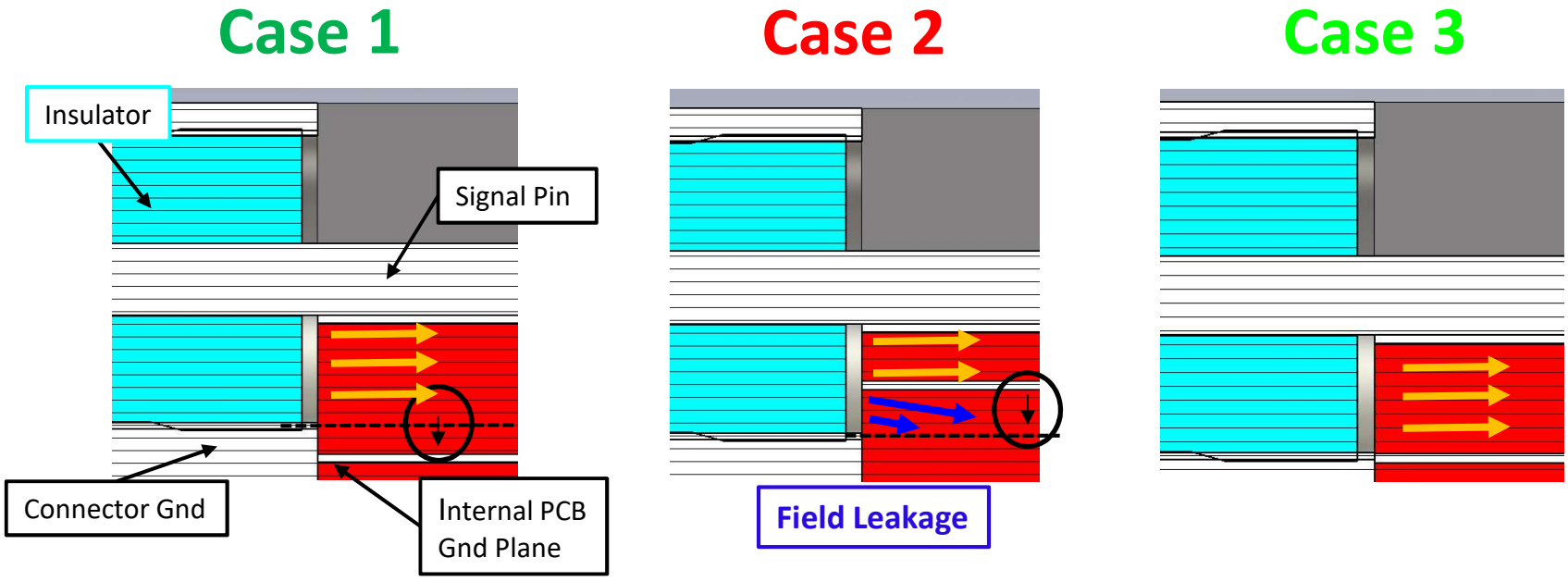
Ground Structure Alignment

- A misalignment of the connector ground and the internal PCB ground plane can lead to resonances.



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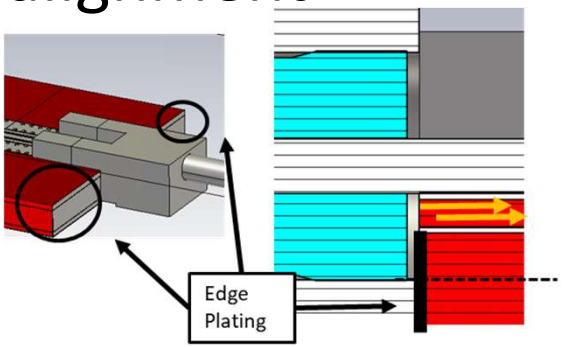
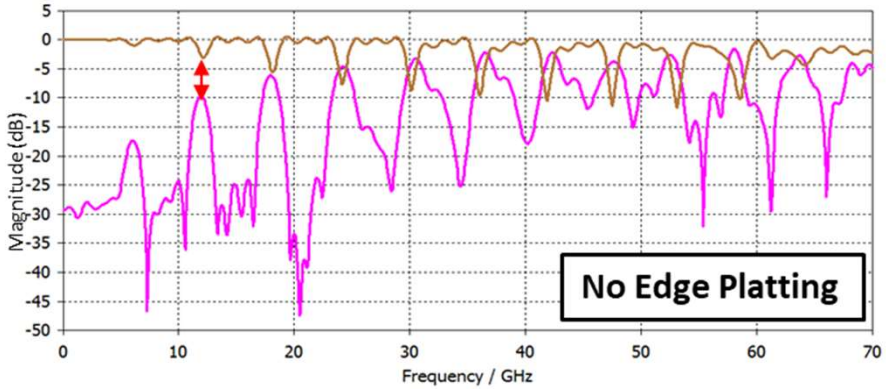
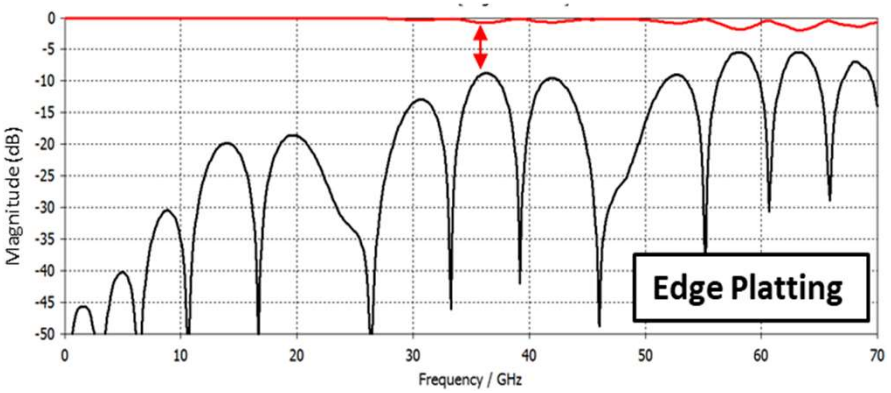
Edge Platting

- Addresses improper ground structure alignment
- Prevents field leakage
- Minimizes ground discontinuities

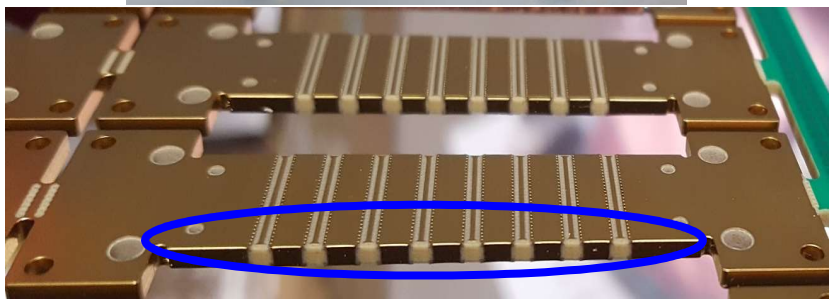




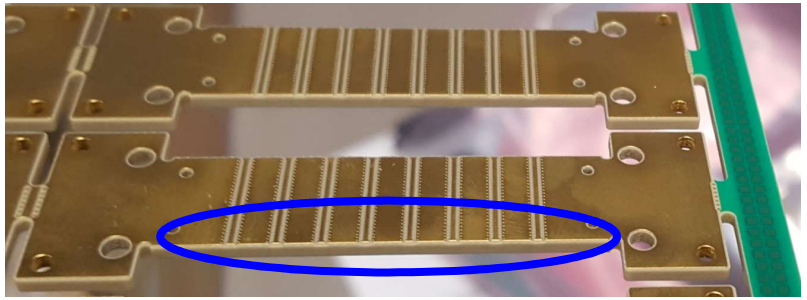


Edge Platting Experiment (1)

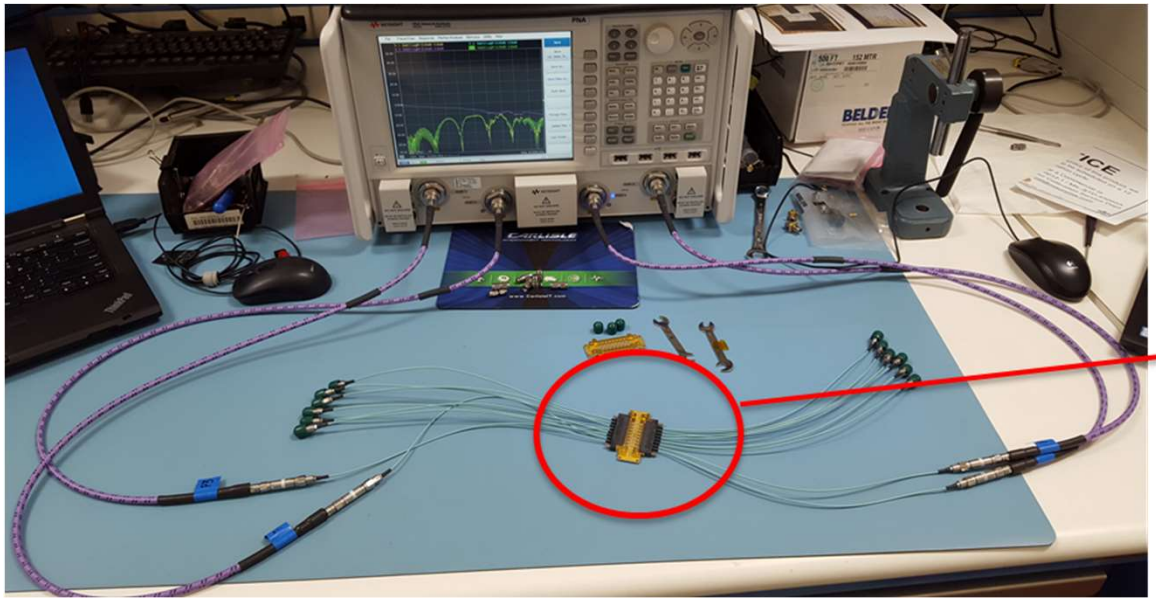
Edge Platting

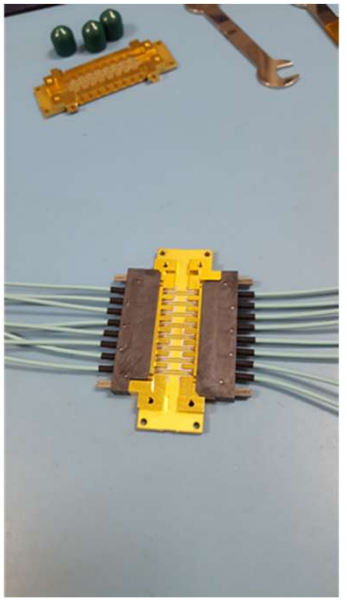


No Edge Platting



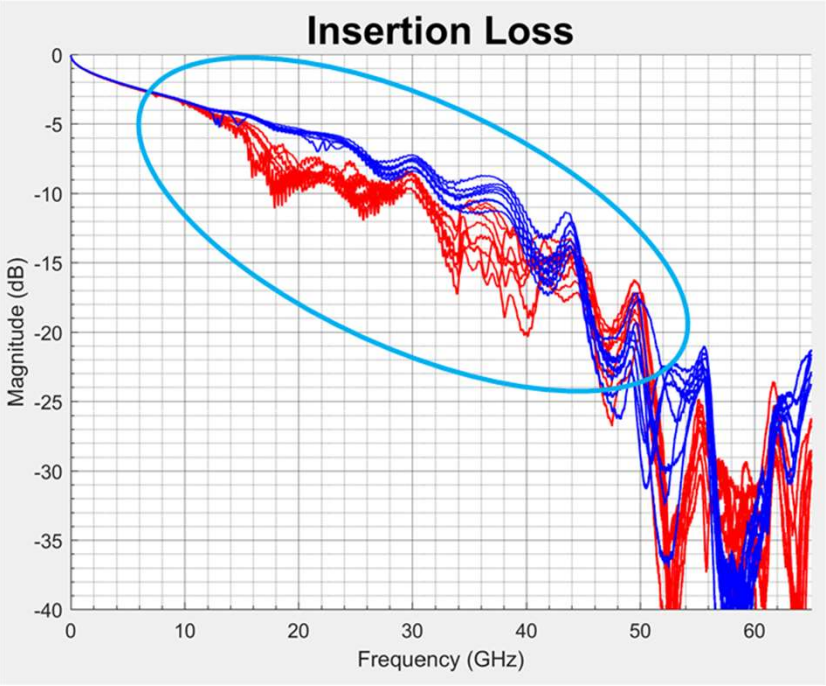
Edge Platting Experiment (2)

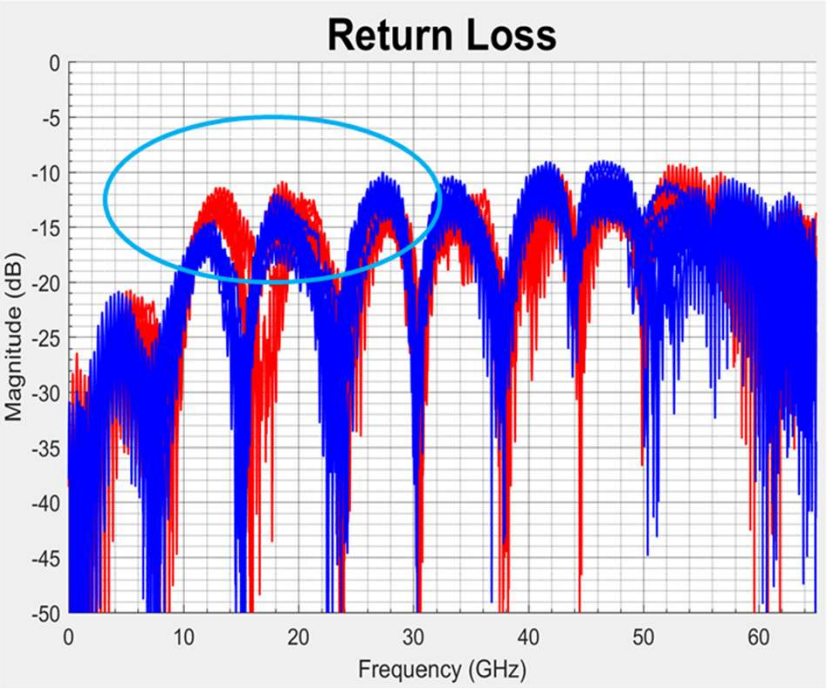




- Keysight PNA Network Analyzer N5227A 10MHz-67GHz & 1.85mm standard calibration kit (85058B)

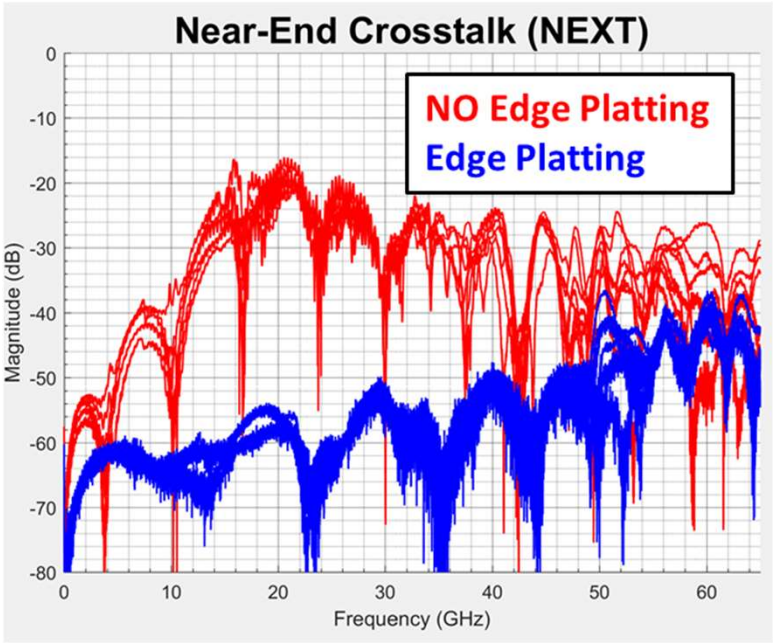
Edge Platting Experiment (3)

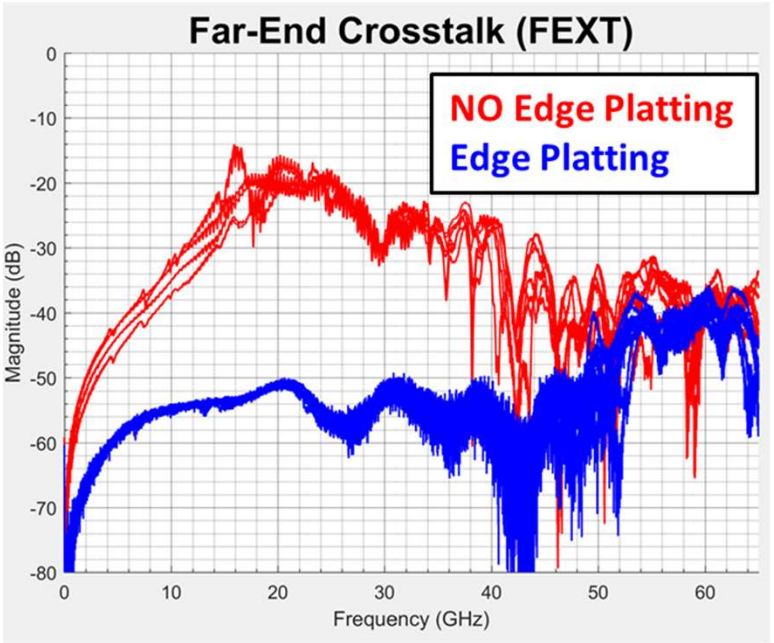


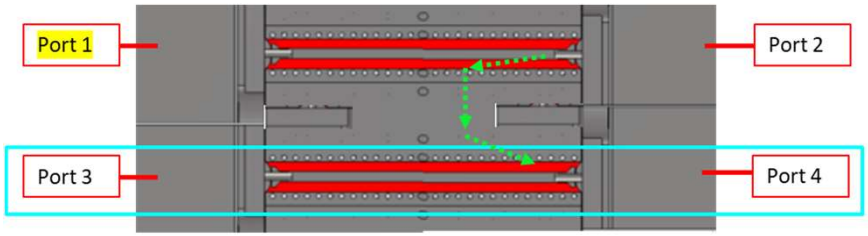


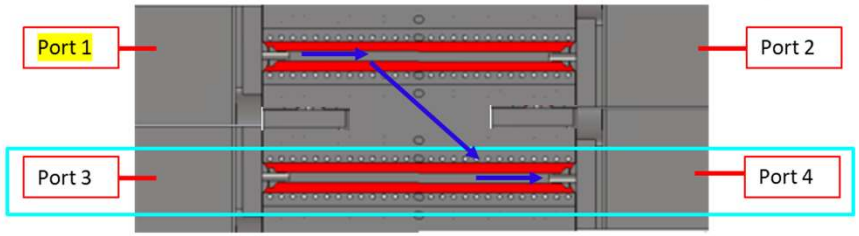
NO Edge Platting
Edge Platting

Edge Platting Experiment (4)









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Conclusions

- Edge launch RF connectors require an optimized footprint to ensure performance.
- Some key challenges to address are:
  - Field leakage (resonances)
  - Ground and signal discontinuities
- Proposed Solutions
  - Match the size of the PCB dielectric layer and connector signal pin.
  - Proper ground structure alignment, including the vias to prevent field leakage
  - Edge platting:
    - Minimizes the ground discontinuities, Prevents field leakage

Next Steps

- Experiment with different edge platting configurations
- Revisit connector design to add redundant ground connections to reduce the effect of manufacturing tolerances on the board