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Signal Integrity Analysis on High-Density Silicon Interposer Package Technology for Next-Generation Applications

Surender Singh, Taranjit Kukal

Cadence Design Systems, Inc.

Outline

- Introduction
- Silicon Interposer vs Package-on-Package (PoP)
- Test Vehicle
- Simulation Results
- Conclusions

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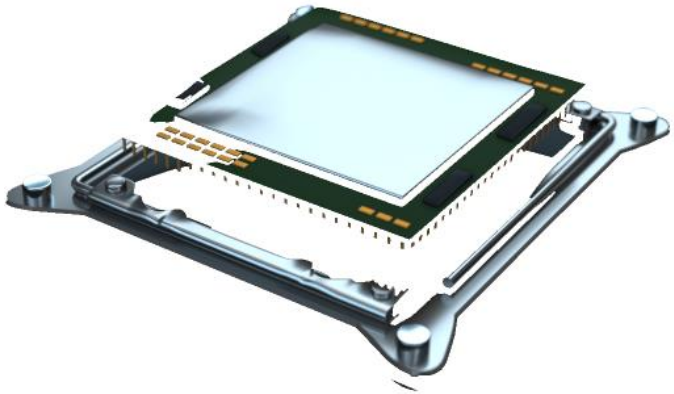
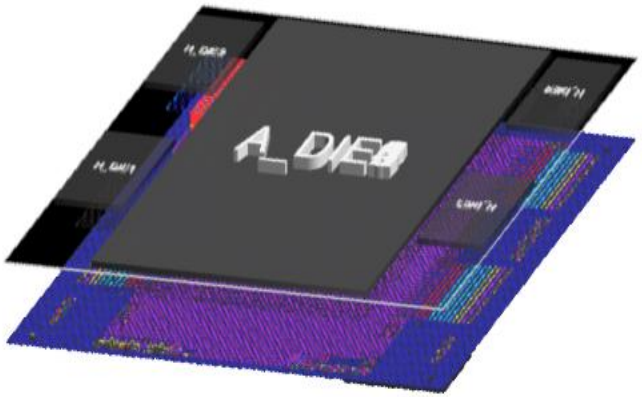
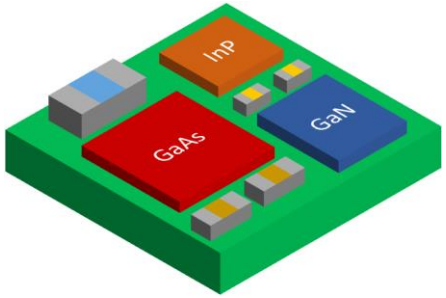
Introduction

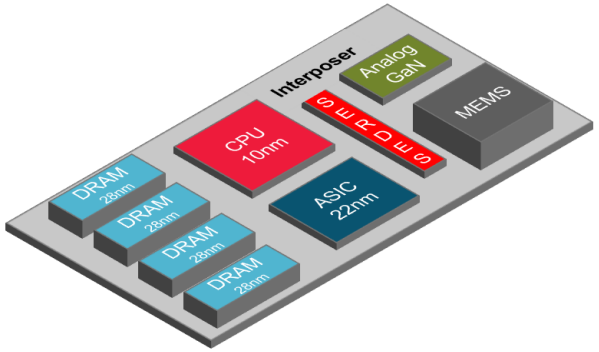
- Advanced packaging trends driven by
  - Heterogenous integration
  - More than Moore…
  - Advanced packaging technologies





Heterogeneous Integration… Transforming Moore's Law





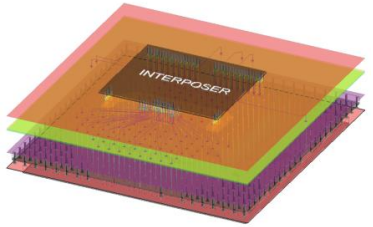
Driven by PCB and Package Designers

Driven by IC Designers

Multi-Chip Module (MCM) — **System in a Package (SiP)** — **Heterogeneous Integration**

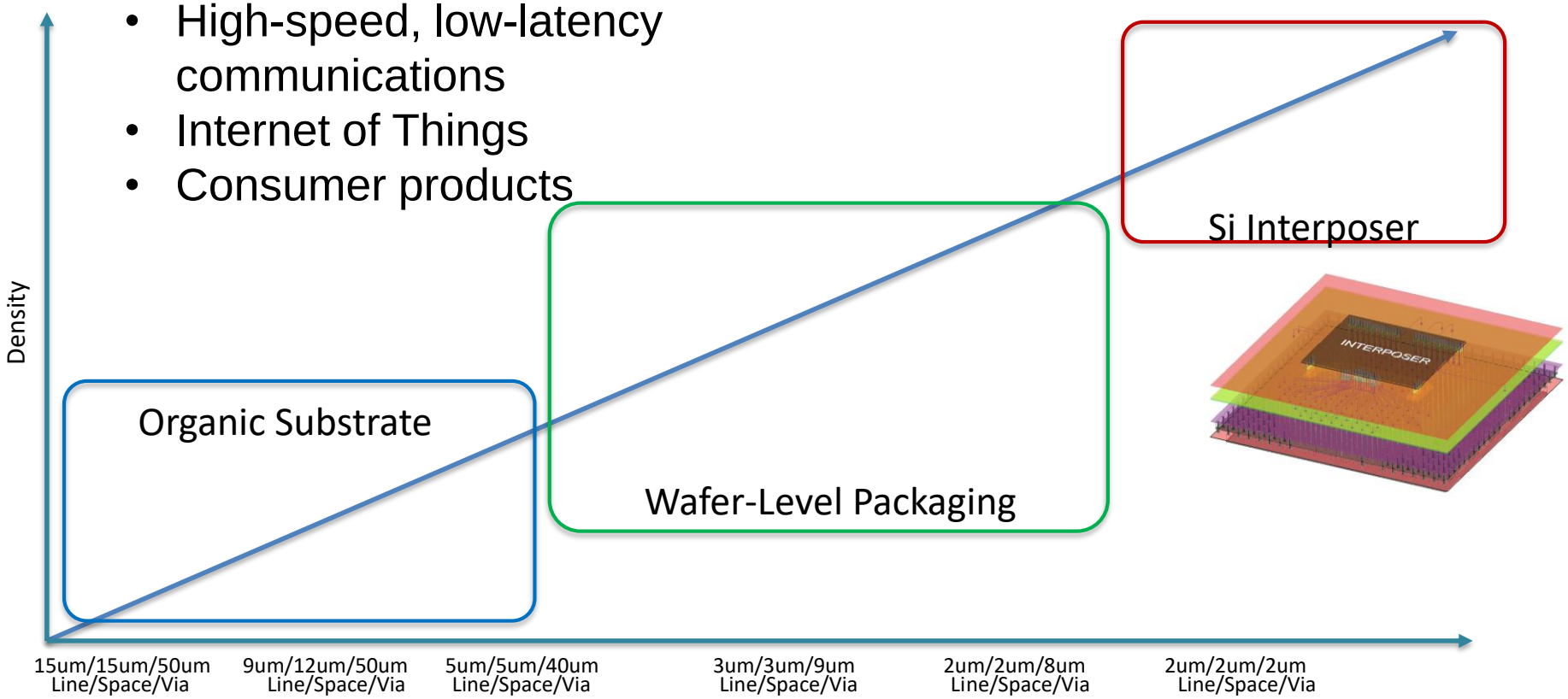
1970 — 2005 — Now

Integrating multiple ICs, across multiple technologies and process nodes, into a single device/package



Advanced Packaging Technologies

- High-performance computing
- High-speed, low-latency communications
- Internet of Things
- Consumer products



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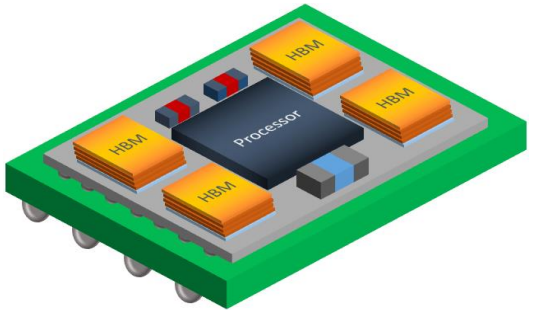
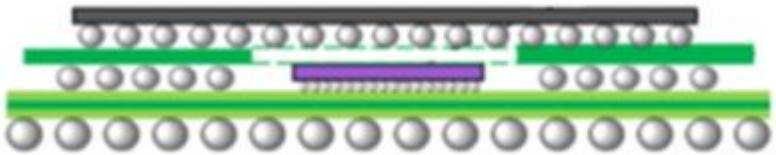
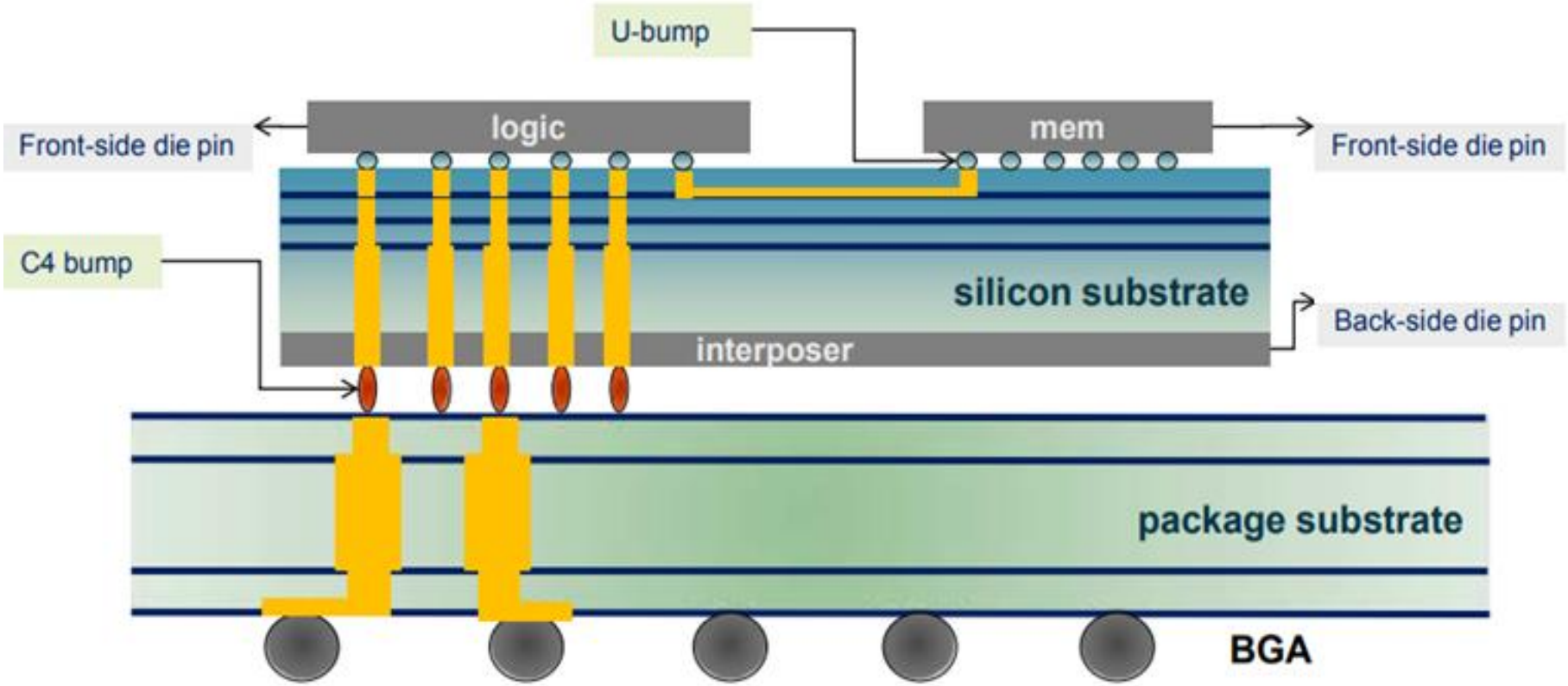
Silicon Interposer vs PoP

- Heterogeneous construction integrates the ASIC die multiple high-bandwidth memory (HBM) stacks; achievable through
  - Si-Interposer configuration
  - PoP configuration

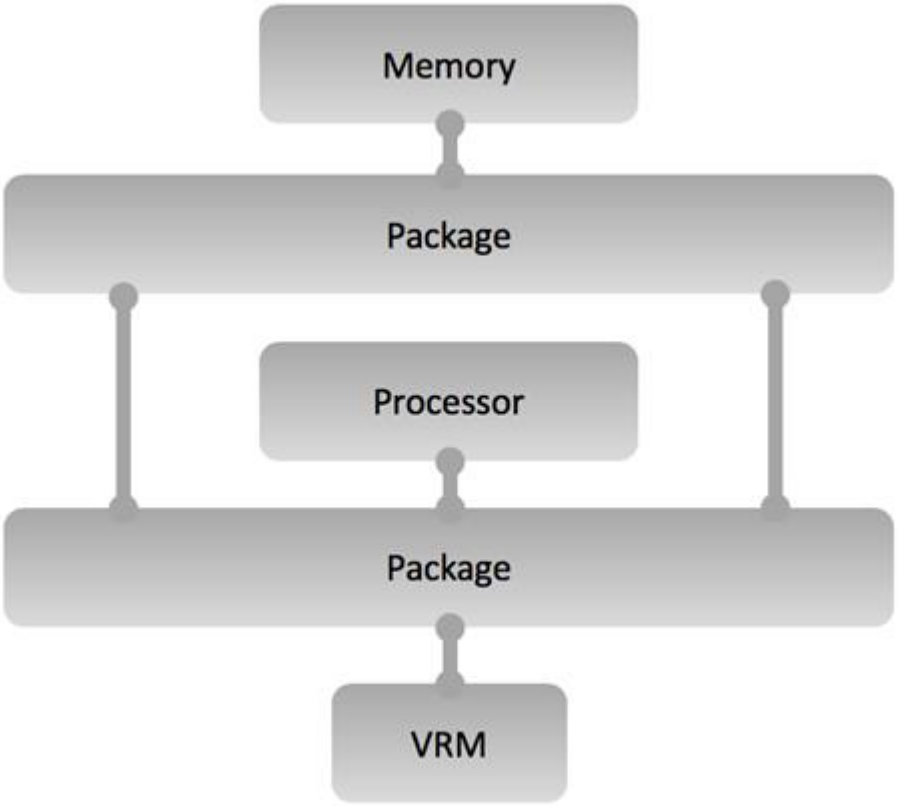


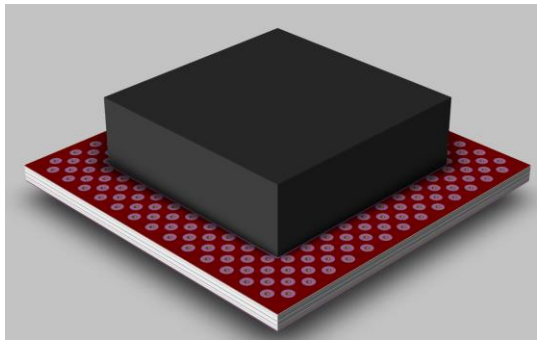


Si Interposer Overview

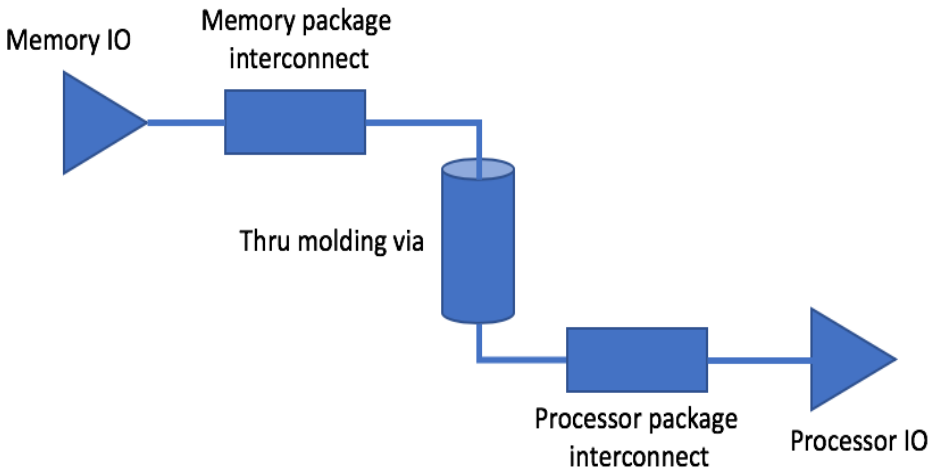


PoP Overview





PoP Interconnect Structure



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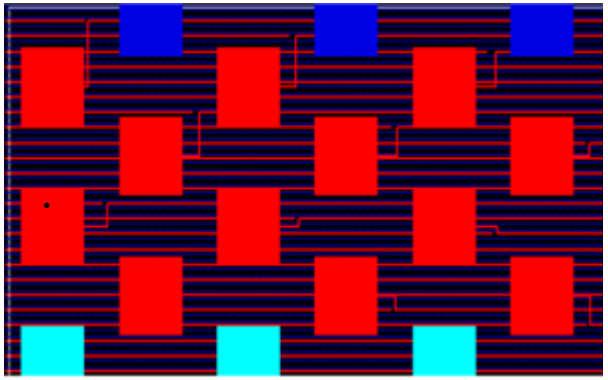
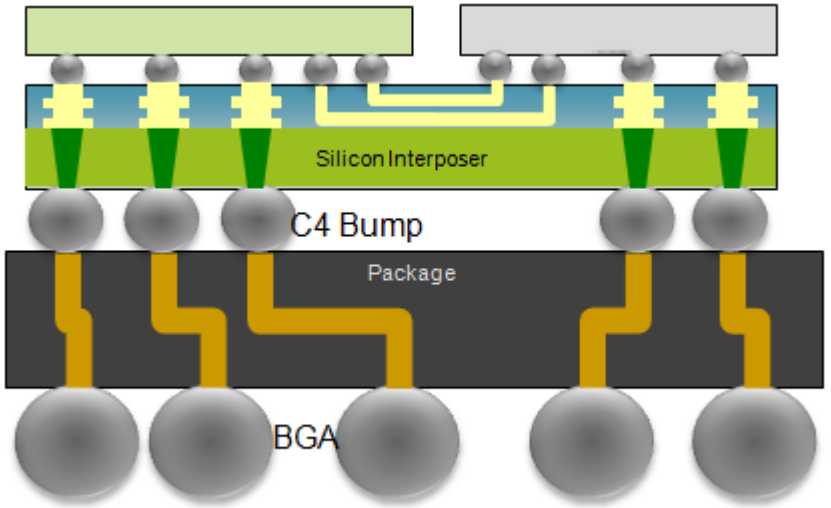
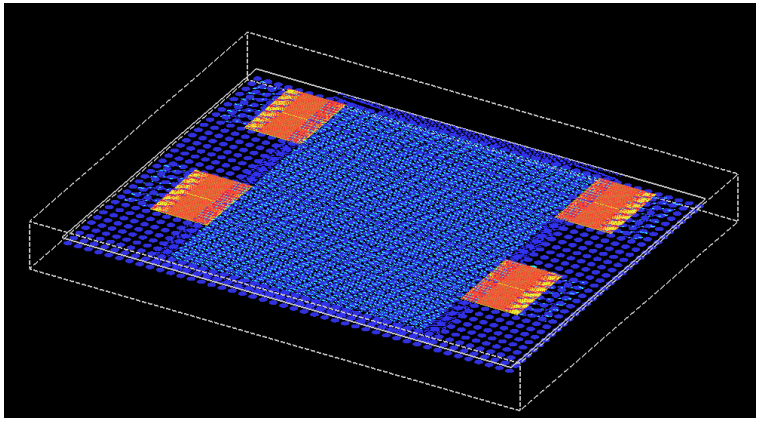
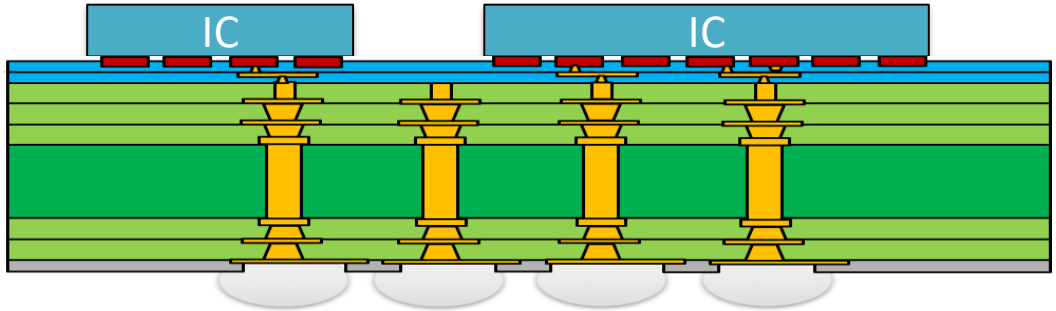
Si-Interposer Design: Topology



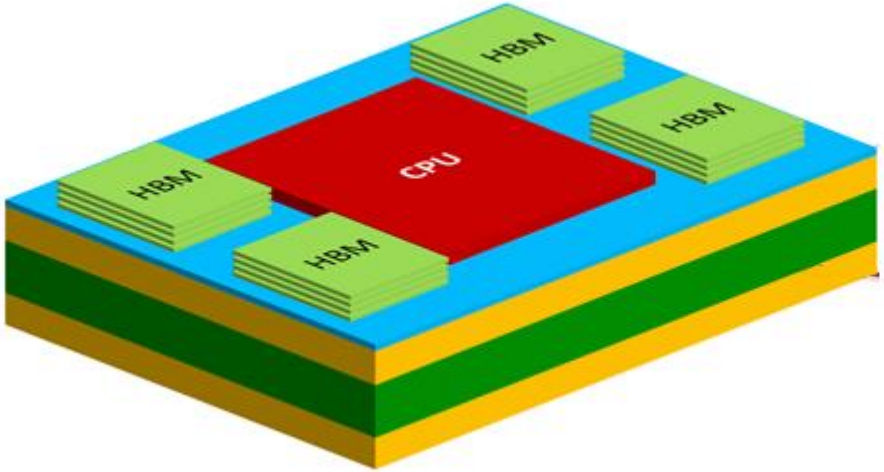


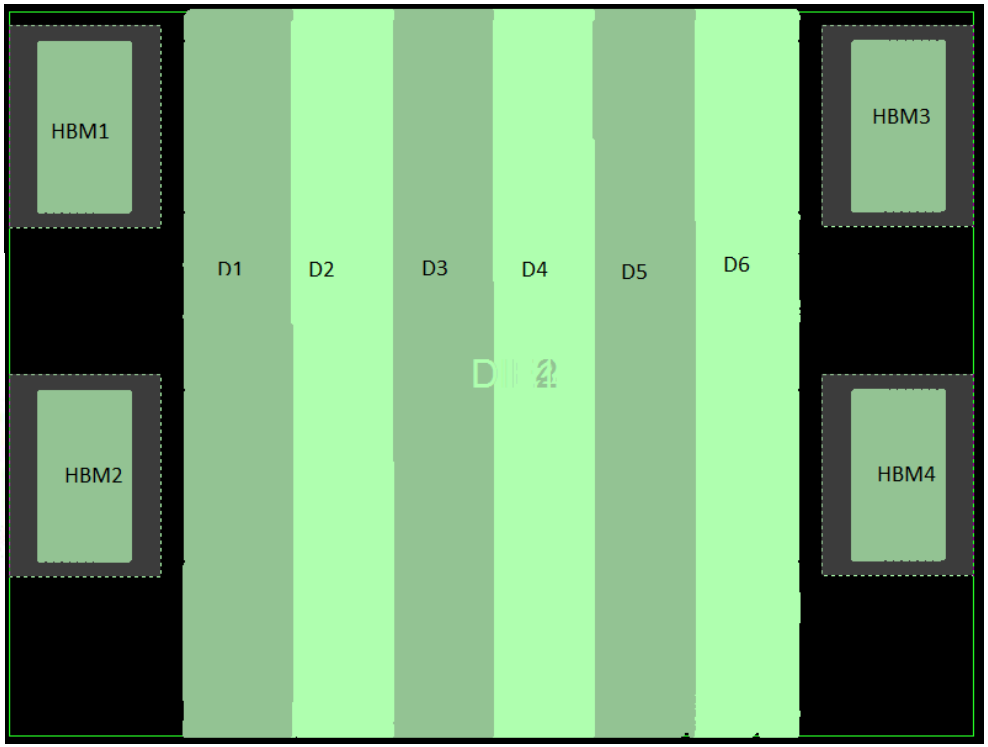




Si-Interposer Design: Components

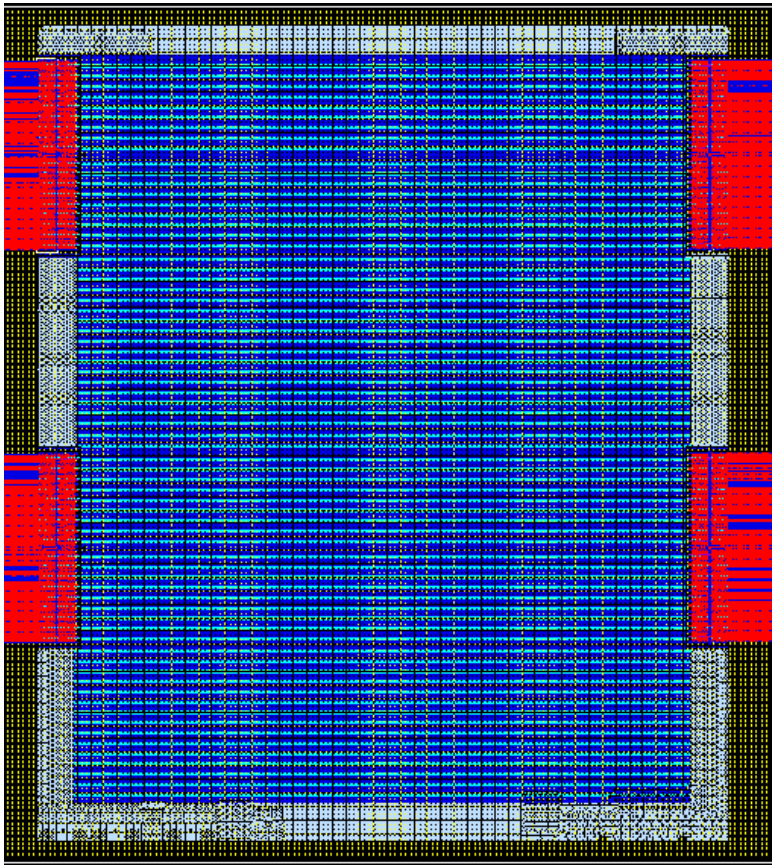
- 4 HBM stacks
- 1 CPU
- Thin-film interposer





Si-Interposer Design: Specifications

- Total bumps: 188K bumps
  - ASIC die: 168K bumps
  - ASIC Die: Split into 6 dies (each 28k bumps)
- No of HBM: 4 dies
  - Each HBM: 5K bumps
    - total 20 K bumps



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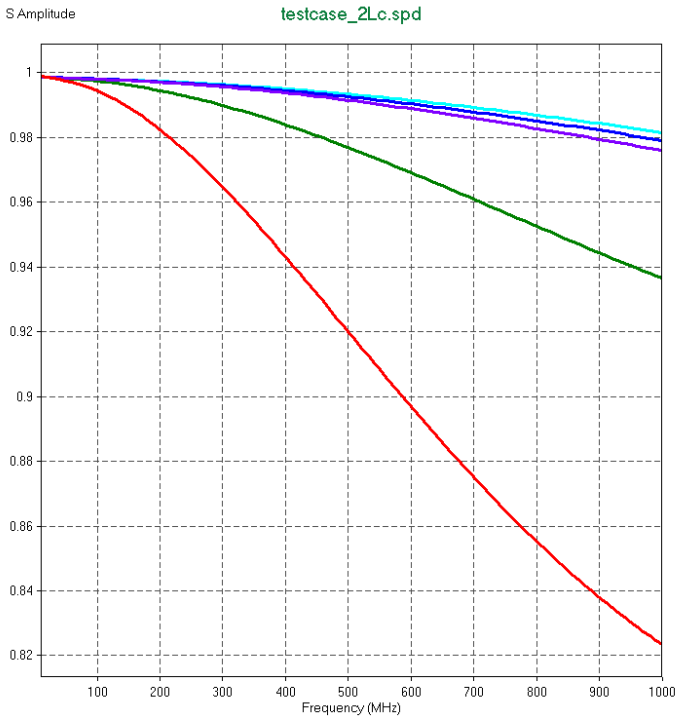
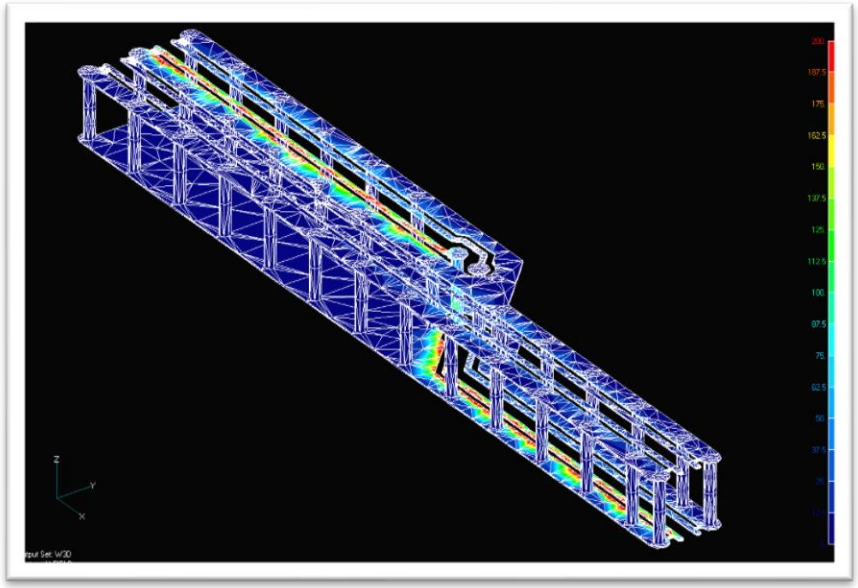
Model Extraction in 3D-FEM



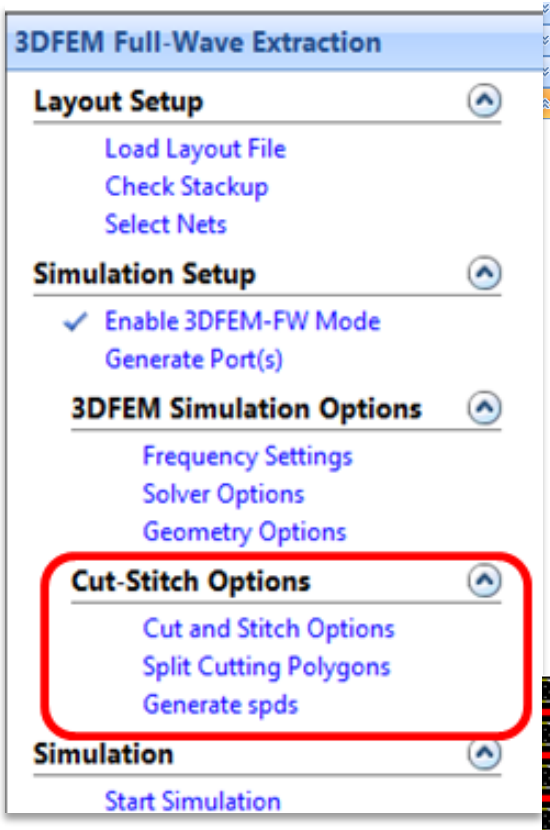
Adaptive meshing example

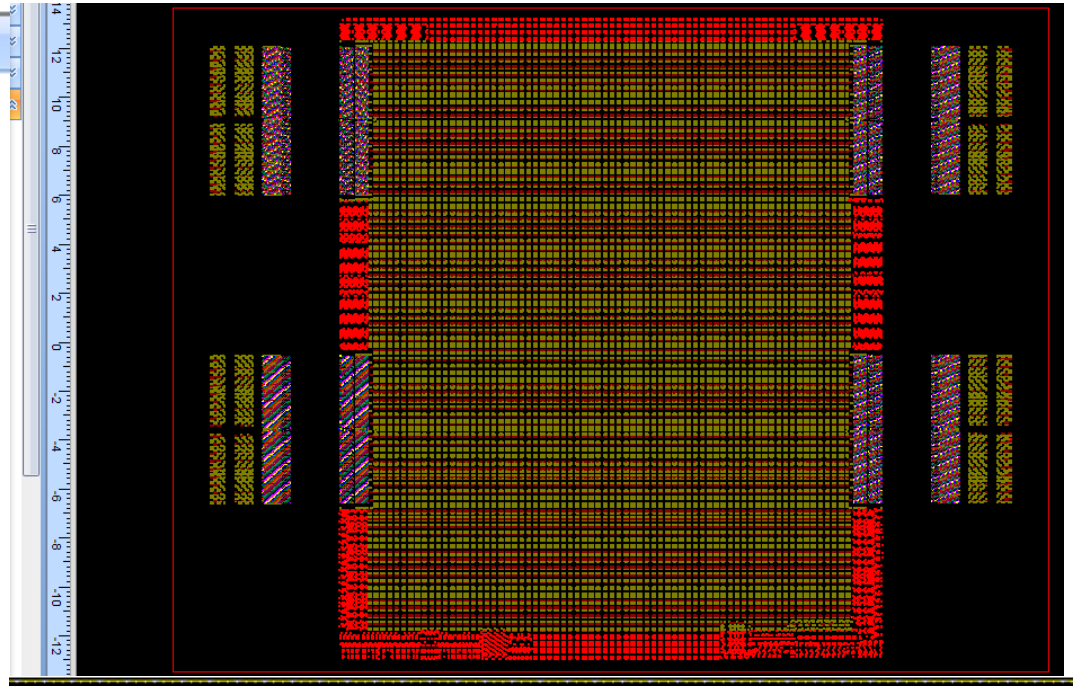
Variation of insertion loss during adaptive meshing

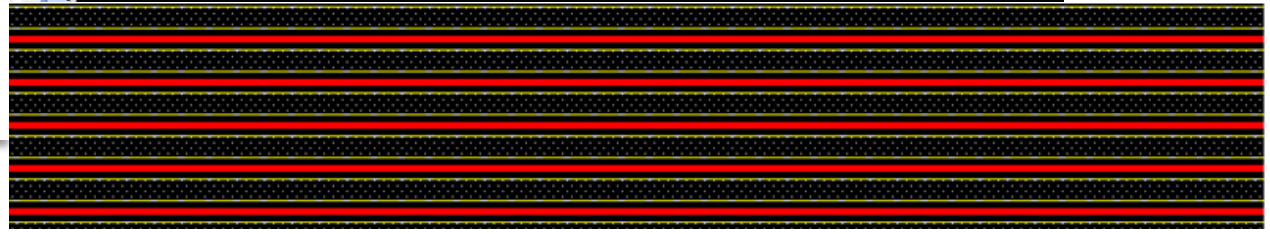


3D-FEM provides full-wave solver for accurate analysis of complex 3D structures

Model Extraction in 3D-FEM

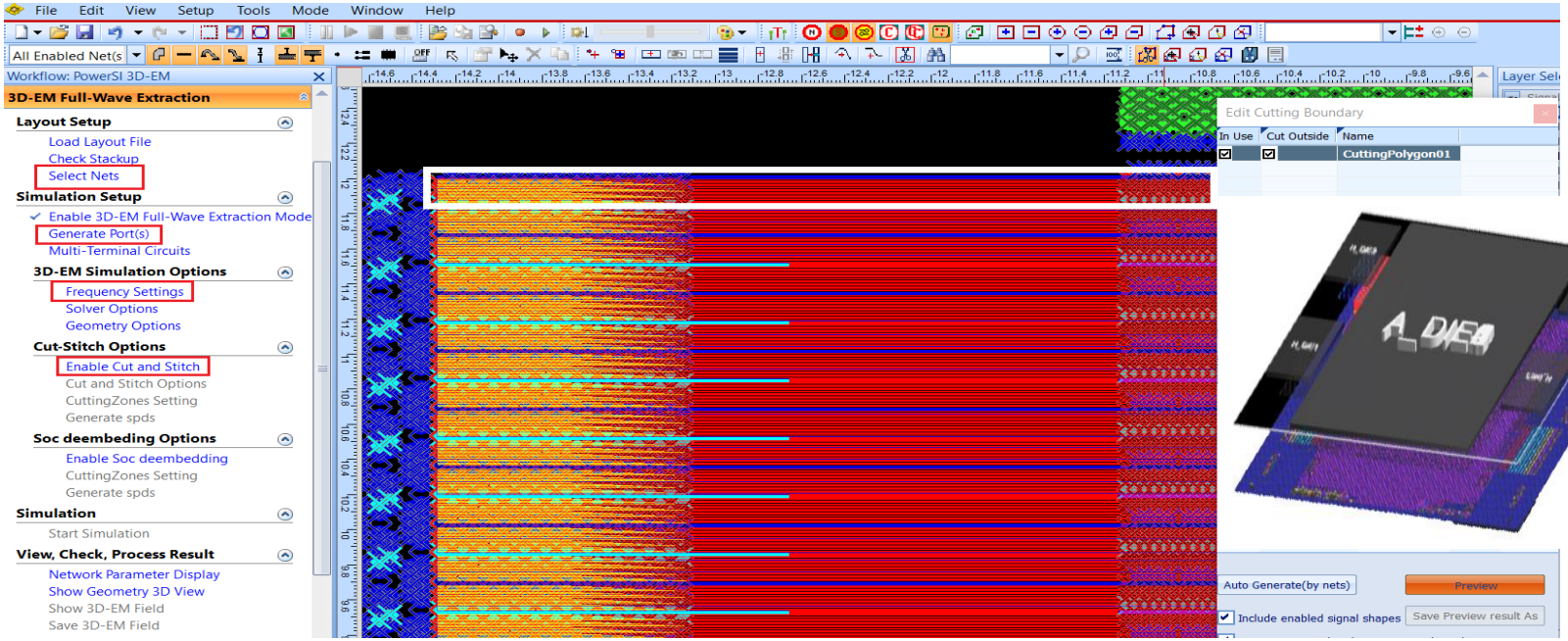




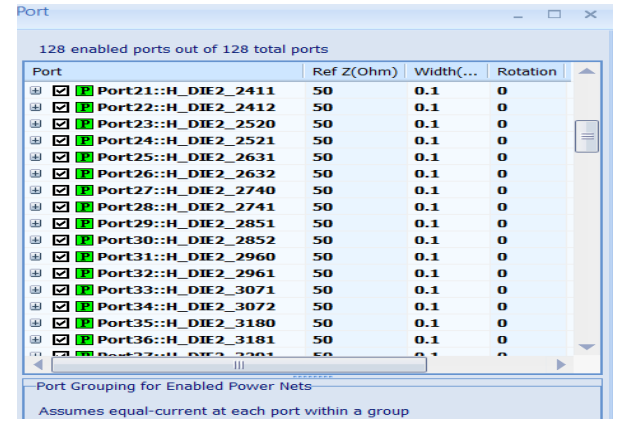


M2

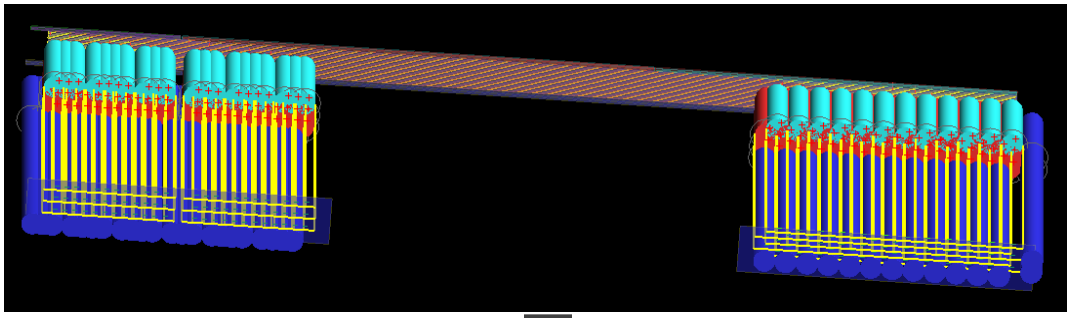
Model Extraction in 3D-FEM



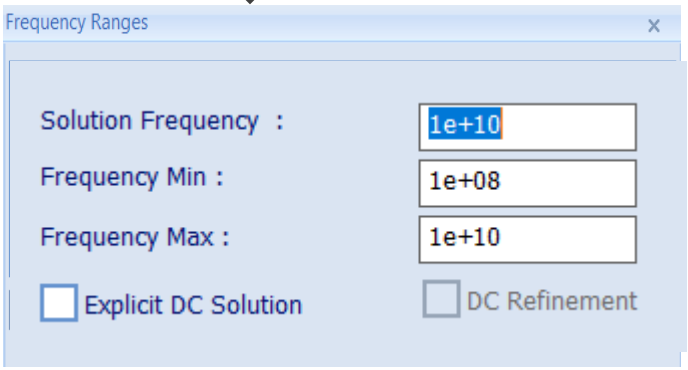
S-Parameter Extraction with 3D-FEM



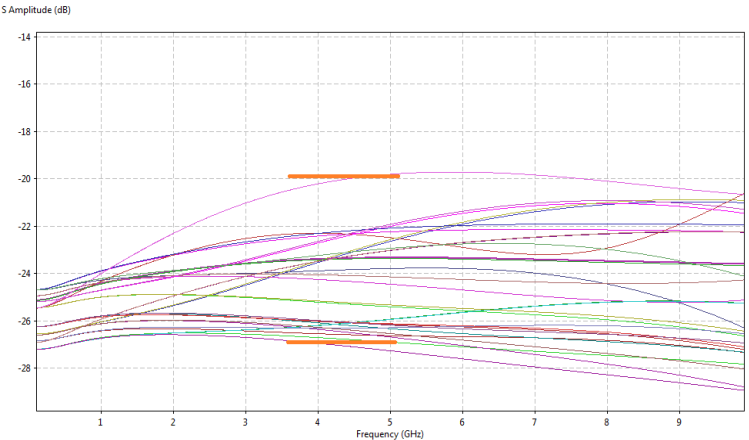
Auto-ports generation



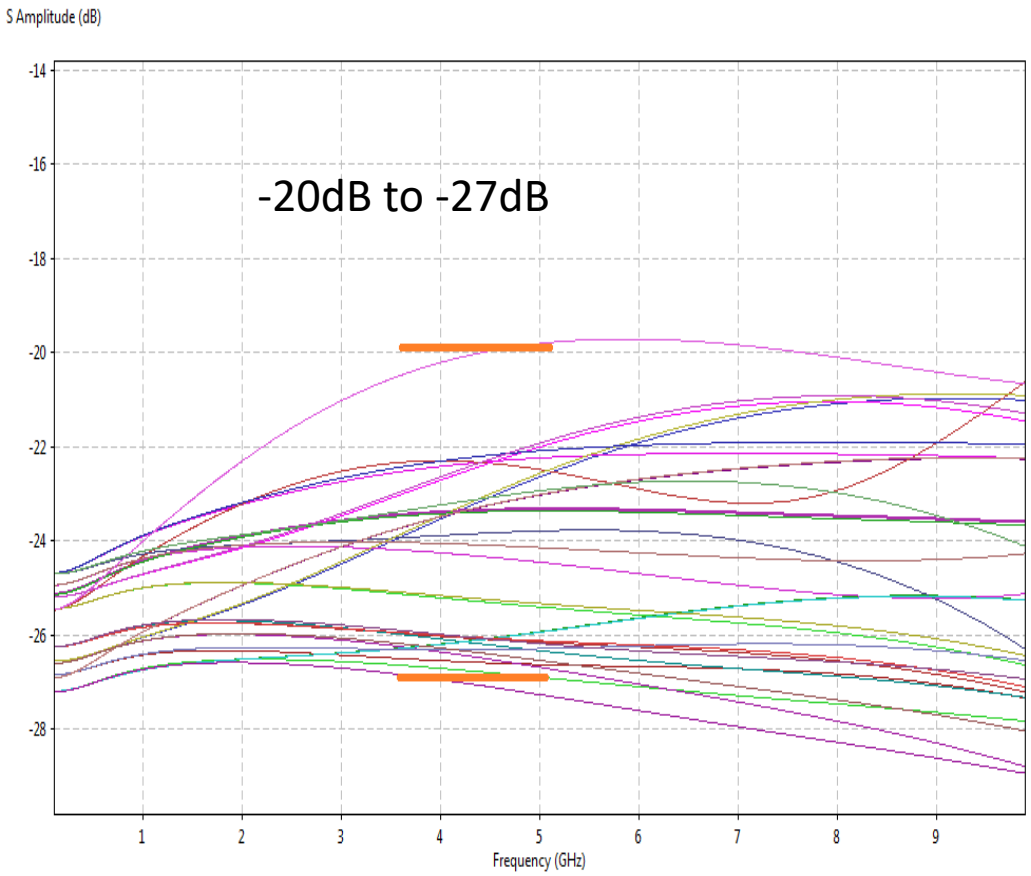
Frequency sweep

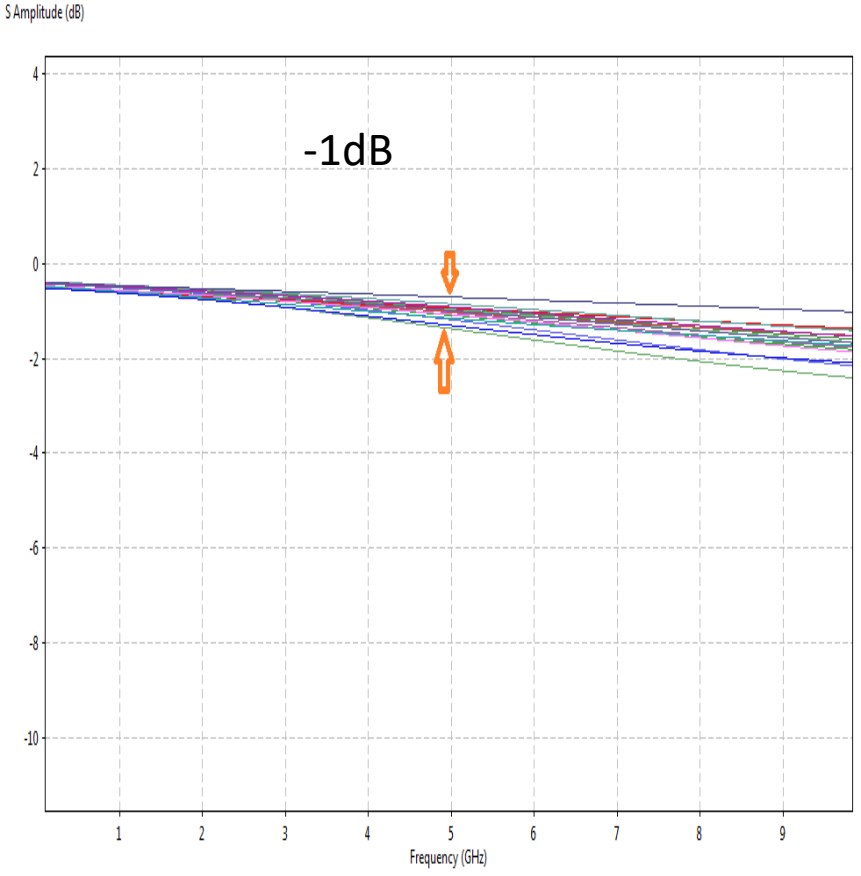


S-parameter generation

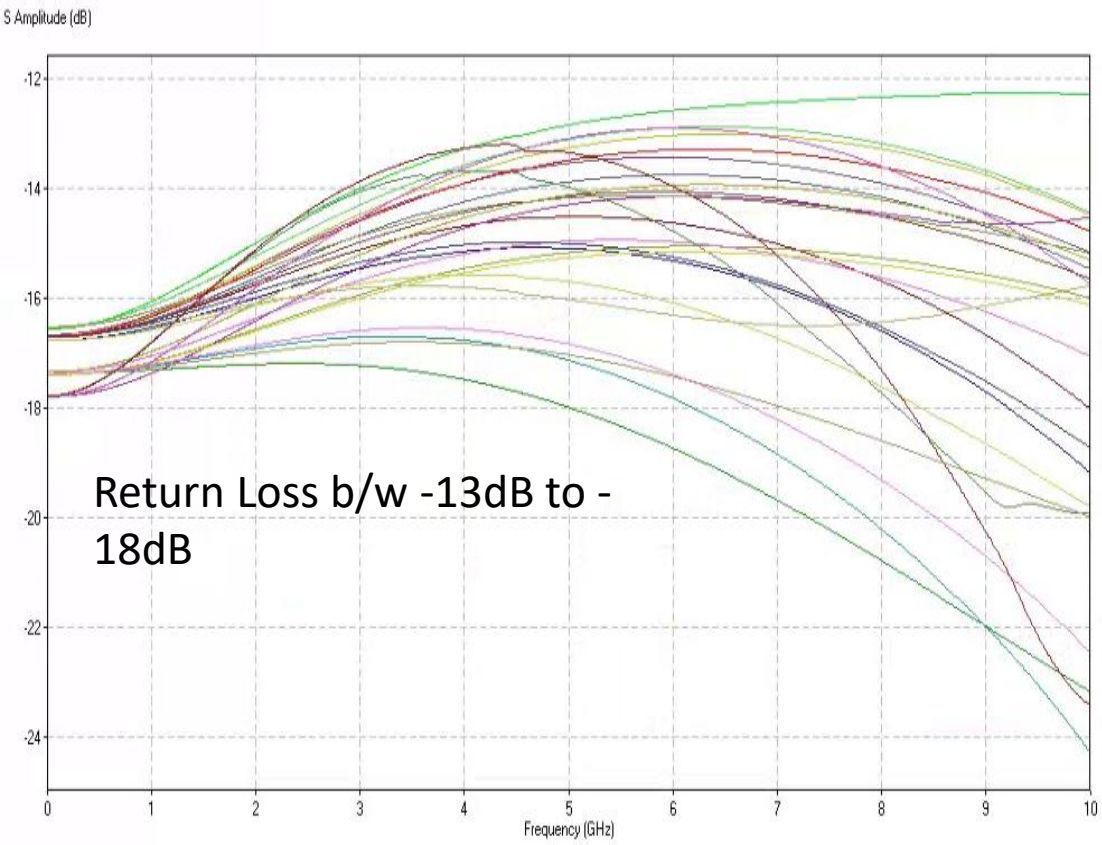


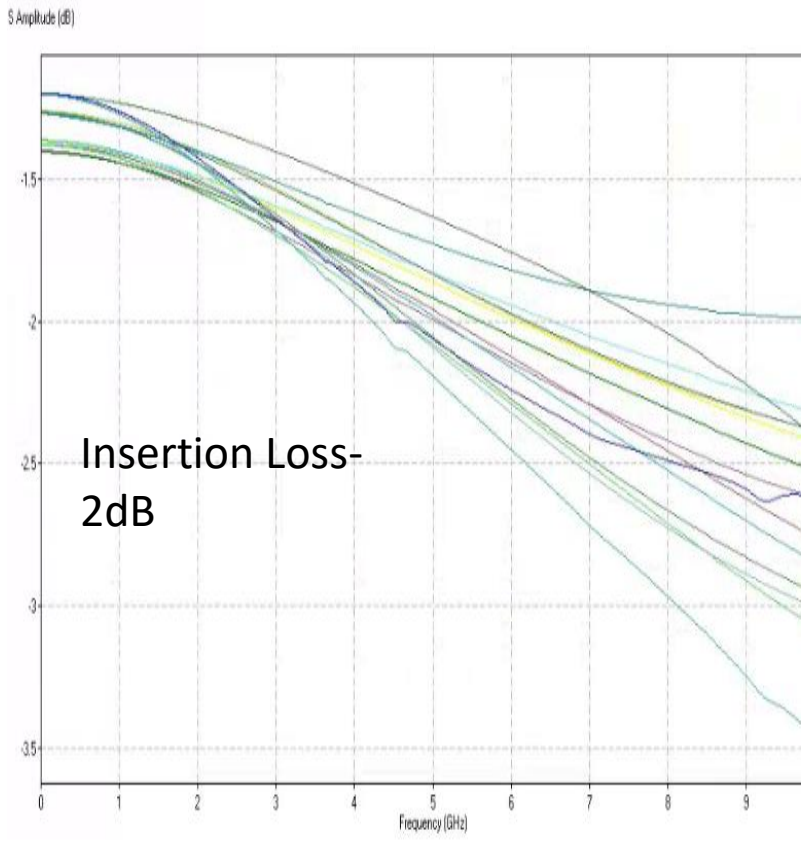
Return Loss and Insertion Loss in 2.5D IC/Silicon Interposer Design



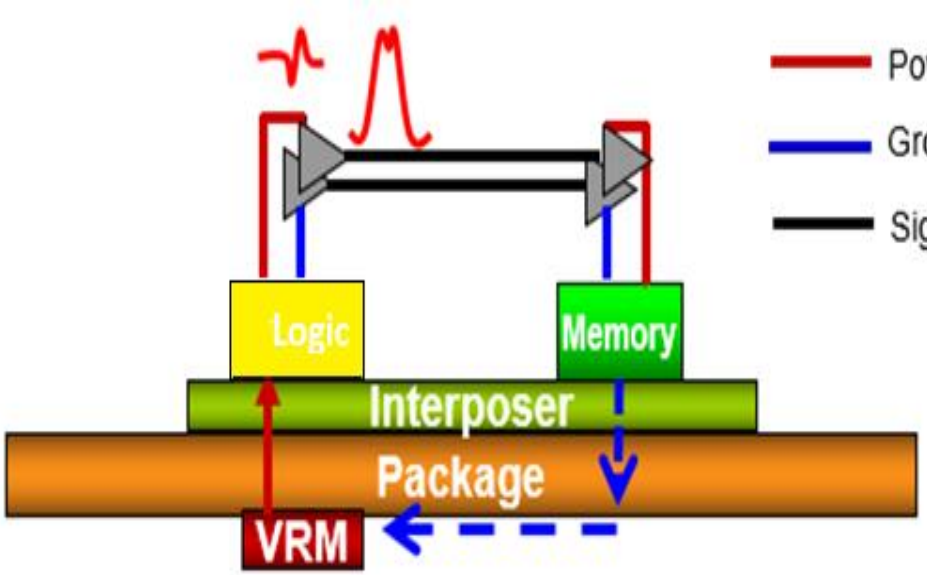


Return Loss and Insertion Loss in PoP Design



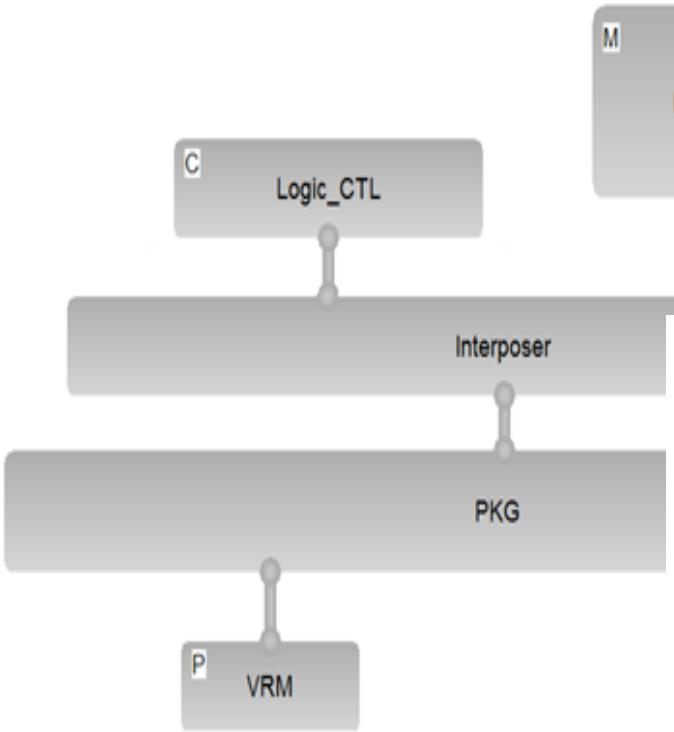


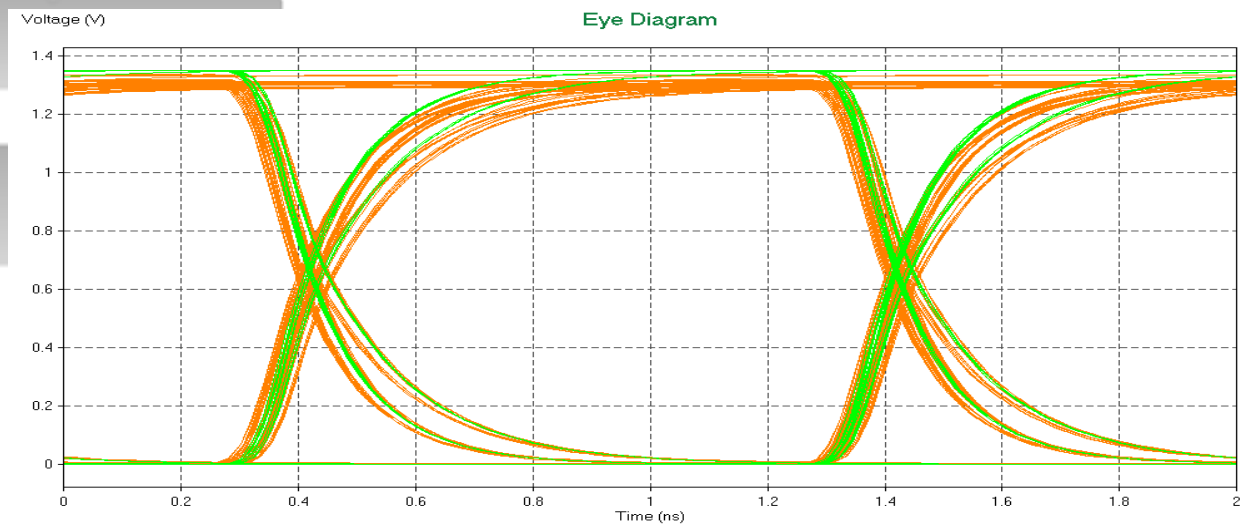
Time Domain Simulation



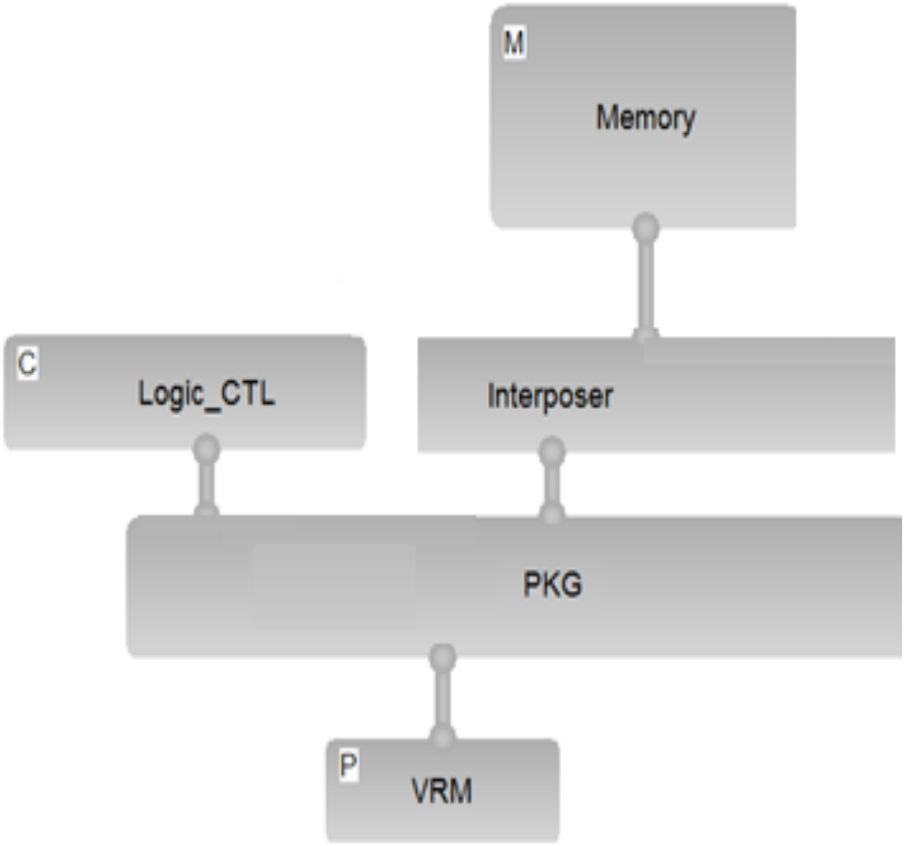
System Topology Construction → Setup Models and Interconnection → Setup Simulation Parameters → Run Simulation & Generate report → What-if analysis

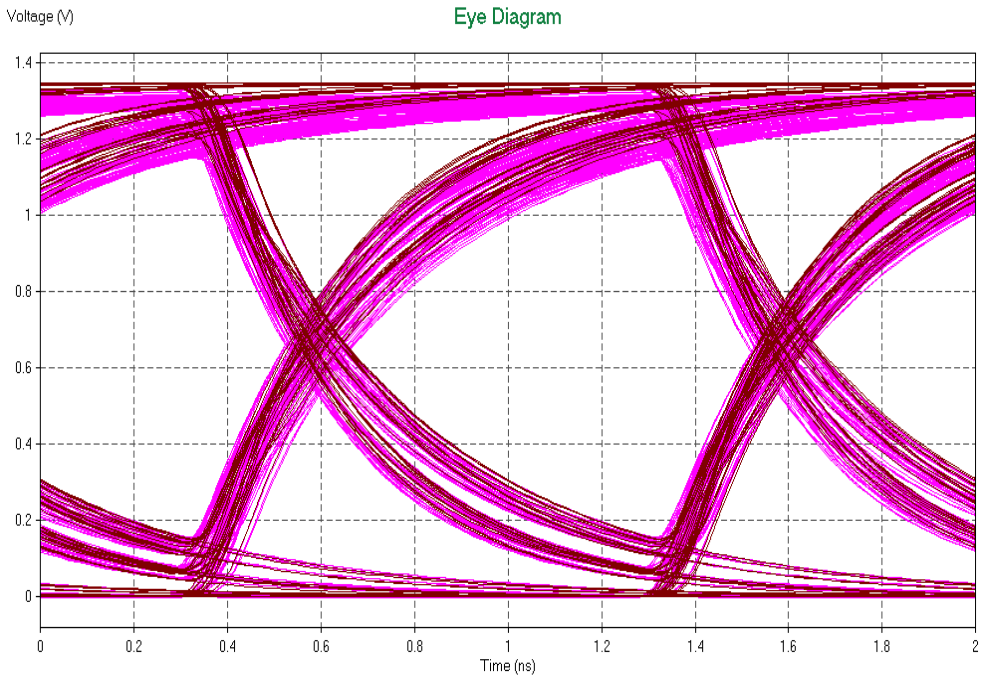
Si-Interposer Testbench and Simulation





POP Testbench and Simulation





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Conclusion

- Advanced-package design needs
  - Handling of large die(s) in terms of managing connectivity
    - Splitting single die into segments is useful
  - Use of Guard-Band to reduce cross-talk between traces is effective
- Si-Interposer can provide significant electrical performance improvements over traditional PoP technology
  - Return loss improved -10dB approximately
  - Insertion loss improved -1dB approximately
  - Eye opening is better in silicon interposer design

Acknowledgements

- John Park: Product Management Director, Cadence IC/Package Solutions