

The logo for EDICON 2018, featuring the text 'EDI' in a blue box above 'CON' in a white box with a blue border.

2018

Electronic Design **Innovation**
Conference & Exhibition

The event details: 'October 17-19 2018', 'Santa Clara Convention Center', and 'Santa Clara, CA'. The background of the header features a blue circuit board pattern with white circular nodes and connecting lines.

Signal Integrity Analysis on High-Density Silicon Interposer Package Technology for Next-Generation Applications

Surender Singh, Taranjit Kukal
Cadence Design Systems, Inc.



2018

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October 17-19 2018
Santa Clara Convention Center
Santa Clara, CA

Outline

- Introduction
- Silicon Interposer vs Package-on-Package (PoP)
- Test Vehicle
- Simulation Results
- Conclusions

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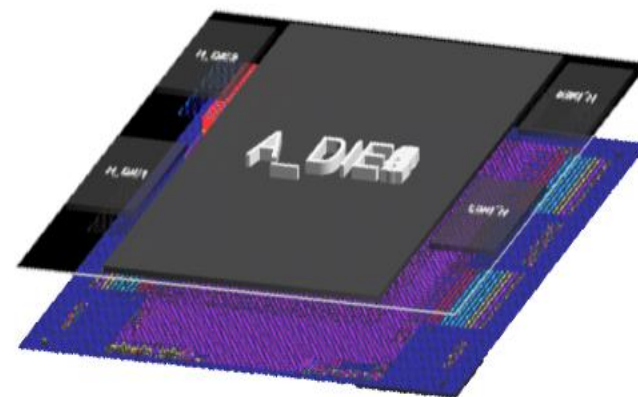
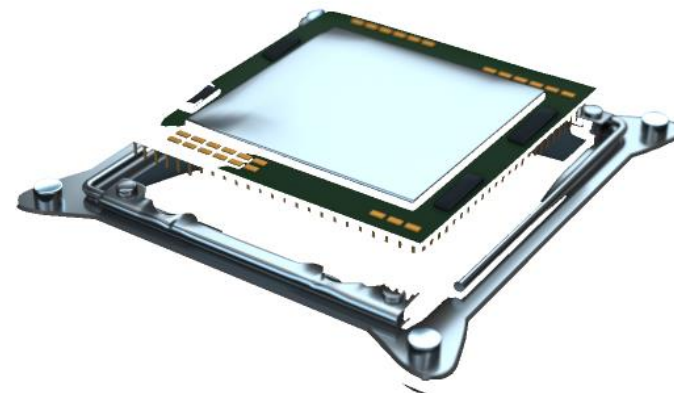
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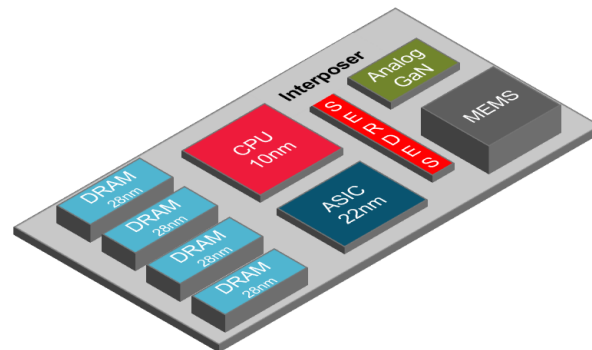
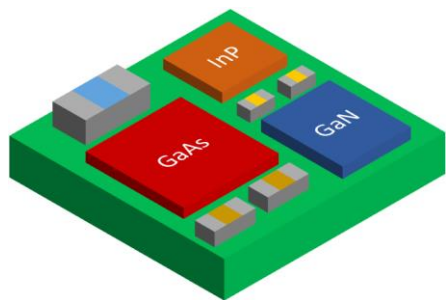
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Introduction

- Advanced packaging trends driven by
 - Heterogenous integration
 - More than Moore...
 - Advanced packaging technologies



Heterogeneous Integration... Transforming Moore's Law



Driven by PCB and Package Designers

Driven by IC Designers

Multi-Chip Module (MCM)

System in a Package (SiP)

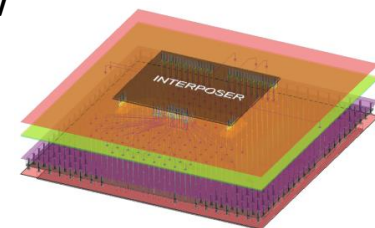
Heterogeneous Integration

1970

2005

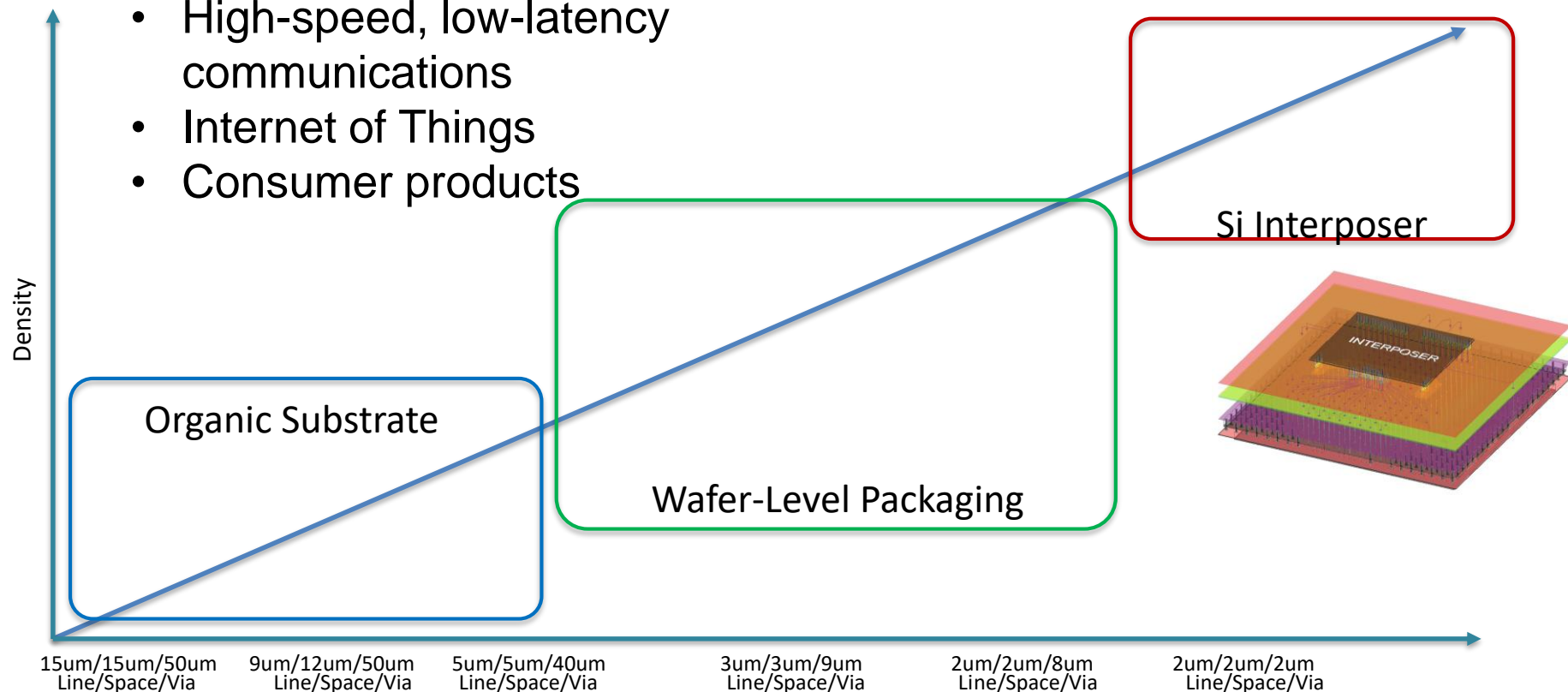
Now

Integrating multiple ICs, across multiple technologies and process nodes, into a single device/package



Advanced Packaging Technologies

- High-performance computing
- High-speed, low-latency communications
- Internet of Things
- Consumer products



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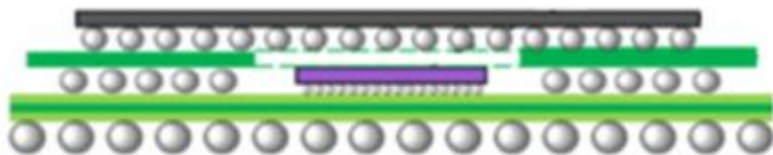
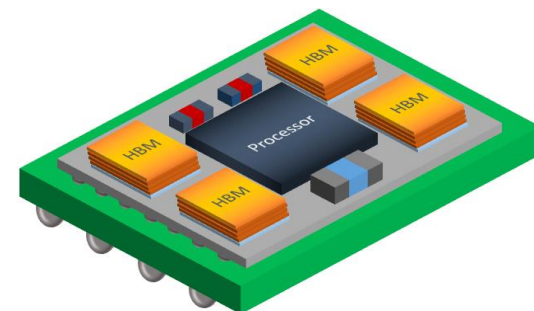
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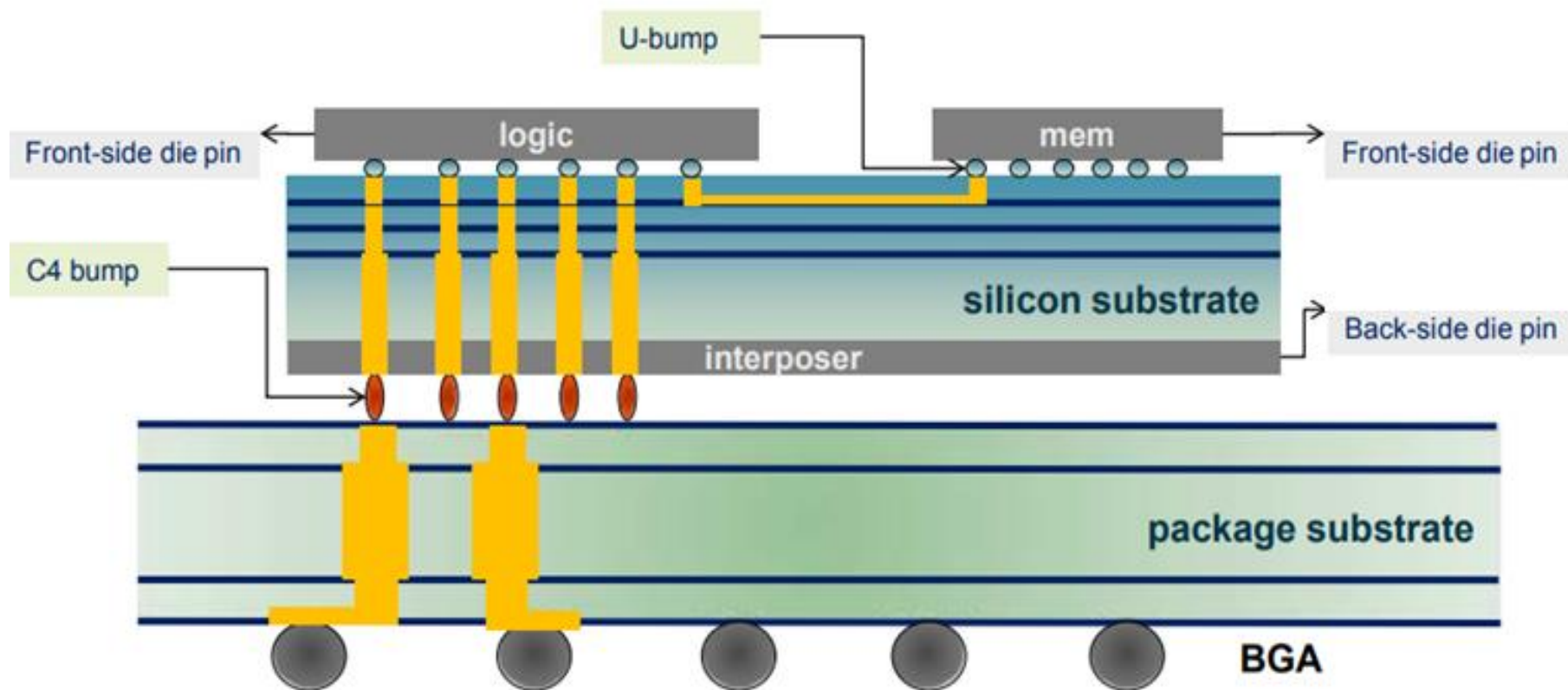
- Introduction
- **Silicon Interposer vs PoP**
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Silicon Interposer vs PoP

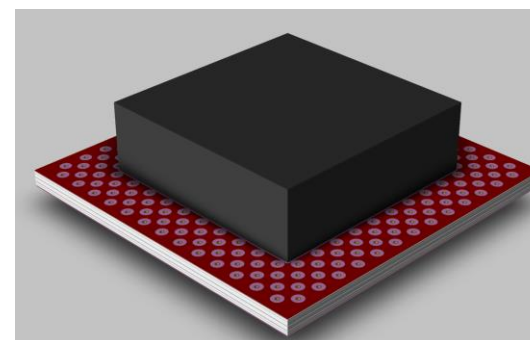
- Heterogeneous construction integrates the ASIC die multiple high-bandwidth memory (HBM) stacks; achievable through
 - Si-Interposer configuration
 - PoP configuration



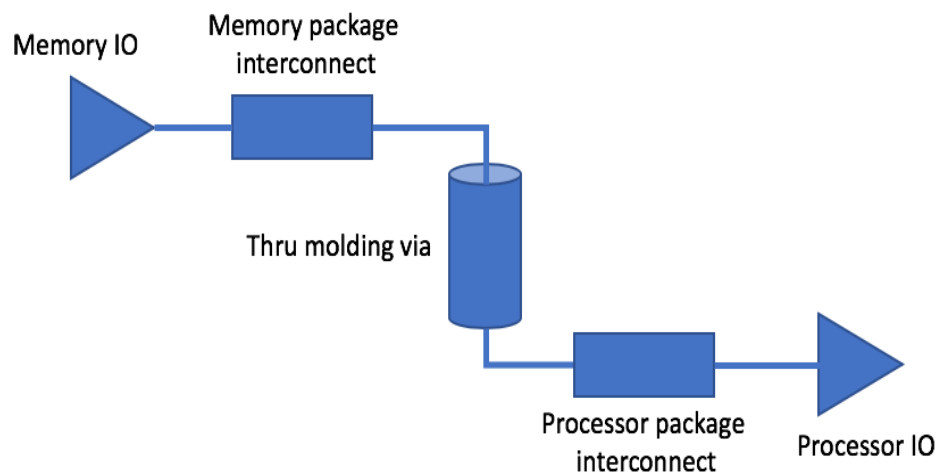
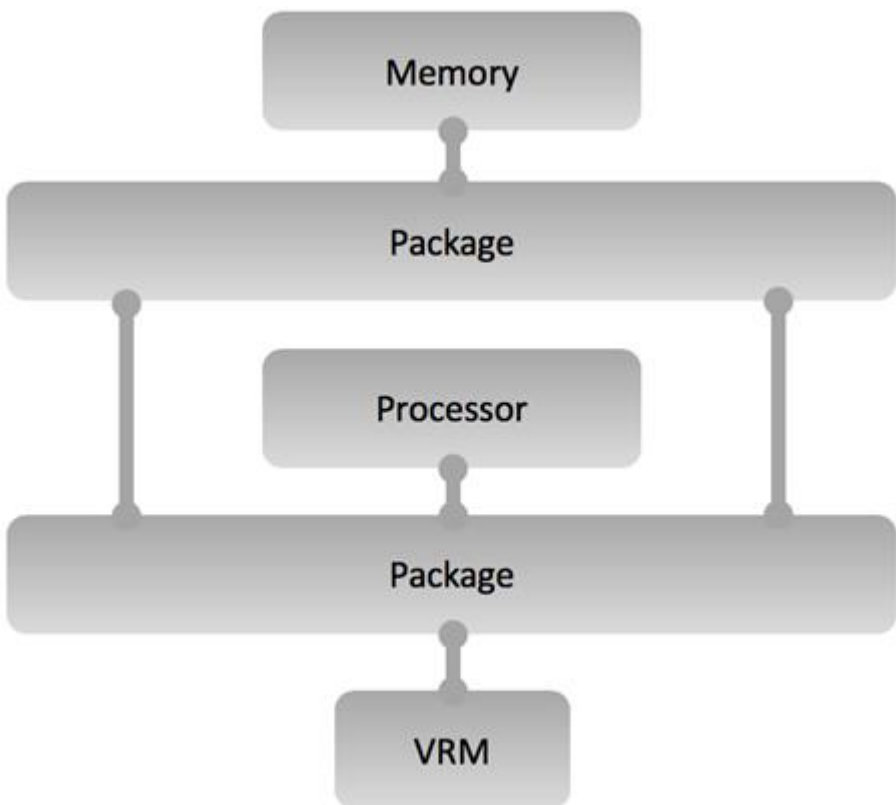
Si Interposer Overview



PoP Overview



PoP Interconnect Structure



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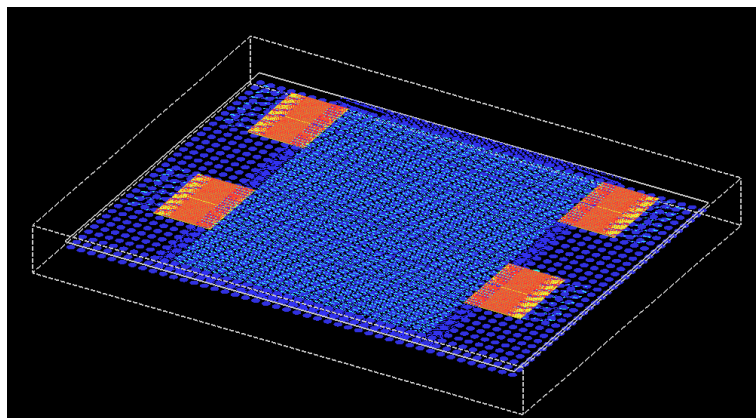
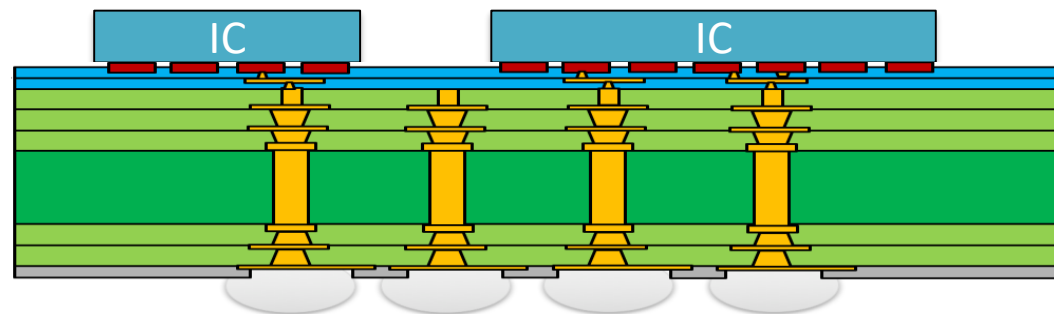
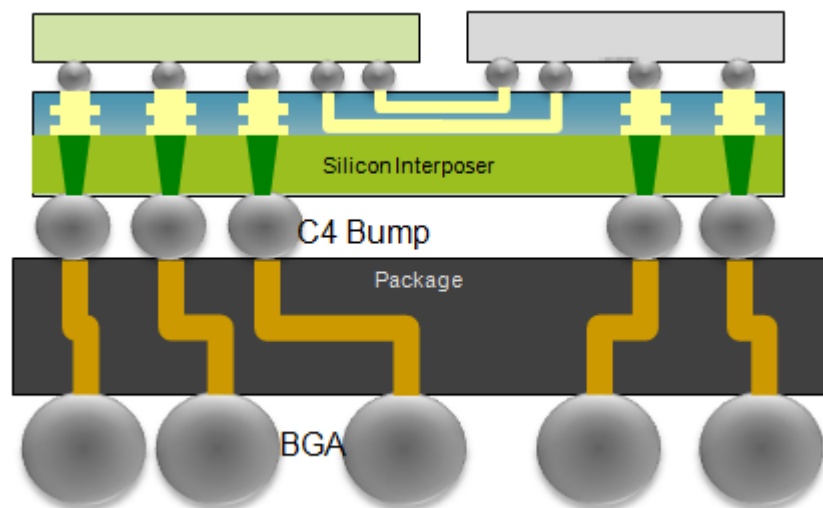
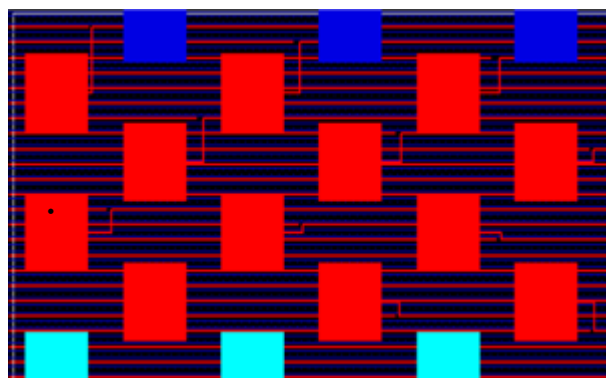
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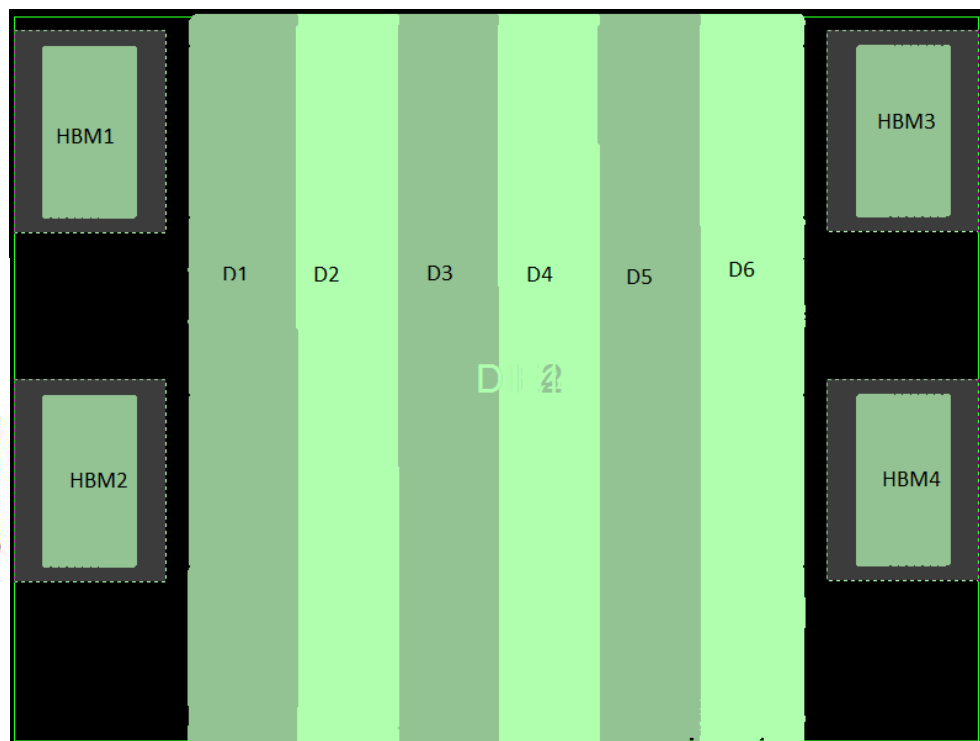
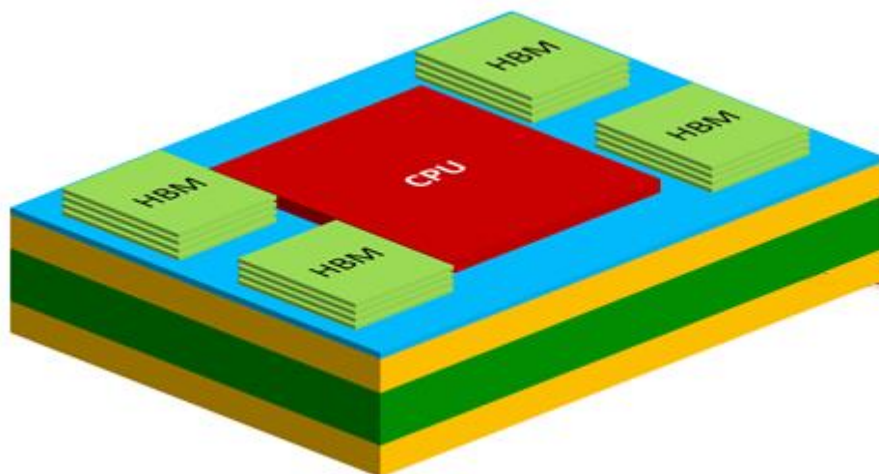
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Si-Interposer Design: Topology



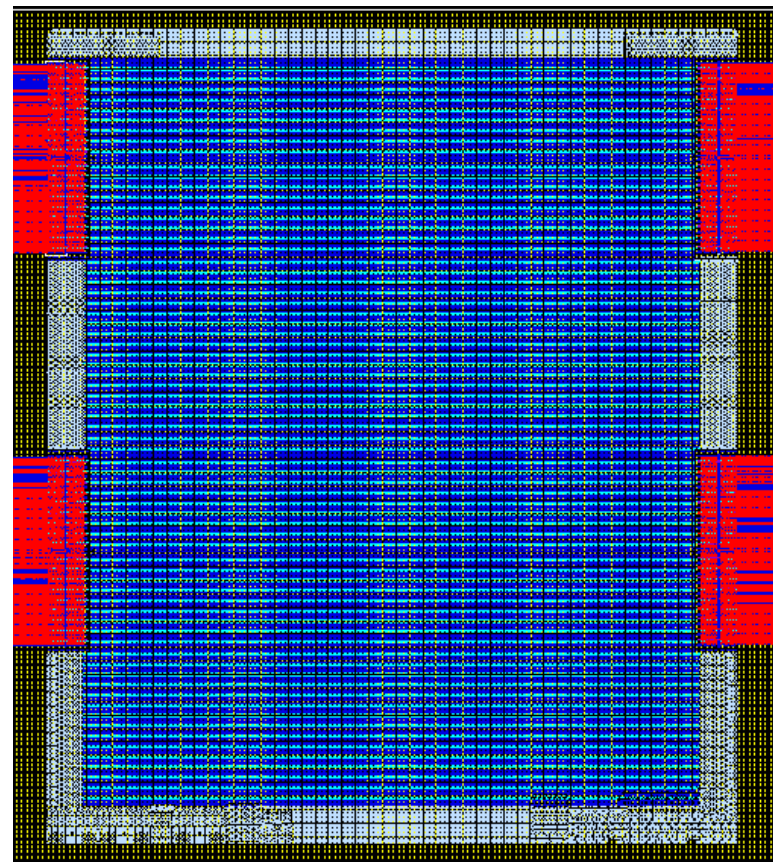
Si-Interposer Design: Components

- 4 HBM stacks
- 1 CPU
- Thin-film interposer



Si-Interposer Design: Specifications

- Total bumps: 188K bumps
 - ASIC die: 168K bumps
 - ASIC Die: Split into 6 dies (each 28k bumps)
- No of HBM: 4 dies
 - Each HBM: 5K bumps
 - total 20 K bumps





2018

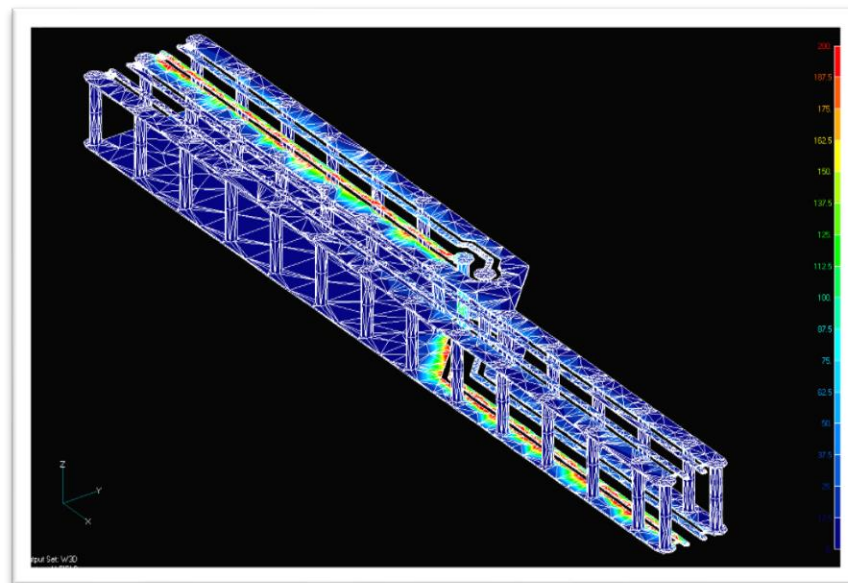
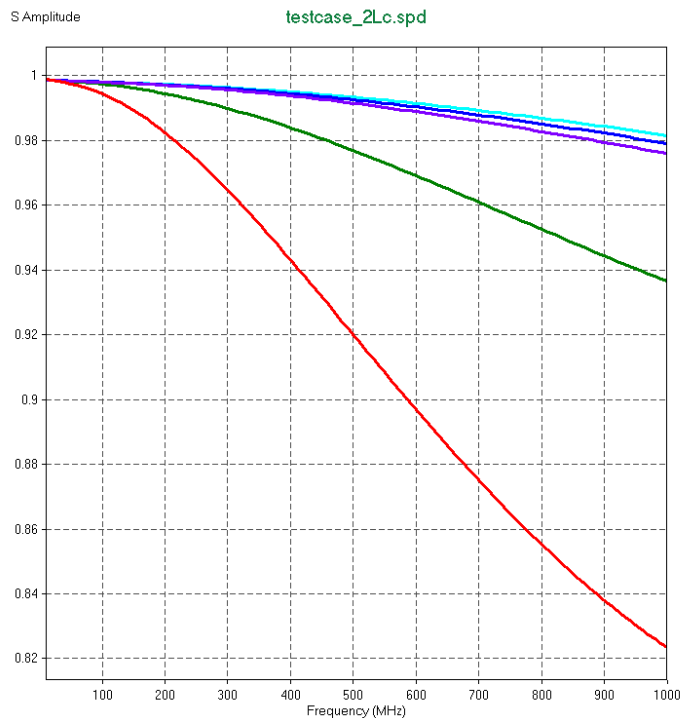
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Model Extraction in 3D-FEM

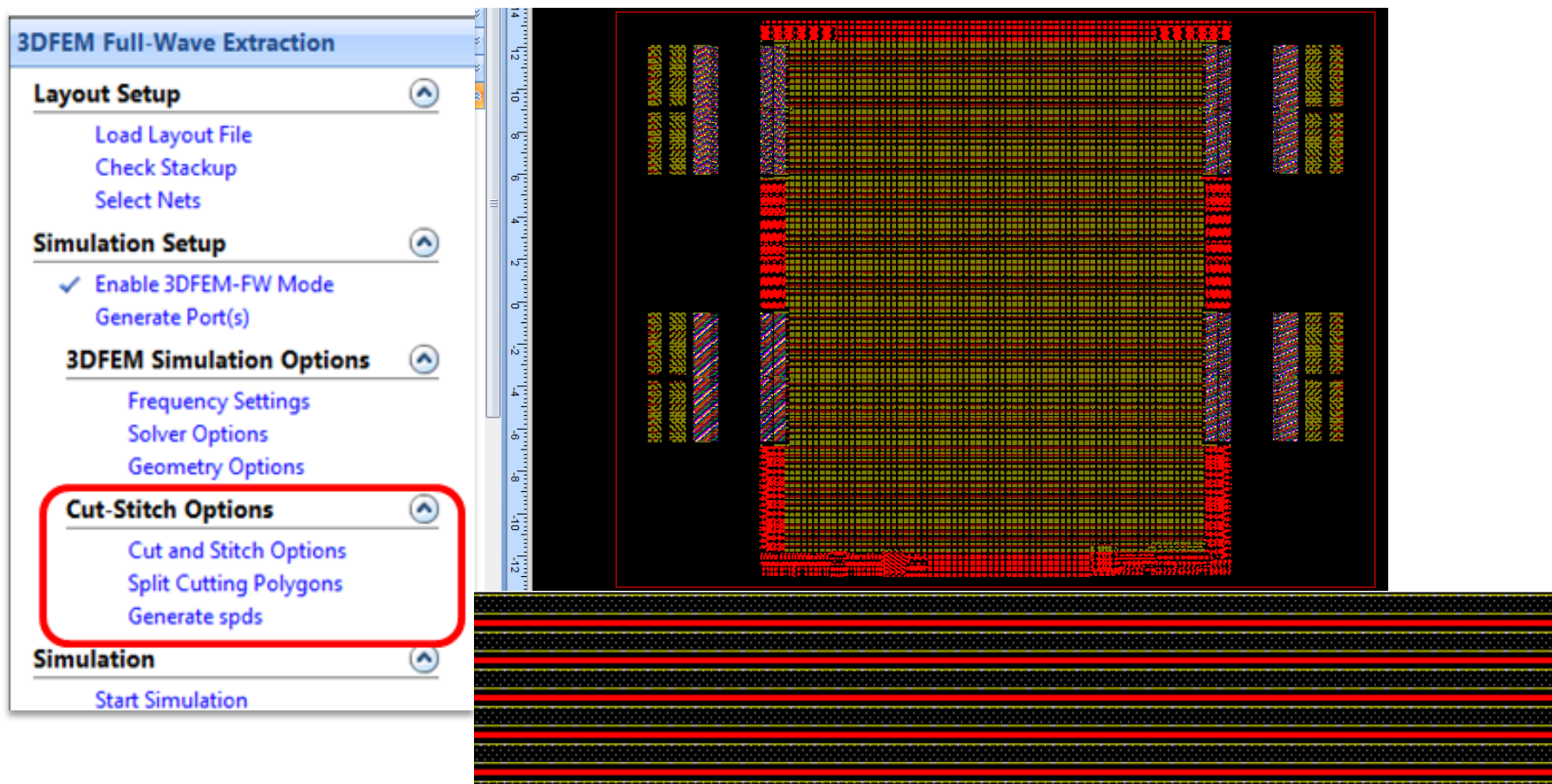


3D-FEM provides full-wave solver for accurate analysis of complex 3D structures

Adaptive meshing example

Variation of insertion loss during adaptive meshing

Model Extraction in 3D-FEM



3DFEM Full-Wave Extraction

- Layout Setup**
 - Load Layout File
 - Check Stackup
 - Select Nets
- Simulation Setup**
 - Enable 3DFEM-FW Mode
 - Generate Port(s)
- 3DFEM Simulation Options**
 - Frequency Settings
 - Solver Options
 - Geometry Options
- Cut-Stitch Options**
 - Cut and Stitch Options
 - Split Cutting Polygons
 - Generate spds
- Simulation**
 - Start Simulation

M2

Model Extraction in 3D-FEM

The screenshot displays the software interface for 3D-FEM simulation. The left-hand panel contains the following sections:

- 3D-EM Full-Wave Extraction**
 - Layout Setup
 - Load Layout File
 - Check Stackup
 - Select Nets
 - Simulation Setup
 - Enable 3D-EM Full-Wave Extraction Mode
 - Generate Port(s)
 - Multi-Terminal Circuits
 - 3D-EM Simulation Options
 - Frequency Settings
 - Solver Options
 - Geometry Options
 - Cut-Stitch Options
 - Enable Cut and Stitch
 - Cut and Stitch Options
 - CuttingZones Setting
 - Generate spds
 - Soc deembedding Options
 - Enable Soc deembedding
 - CuttingZones Setting
 - Generate spds
 - Simulation
 - Start Simulation
 - View, Check, Process Result
 - Network Parameter Display
 - Show Geometry 3D View
 - Show 3D-EM Field
 - Save 3D-EM Field

The main workspace shows a 3D-FEM model of a PCB layout. A cutting boundary is defined, and the 'Edit Cutting Boundary' dialog box is open, showing the following table:

In Use	Cut Outside	Name
<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	CuttingPolygon01

At the bottom right, there is a 3D-FEM model of a PCB with a die and pads. Below it, there are buttons for 'Auto Generate (by nets)', 'Preview', and 'Save Preview result As'. A checkbox 'Include enabled signal shapes' is also present.



Port

Port

S-Parameter Extraction with 3D-FEM

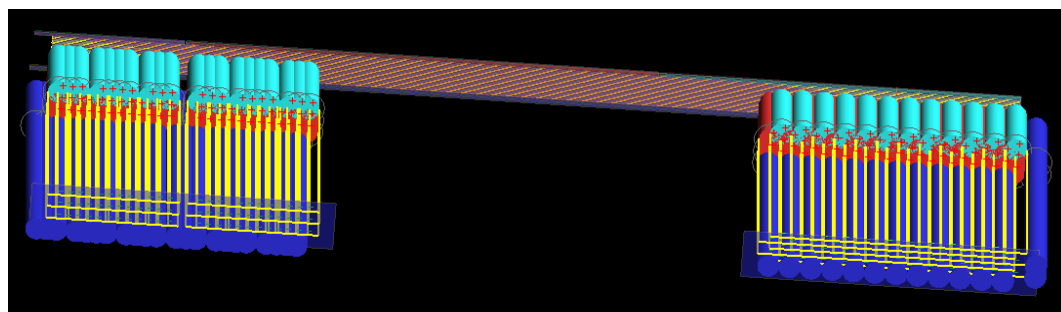
Port

128 enabled ports out of 128 total ports

Port	Ref Z(Ohm)	Width(...)	Rotation
Port21::H_DIE2_2411	50	0.1	0
Port22::H_DIE2_2412	50	0.1	0
Port23::H_DIE2_2520	50	0.1	0
Port24::H_DIE2_2521	50	0.1	0
Port25::H_DIE2_2631	50	0.1	0
Port26::H_DIE2_2632	50	0.1	0
Port27::H_DIE2_2740	50	0.1	0
Port28::H_DIE2_2741	50	0.1	0
Port29::H_DIE2_2851	50	0.1	0
Port30::H_DIE2_2852	50	0.1	0
Port31::H_DIE2_2960	50	0.1	0
Port32::H_DIE2_2961	50	0.1	0
Port33::H_DIE2_3071	50	0.1	0
Port34::H_DIE2_3072	50	0.1	0
Port35::H_DIE2_3180	50	0.1	0
Port36::H_DIE2_3181	50	0.1	0

Port Grouping for Enabled Power Nets
Assumes equal-current at each port within a group

Auto-ports
generation



Frequency
sweep



Frequency Ranges

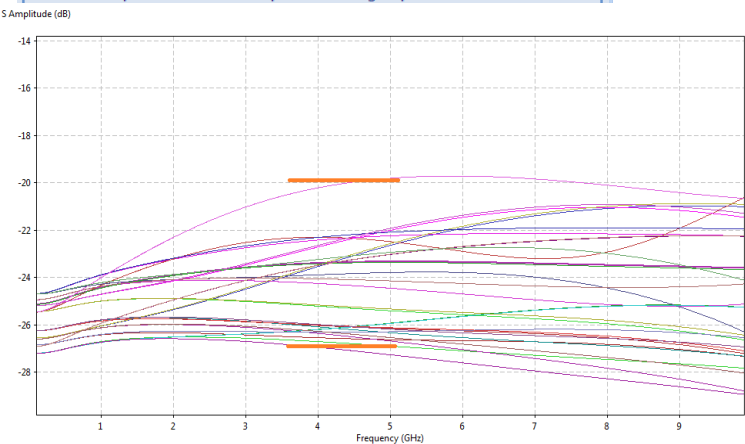
Solution Frequency :

Frequency Min :

Frequency Max :

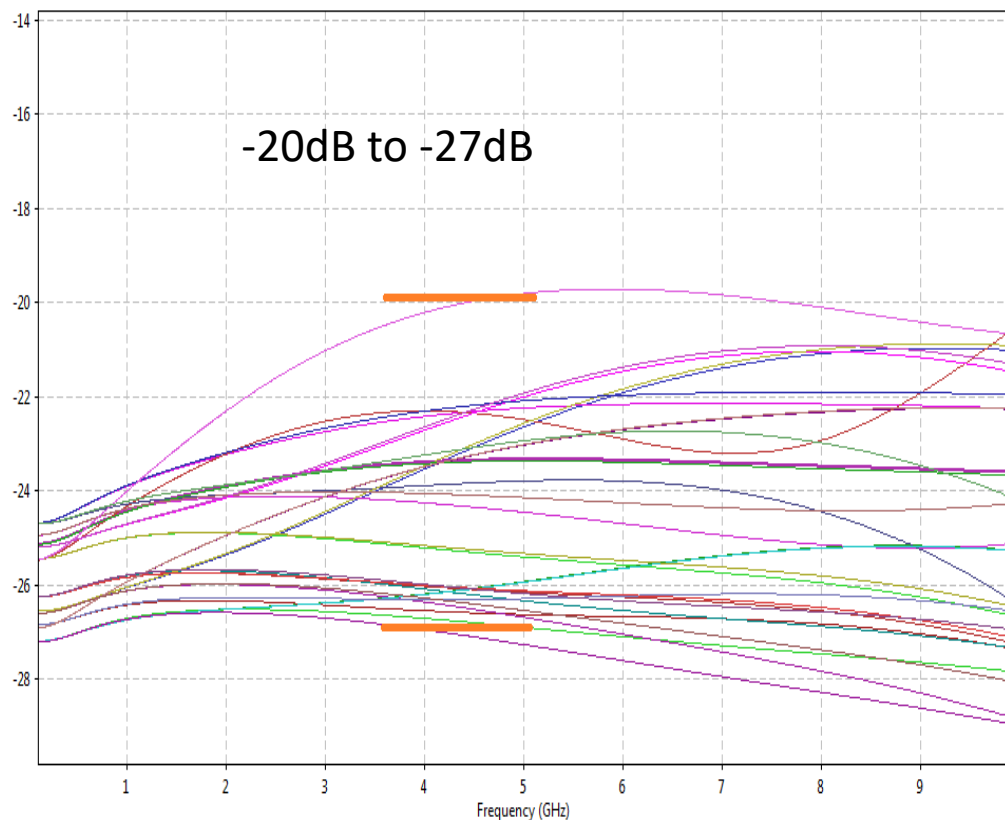
Explicit DC Solution DC Refinement

S-parameter
generation

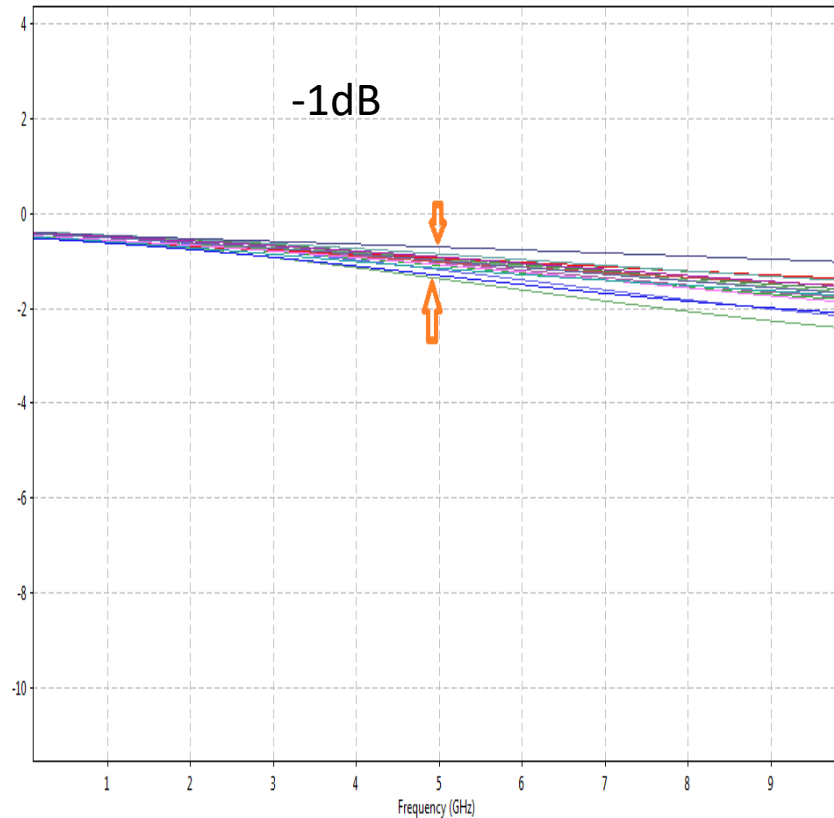


Return Loss and Insertion Loss in 2.5D IC/Silicon Interposer Design

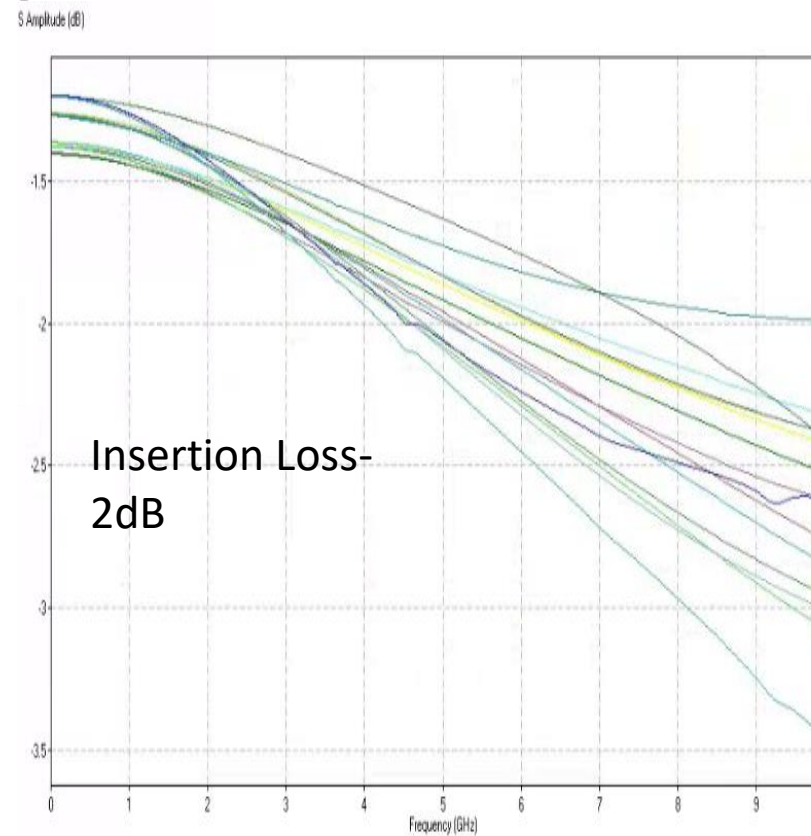
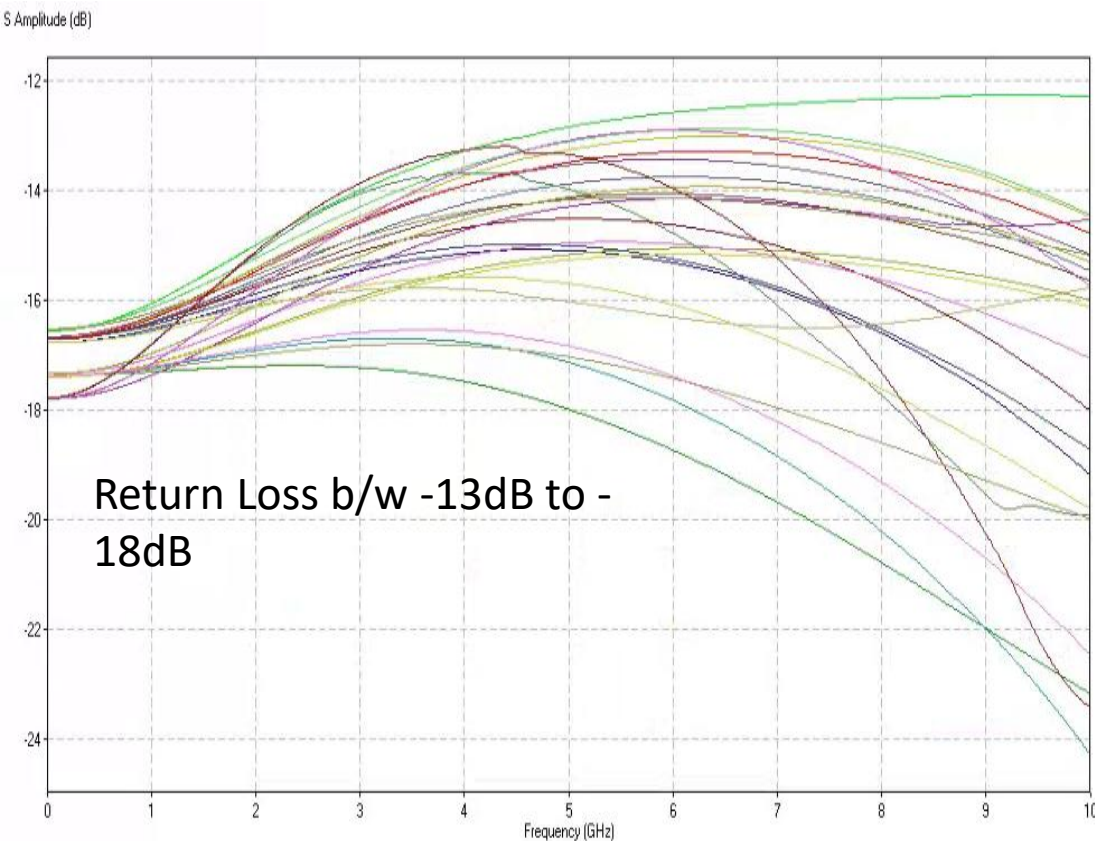
S Amplitude (dB)



S Amplitude (dB)



Return Loss and Insertion Loss in PoP Design



Time Domain Simulation

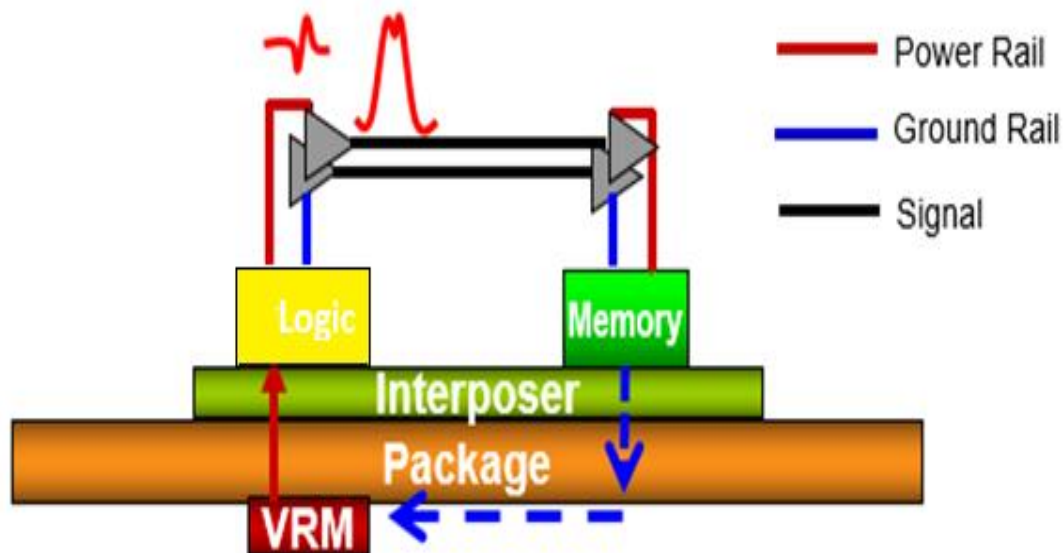
System Topology
Construction

Setup Models and
Interconnection

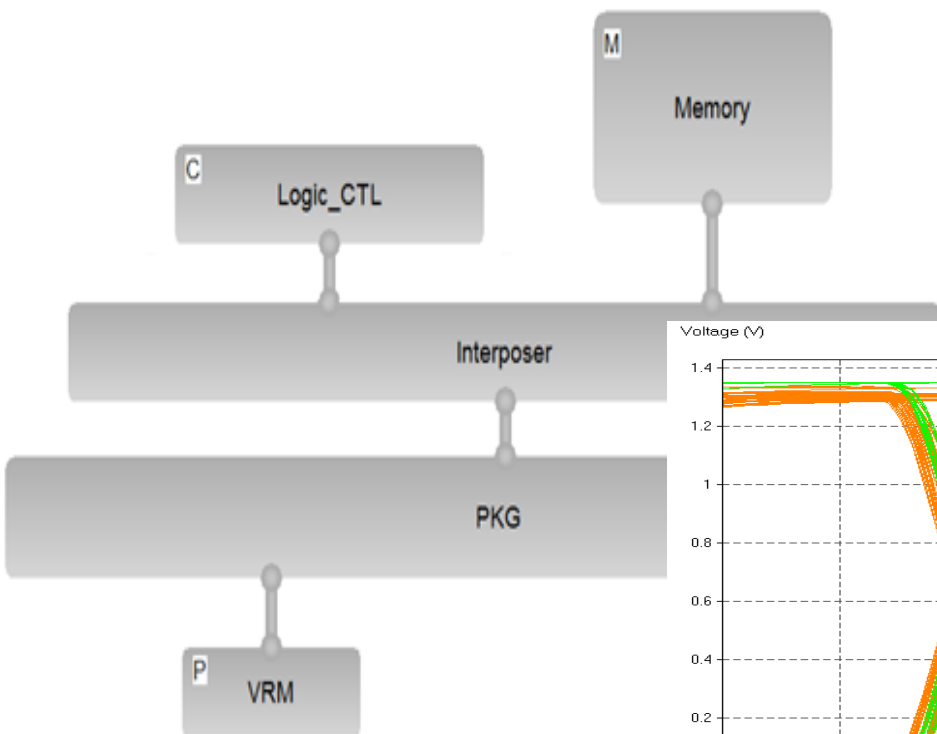
Setup Simulation
Parameters

Run Simulation
&
Generate report

What-if analysis

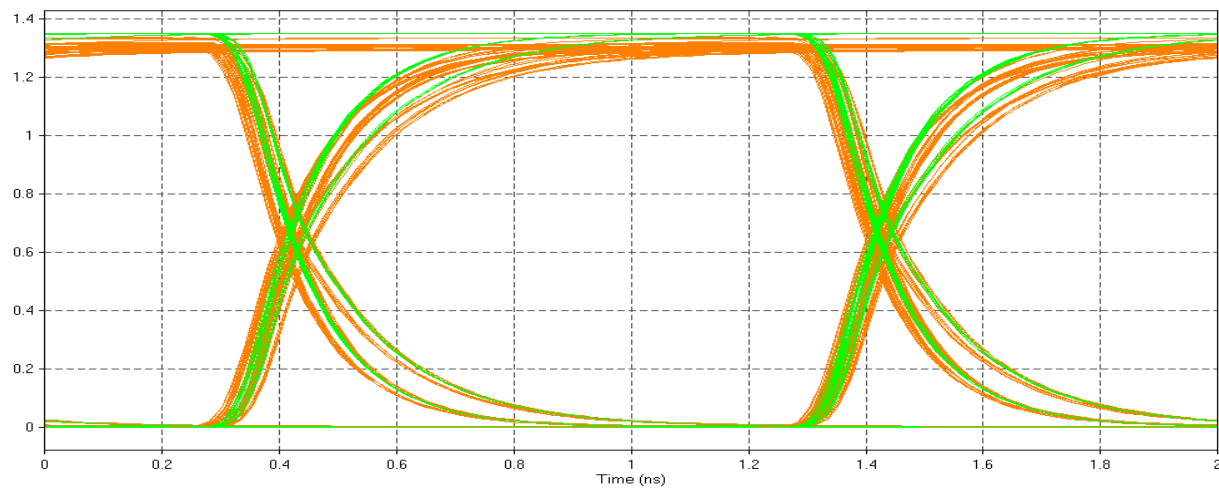


Si-Interposer Testbench and Simulation

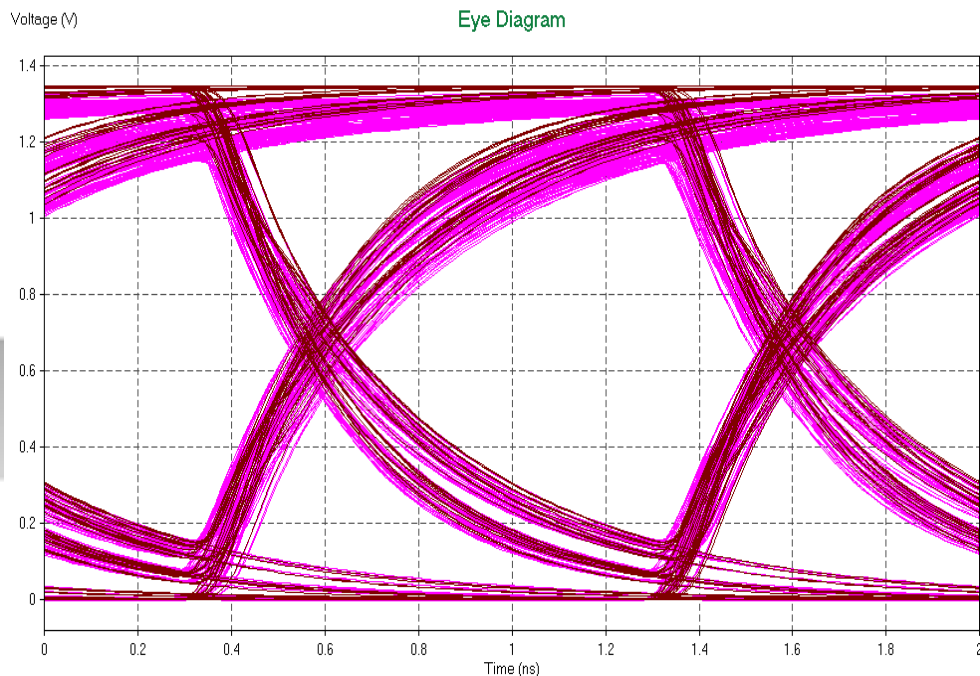
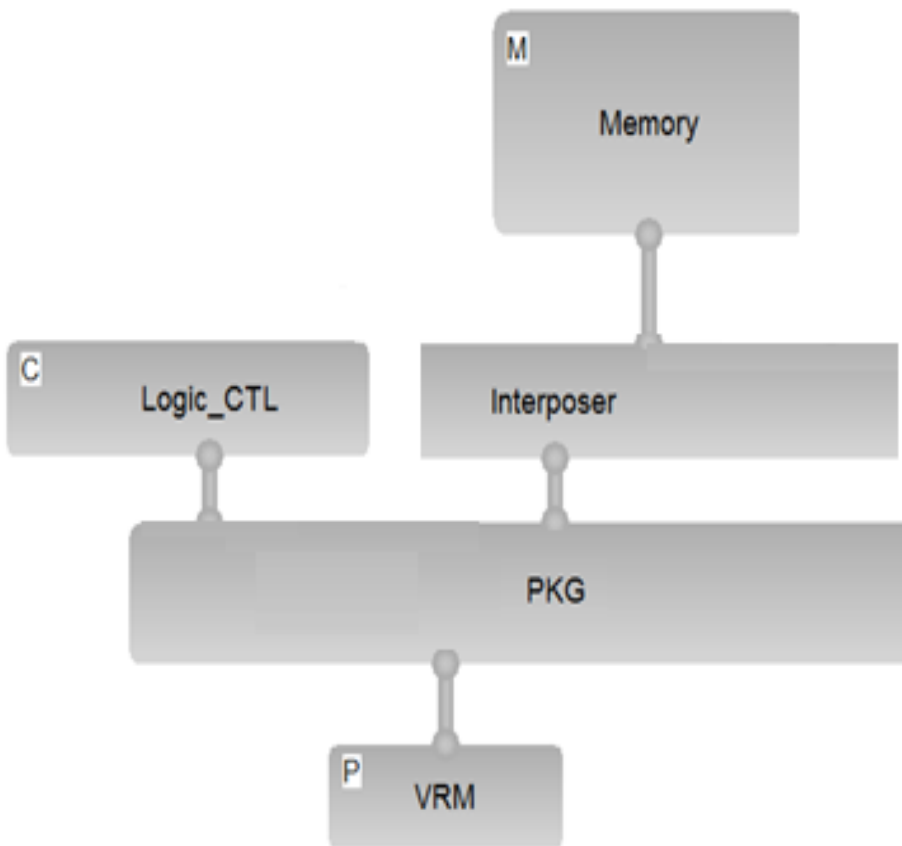


Voltage (V)

Eye Diagram



POP Testbench and Simulation



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- Advanced-package design needs
 - Handling of large die(s) in terms of managing connectivity
 - Splitting single die into segments is useful
 - Use of Guard-Band to reduce cross-talk between traces is effective
- Si-Interposer can provide significant electrical performance improvements over traditional PoP technology
 - Return loss improved -10dB approximately
 - Insertion loss improved -1dB approximately
 - Eye opening is better in silicon interposer design

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Acknowledgements

- John Park: Product Management Director, Cadence IC/Package Solutions