

IEEE P370: A fixture design and data quality metric standard for interconnects up to 50 GHz

Jay Diepenbrock, SIRF Consultants, LLC Xiaoning Ye, Intel Corp. Jason Ellison, Amphenol AICC Mikheil Tsiklauri, Missouri Inst. of Science & Technology



Outline

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Background

- Increased accuracy needed for simulation of systems using devices operating with significant spectral content at 50 GHz; e.g., 56 Gb/s
- Accurate de-embedding method needed for devices characterized to 50 GHz
- Different structures, different methods in use in industry
 - Lack of consistency
 - Proprietary algorithms, tools
 - Poor results due to poor fixture design
 - Poor quality S-parameter data -> inaccurate simulation
 - No objective way to evaluate quality of results
- P370 is not a calibration standard (see P378, now expired)



Test connector guidance

 Good quality connectors and PCB launches needed for devices characterized to 50 GHz

Connector inside diam., mm	7	3.5	2.92	2.4	1.85
Rated max. frequency, GHz	18	33	40	50	65
TE11 onset limit freq., GHz	19.4	38.8	46.5	56.5	73.3



Conventions

• DUT port labeling



• Component/port labeling



"FIX-DUT-FIX"



Conventions

- Touchstone File Header info proposed by IEEE P370
 - Data source measured, calculated, simulated
 - Component type
 - De-embed structure 1X reflect Short, 1X reflect Open, 2X thru
 - Calibration structure Short, Open, Load, TRL Line 1, etc.
 - DUT
 - Composite FIX-FIX (2x thru), FIX-DUT-FIX, etc.
 - Fixture
 - Calibration Method SOLT, TRL
 - De-embedding Method 1x Reflect, 2x Thru, Z-corrected 2x thru



De-embedding objective: Separate the DUT from the fixture



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Test Fixture Design Criteria

- Test connector guidance
- Topology and electrical parameter limits for de-embedding structures
 - 1x Reflect
 - 2x thru
 - Single-ended fixture crosstalk
 - Mixed mode fixture crosstalk
- Fixture Electrical Requirements limits on
 - Insertion Loss
 - Return Loss
 - Insertion/return loss separation
 - Intra fixture crosstalk
 - Impedance variation difference between fixture in 2x thru and FIX-DUT-FIX
 - (Differential fixtures) Differential to Common Mode Conversion
 - Line to line or Pair to pair skew



Test Fixture Design Criteria

- Introduce concept of Compliance "Classes" to Electrical Criteria
 - FER 1, Insertion loss
 - Class A = min. -10 dB at all frequencies
 - Class B = min. -15 dB at all frequencies
 - Class C = min. -15 dB at all frequencies
 - FER 2, Return loss
 - Class A = max. -20 dB at all frequencies
 - Class B = max. -10 dB at all frequencies
 - Class C = max. -6 dB at all frequencies
 - FER 3, Insertion/Return loss separation
 - Class A = max. 5 dB at all frequencies
 - Class B = max. 0 dB at all frequencies
 - Class C = max. 0 dB at all frequencies



- Compliance "Classes," cont'd
 - FER 4, Intra fixture crosstalk less than DUT
 - FER 5, Impedance Variation difference between FIX in 2x thru and FIX-DUT-FIX
 - -> Is the 2x thru really representative of <u>all</u> DUT paths?
 - Class A = max. ±2.5 dB at all frequencies
 - Class B = max. ± 5 dB at all frequencies
 - Class C = max. ± 10 dB at all frequencies
 - FER 6, Differential to Common Mode Conversion max. -15 dB at all freqs.
 - FER 7, Line to line or pair to pair skew max.



Verification Structures

• Beatty







Verification Structures, cont'd

• Line structure





De-embedding methods

• 1x Reflect – uses single Open or Short standard



- Measured s11 data converted to time domain
- Fixture s11 calculated from converted, measured s11 data
- 2x thru calculated from either time domain converted s11 and measured s11 (Keysight patent) or additional measured standard 1x data



De-embedding methods, cont'd

• 2x thru – uses measured 2x thru



- Measured s11 data converted to time domain, reflect data used to calculate fixture s11
- Results dependent on Z match between 2x-thru and FIX-DUT-FIX, can cause causality errors



De-embedding methods, cont'd

- 2x Impedance-corrected thru uses 2x thru
 - Compensates for Z mismatch between 2x-thru and FIX-DUT-FIX, reduces causality errors
- De-embedding algorithm acceptance criteria compare extracted data to known-good
 - Time domain
 - Frequency domain
 - Error vector magnitudes
 - Three quality classes



• Synthesized Library





• Synthesized Library - sample



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Comparison of S-parameters – Error vector



$$\mathsf{EF}_{ij}(f) = \mathsf{mag}\left[\mathsf{S}_{ij}^{\mathsf{A}}(f) - \mathsf{S}_{ij}^{\mathsf{B}}(f)\right]$$

$$rEF_{ij} = \frac{mag\left[EF_{ij}(f)\right]}{0.5 \times mag\left[S^{A}_{ij}(f) + S^{B}_{ij}(f)\right]}$$



• Plug and Play Boards





• Plug and Play Board example





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• Demonstration Boards



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Annexes in the P370 Draft

- Network parameters, incl. multiports
- Calibration and de-embedding
- Sensitivity analysis with synthesized library elements



Annexes: Best Practices

- Design & manufacturing considerations
 - Trace geometry, coupling, routing
 - Conductor plating
 - Dielectric material
 - Surface roughness
- Fixture Design
 - Via design
 - Test connector launches coaxial via structures
 - Stitching vias
 - Ground plane cutouts



Best Practices, cont'd

- Test equipment, cables
- Max. frequency extrapolation
- Analytical input pulse creation
- DC extrapolation
- Interpolation



More Information

See https://standards.ieee.org/develop/project/370.html

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