Advances in Recent PCB Design Verification flows

Today's RF/mixed-signal printed circuit boards (PCBs) employ complex board structures to support greater functionality for specific applications. For PCBs in mobile devices, the interconnect and board dimensions are rapidly shrinking as designs rely on a reduced number of highly-integrated modules, each with high pin-counts. At the same time, boards for networking and computer applications are getting larger, with more interconnect and plane layers.

Within these densely-populated, multi-layer boards, integration of high-speed data lines and RF circuitry poses a potential risk to system performance because of coupling (cross talk) and other parasitic behavior along the signal traces. PCB design based on EM analysis is critical to verifying performance and allows designers to mitigate the effects of parasitic behavior.

The incorporation of EM analysis into the design verification flow has evolved with enhanced automation to fit the needs of a diverse range of applications. With complex PCB designs, this flow includes interoperability between tools via open data exchange and the ability to easily set up the EM analysis for the board section or traces of interest, as well as the EM analysis itself.

Capability in the latest version of the NI AWR Design Environment platform has introduced a PCB import wizard to accelerate EM verification of PCBs by enabling users to isolate areas of interest with powerful net and area selection of imported designs originally created in board layout tools from leading CAD vendors. As a result, EM analysis is simplified to address just the areas/nets that require further simulation and engineering review. This paper walks through an example that highlights the capabilities in this new wizard that enables designers to isolate and characterize critical traces within complex multi-layer configurations.

PCB Design

In this example, a Zuken designed PCB (Figure 1) is imported using NI AWR software. To streamline the EM analysis/verification of this board, it is prudent to obviate the parts of the board that do not impact the performance.

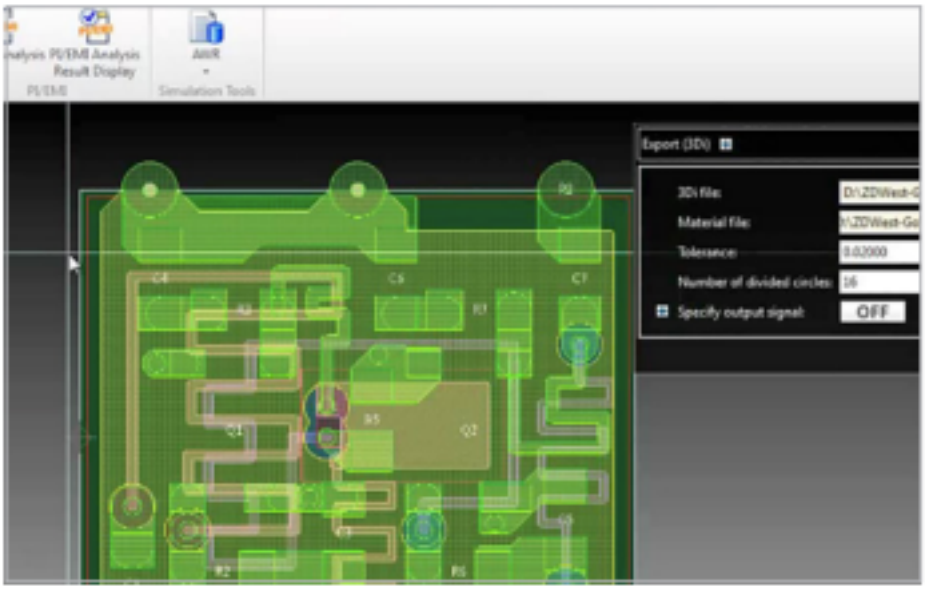

Figure 1. Zuken PCB imported into NI AWR software using the V14 PCB import wizard.

The import process begins by simply pointing to the file of choice and selecting it. The wizard imports XML files using the IPC-2581 standard format developed by the ICP-2581 Consortium for PCB and assembly manufacturing description data and transfer methodology.
The wizard also supports 3Di and ODB++ formats.

Once the file is selected, all layers, nets, and stackup information that are in the PCB file are directly read by the wizard and imported into the RF design software which will support the EM verification. Designers can specify exactly which layers and nets they want to import. By executing the *Copy to EM Structure* command, the layout is then sent to the EM simulator of choice, in this example the AXIEM planar EM simulator within the NI AWR Design Environment platform was chosen, however the EM structure could also have been solved by supported EM simulators such as ANSYS HFSS, CST Microwave Studio or Sonnet Software. These 3rd party simulators are supported through the EM socket available through the design environment. Ports can easily be added to the component pins and pads by selecting *Create Ports From PCB Pins*. The wizard then runs the information specified by the designer, imports the file, and produces a layout of the entire board, ready for EM simulation.

Once the board is imported, layer visibility options can be selected to make it easier to see exactly what is to be simulated. In this example, the region to be simulated is at the top (Figures 2 and 3).

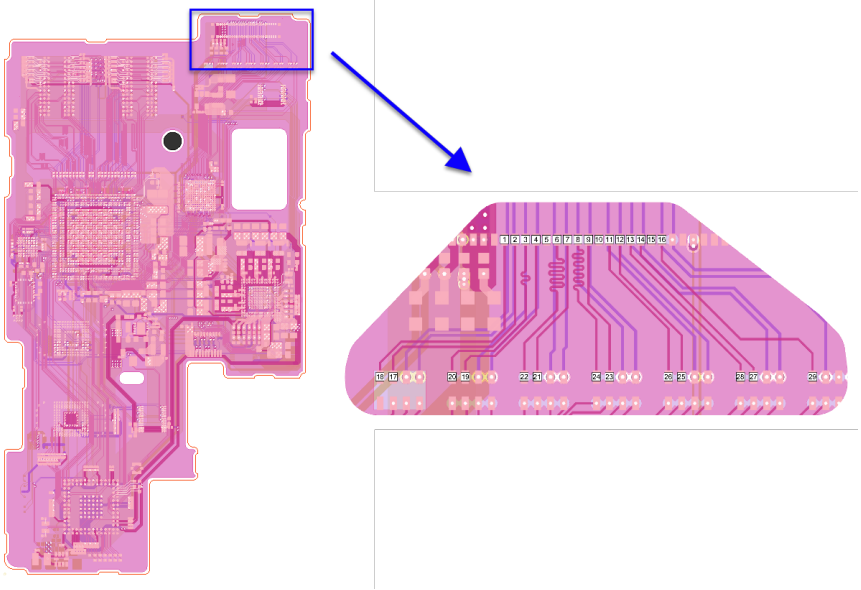

Figure 2: The complete PCB layout with the region of interest shown at the top.

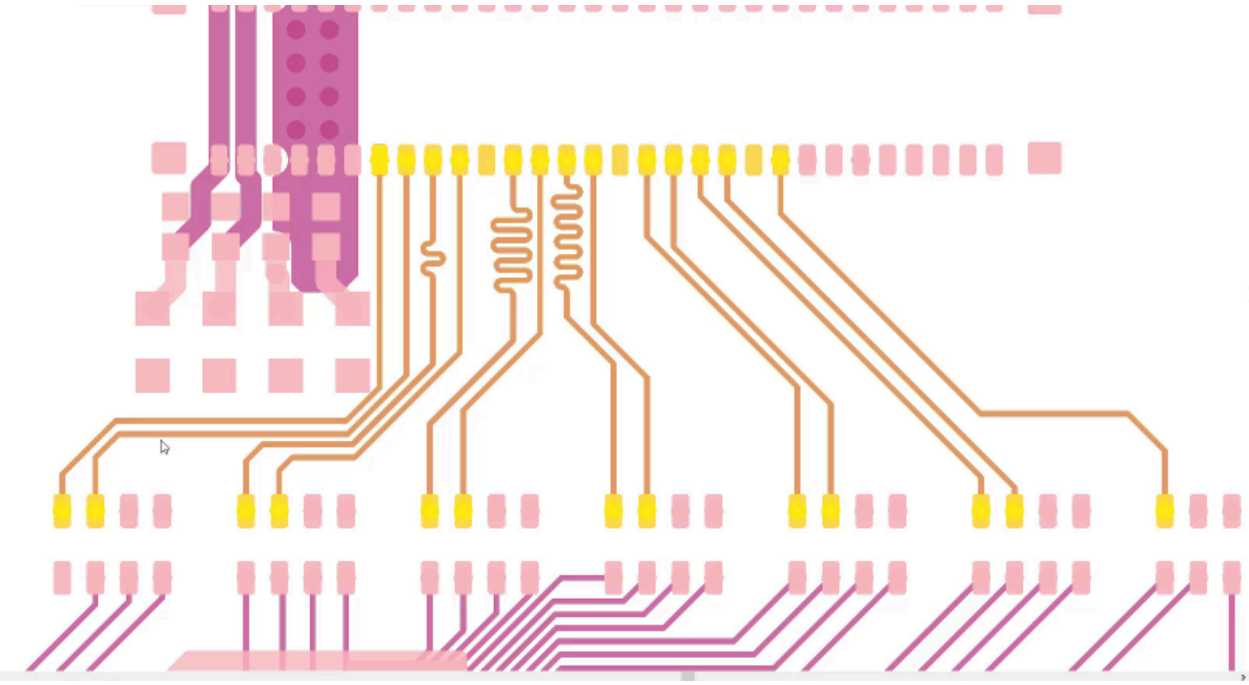

Figure 3. Detail of the top portion is the area of interest to be simulated.

The *Select Net Routes* command propagates the selection of nets based on the net names, thereby selecting anything that has the same net names, i.e. the entire trace. In this example, there are many overlapping traces running between pins. The objective is to use EM simulation on only those parts of the board, thereby saving considerable simulation time. This is accomplished by isolating the area of interest from the rest of the layout. This is done by opening a second PCB EM setup wizard and selecting the pins in the area of interest. The smart select button identifies and selects all the nets that are connecting the pins.

In this design, some of the pins have nets that connect to different ground or power planes at the port. If this is the case, the user has an alternative method of selecting nets that applies further automated intelligence. The *PCB EM setup* wizard works similarly to the *Select Net Routes* command in that it propagates the selection down nets omitting (not select) shapes that are connected to either power or ground nets. The EM setup wizard can also propagate net selection through open gaps in the net where (series) surface-mount components would be located. For complicated boards with many components, this capability makes net selection much faster than manually trying to select individual common nets that are interconnecting multiple components.

The software highlights the areas containing the nets selected for EM simulation. The EM setup wizard can be used to confirm visibility of layers and select the kind of cutout style desired, i.e. details of the PCB area surrounding the selected trace(s). The default is a bounding box, but in this case, to avoid selecting areas that are not of interest, which adds unnecessary simulation time, the user can specify the bounding polygon, which provides a four-sided figure cutting out the area not wanted in the simulation. This feature also allows the user to adjust the distance from the selected trace metals to the edges of the bounding box (Figure 4).

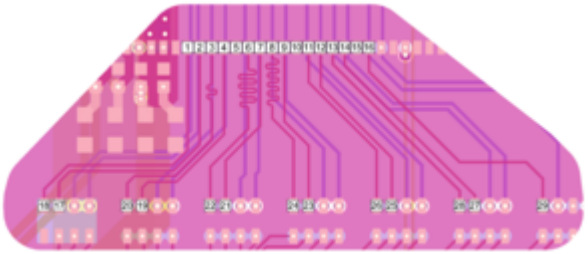

Figure 4: Bounding polygon.

Now that all the traces of interest are selected, the simulation space can be trimmed to a reasonable size using the *Create EM Clip Region* command, which provides different options for the size and shape of the simulation space. Once this is set, the EM structure can be created with the *Copy to EM Structure* command. The PCB simplification tools provide users with some simplification choices, and the wizard looks at the nets and geometries and offers suggestions based on the geometries within. Designers can edit the suggestions or accept them all. The idea behind this is to simplify the geometry without changing the basics, enabling a faster EM simulation without compromising accuracy.

Now that the EM structure exists, ports can be added, and the simulation can be done. The PCB EM setup wizard assists with this task as well. The pins of interest have already been selected, and rather than repeating, they can be restored in the EM structure through the wizard. Once the simulation is done, it is easy to bring the results into a schematic and wire up components that automatically show up on the subcircuit and schematic. To better guide the designer working with a section of board in the schematic editor, it is easy to create custom symbols based on the layout of the PCB EM structure so that is easy to visually know what port is where in the layout. With this particular design automation, it is possible to import a PCB into this platform, intelligently trim down the problem to the region of interest and get it ready for EM simulation and then hook up the surface mount components in a schematic and look at the performance. A simplified diagram of the available design flow for EM verification of PCB layouts from 3rd party CAD tools is shown in figure 5.

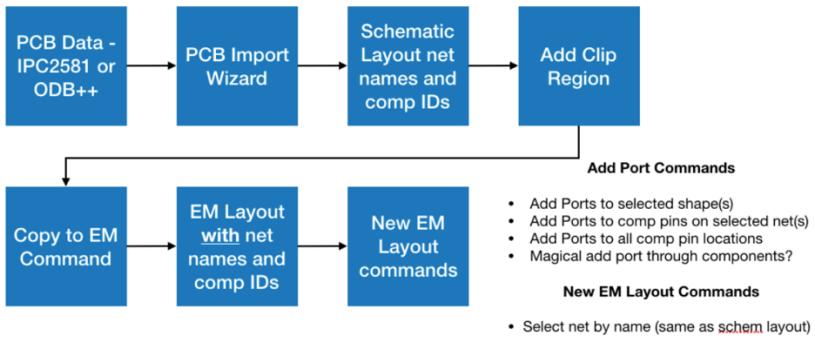

Figure 5: Design flows for EM verification of PCB layouts from 3rd party CAD tools

For this structure, the resulting mesh is around 20,000 unknowns (Figure 6). With the use of the wizard in V14, the mesh and resulting unknowns are reduced and simulation time are significantly shorter and results are obtained faster -- without losing accuracy.

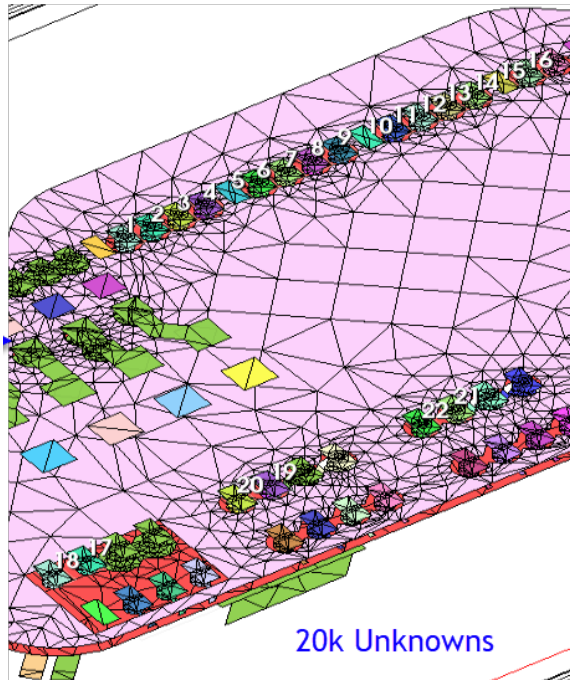

Figure 6:Shape simplification reduces the number of unknowns in the mesh, thereby reducing simulation time.

Note: The original geometry has rounded corners on the pads and the EM structure generated in the PCB EM structure wizard has rectangular pads (Figure 7), which provides a much simpler mesh.

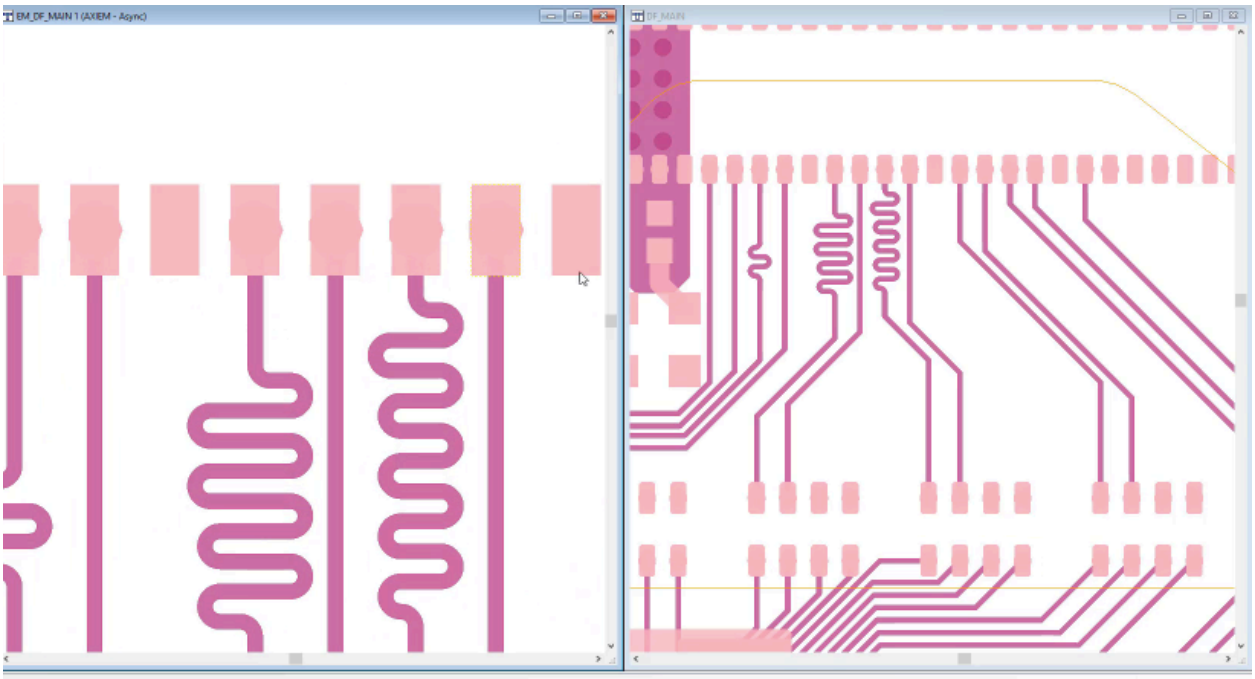

Figure 7: Rounded pads on the left and the EM generated structure on the right with simpler mesh.

When the simulation is complete and the EM structure is viewed within a circuit schematic, it is then ready to analyze further and connect components across the board. Component pin names are indicated in the schematic, so each pin is easily identified. In addition, in custom symbols that match

the layout of the structure can be created to ensure that components are connected correctly (Figure 8).

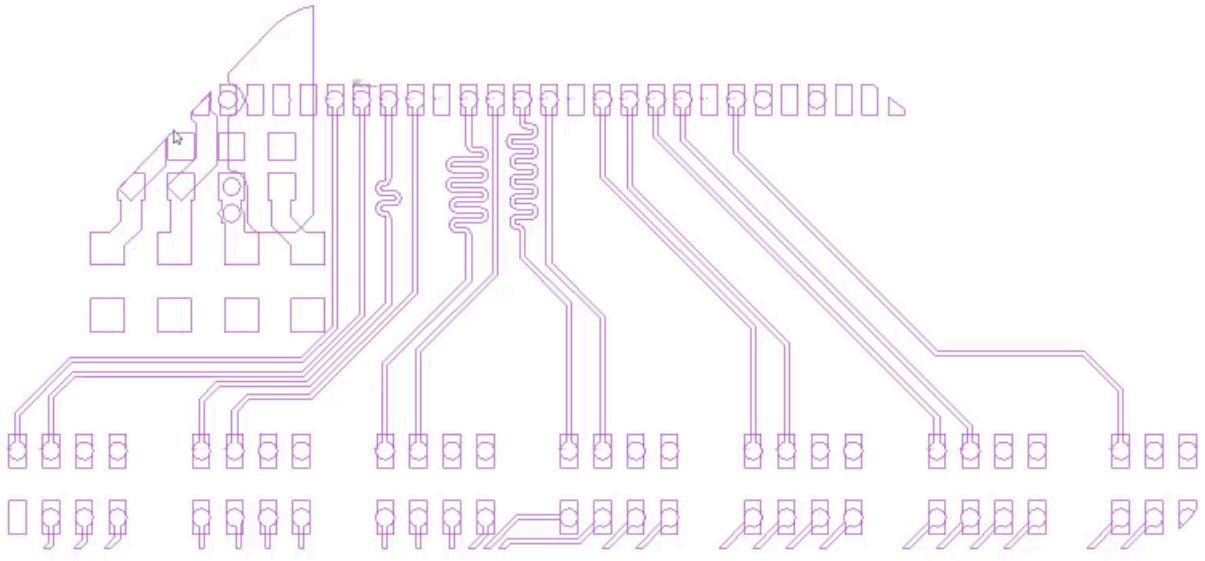

Figure 8:EM simulated schematic that enables easy analysis and adding of components across the board.

Conclusion

Today's complex PCBs require time-intensive investment in design and simulation tasks to ensure high-level performance in shrinking footprints. The example presented in this paper showcases the powerful capabilities in a new PCB import wizard, which supports interoperability and data exchange between commercial CAD layout tools and RF analysis software. This productivity-enhancing utility enables designers to go from selecting and importing a PCB file to a full EM simulation using a simple and automated process that significantly cuts simulation time without compromising accuracy.

Note: Thank you to Zuken for providing sample PCB files from which to develop this article.