Comparison of Embedded Coplanar Waveguide and Stipline for Multi-Layer Boards

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***Abstract*— In this paper we present comparison of conductor-backed Coplanar Waveguide (CPW) with a cover shield and Stripline for multi-layer boards using a full 3D EM CAD software. It is important in High-Speed Digital Applications to decrease the form factor and increase the signal density by reducing isolating metal layers while preserving comparable crosstalk, loss and dispersion at the frequency of interest. Conductor, and dielectric losses of conductor-backed CPW with a cover shield and Stripline are compared up to 25 GHz, for 5Gbps digital applications. Typical dimensions are used for Intel's stripline SDRAM multilayer interconnect boards, and equivalent dimensions are calculated for CPW. Isolation and coupling is presented for tightly and loosely coupled edge and broadside coupled CPW and Stripline. We show that CPW with smaller form-factor outperforms Stripline in isolation and coupling.**

***Index Terms*— Embedded coplanar waveguide, conductor-backed Coplanar Waveguide with a cover shield, stripline, loss characterization, high-speed digital interconnects .**

I. Introduction

Various CPW configurations have been investigated in the past. Coplanar Waveguide (CPW) has been proposed by Wen in 1969 [1], [2]. Gupta in [3] lists various types of CPW: CPW with finite dielectric thickness, CPW with finite width ground planes, CPW with a cover shield, conductor-backed CPW with a cover shield, conductor-backed CPW, multilayered CPW, asymmetric CPW and asymmetric CPW with finite dielectric thickness coplanar waveguide (CBCPW). Wolff examines CPW in [4]. Recently there has been a renewed interest in broadband characterization of transmission lines on both PCB and integrated circuits at millimeter-wave frequencies for 5G applications [5], for high-speed digital applications [6]–[9], and optical frequencies [10]. Specific transmission lines features have been investigated, from copper roughness modeling [11], [12], placement of vias in CPW [12]–[18], and comparison of CPW performance has been compared to microstrip in [19].

II. Background

Stripline is the preferred transmission line in high-speed digital circuits. The benefit of stripline is that it supports TEM mode and therefore has no dispersion and no lower cutoff frequency. Striplines have low radiation, and in addition, far-end cross talk is zero as symmetry produces relative capacitive and inductive coupling to be approximately equal [20]. Width of the signal strip to height of the substrate must be fixed for a specific transmission line impedance, which limits the design flexibility of striplines.

An advantage of a CPW is in design flexibility. CPWs can be made on thick substrates. Design criteria in a CPW to achieve specific characteristic impedance is the ratio of signal strip width and gap. The ratio of the width of the signal strip and the the height of the substrate does not need to be fixed to produce a 50-Ω line. Characteristic impedance is independent of the thickness of the substrate as long as the gap size is smaller than the thickness of the substrate [1]. To avoid parasitic microstrip mode, the width of the strip and the gap has to be smaller than the distance to lower or upper ground. To avoid stripline mode, the gap has to be smaller than the signal line width.

Via-holes can be introduced in both striplines and CPW to prevent parallel-plate waveguide modes, but this increases fabrication complexity and cost. Further, airbridges can be introduced to remove the slotline (aka odd CPW) mode. CPW can be made smaller in size than compared to microstrip [21] and therefore striplines as well. In order to minimize parallel-plate modes, the size of the ground planes on the same layer as the signal line can be made smaller, making the structure finite ground coplanar waveguide (FGC).

In practice the bottom of a substrate is usually metalized for structural support and to improve isolation between layers in a multi-layered board. The top metal cover is present as well in a packaged circuit, making most cpw structures conductor-backed CPW with a cover shield. This work investigates embedded conductor-backed CPW with a cover shield and finite-size grounds FGC applicable to multi-layered boards, such as Intel Architecture Platforms [22]. In this paper, comparison of stripline and conductor backed FGC with a cover shield losses, modal analysis and coupling are investigated.

III. Simulation setup

Single line simulations are first performed for FGC and Stripline using Modal analysis in HFSS. For a single line, four modes were set for CPW and for Stripline for a 4mil length of the lines. The results were then de-embedded to 1 inch using HFSS deembed function.

Typical values for an FR-4 board were used in the simulations: $\epsilon_r = 4.4$, $\tan\delta = 0.02$ $\sigma = 5.7\,10^8$. Groiss model [23] option in HFSS was used with roughness set to RMS=6μm. The same roughness was set to all metal surfaces. It is likely that the CPW performance in this case is underestimated because the roughness on the side of the signal strip, where the fields are concentrated, is lower [19]. All metals have finite thickness of 1/2oz, or $t = 0.7$ mils. Dielectric loss was modeled using the simple loss model.

Stripline dimensions are designed using Linecalc in Keysight's Advanced Design System [24]. Dimensions of the substrate were initially used from a typical Intel-based multilayer board. In a multi-layer stackup, the layers are core, prepreg and copper foil. In this simulation, the dielectric material is typical FR4 homogeneous substrate, and that core and prepreq have the same dielectric properties. Stripline signal width was set to w=7 mils, and the distance to either ground was kept at 9 mils to maintain 50-Ω impedance.

Conductor backed CPW with shield impedance was calculated in Matlab [25] using equations in [26] and ADS. Width of signal line was set to 7mils and the distance to ground was increased until the parasitic microstrip mode was minimized at the height of the substrate of h=12mils. The distance from the CPW to the ground plane was then set to 16mils. The gap is $g = 4$ mils for a 50-Ohm line. Transmission line impedance simulation in HFSS was then inspected by looking at the generalized S-parameters to see that the line impedance was implemented successfully.

IV. Characterization of Losses

A. Visualization of Modes in CPW and Stripline

Simulated CPW and Stripline modes are shown in Figures 1. Attenuation α and phase β constants have been simulated for all modes in HFSS. Dominant modes in CPW and Stripline have large real phase constants 400radm and attenuation constants of ($\sim$10 Np/m at 10 GHz). Other non-dominant modes in the simulation are evanescent.

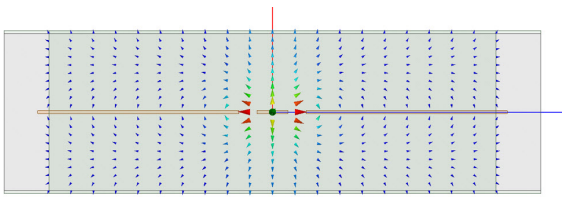

Fig. 1. Vector representation of even (cpw) mode.

To estimate the effect of each type of loss on embedded CPW, conductivity of copper, dielectric loss and roughness was sequentially added as shown in Figure 3. The worst-case scenario was used here, where all signal and ground

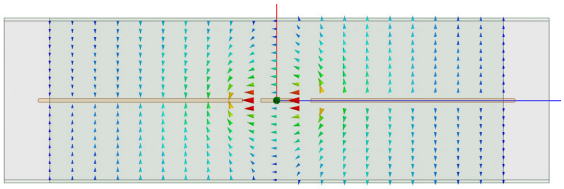

Fig. 2. Vector representation of parasitic slotline (odd) mode.

surfaces are assumed to have roughness of 6μm. Graphs show that the roughness becomes important when the skin-depth is of the order of roughness (0.1 GHz). To make a fair comparison of losses in the bandwidth of interest, insertion loss and return loss are subtracted from the total power, as shown in Equation 1. Dielectric loss $\tan\delta$ is the largest contributor to the overall loss.

$$P_{Loss} = 1 - |S_{21}|^2 - |S_{11}|^2 \tag{1}$$

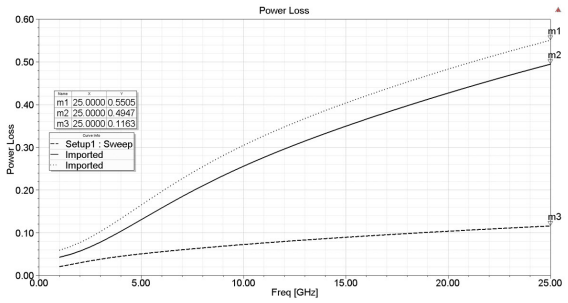

Fig. 3. Contribution of losses to CPW loss. (a) ohmic losses (b) ohmic and dielectric losses (c) omic, dielectric and roughness.

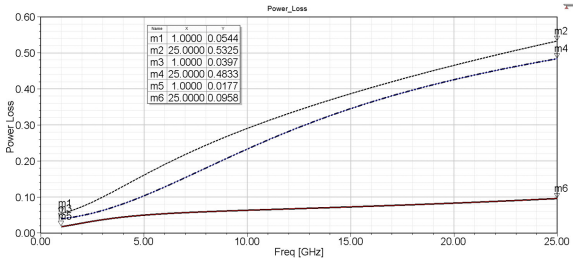

Fig. 4. Contribution of losses to CPW loss. (a) ohmic losses (b) ohmic and dielectric losses (c) omic, dielectric and roughness.

B. Edge coupled CPW and Stripline comparison

In this section two edge-coupled CPWs and striplines were simulated as shown in Figure 5. The horizontal separation gap between two striplines was varied from 5mils to 15mils in 5 mil increments. In CPW, the width of the center ground, between two CPWs was varied for the same distance. 4-mils thick line segments were simulated using Terminal simulation, with one 996mils

de-embedeed port. Waveports are assigned to the front and back side of the circuit, as shown in Figure 5. The size of waveport was selected so that the higher-order modes, including waveguide modes from the waveport do not propagate. Top, bottom and side grounds were selected as reference conductors, and three terminals were placed at left and right center conductor and the middle ground. Side grounds are designated as grounds through the edges of waveport. Middle ground terminals were renormalized to $10^{-6}\Omega$ to designate another ground conductor, and the center conductors were re-normalized to 50Ω. Both CPW and uncoupled striplines are 50Ω with return loss above 30dB.

In all configurations cpw significantly outperforms stripline as shown in Figures 6-7. Dotted lines in Figures 6-7 show isolation and coupling for edge-coupled conductors separated by 5 mils, solid lines show separation of 10 mils and dashed lines show separation of 15 mils. The top dotted line represents the Stripline, and bottom lines CPW. The density of coplanar CPW lines can be significantly increased to produce the same coupling and isolation as in Striplines. For example, isolation of two edge-coupled CPWs separated by 5mils is the same as two striplines separated by 15mils. The coupling in CPW can be further reduced by making the gap width smaller, therefore confining the fields tighter to the gap [27].

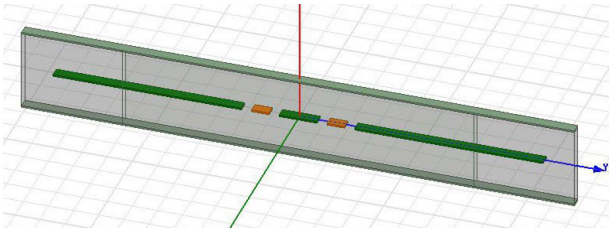

Fig. 5. Edge coupled CPW lines.

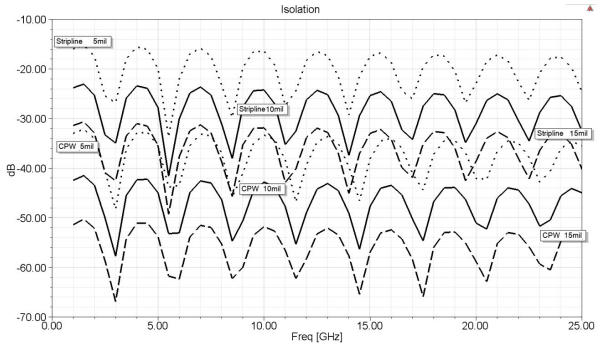

Fig. 6. Isolation comparison for two edge-coupled CPW and striplines.

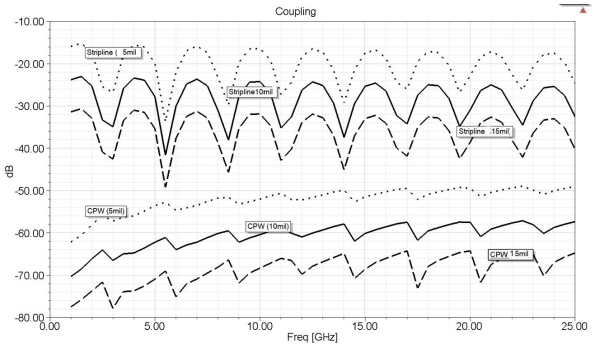

Fig. 7. Coupling for two edge-coupled striplines.

C. Broadside coupled CPW and Stripline comparison

Two broadside-coupled CPWs are shown in Figure 8, and the stripline was simulated in a similar configuration. Circuits were simulated using Terminal simulation in HFSS. The distance between the broadside coupled lines was 4, 6 and 8mils. The labels on Figures 9-10 show the distance between the axis of symmetry, x-y plane, and each line. The simulation was performed in a similar way with the previous one, except this time, only the input port was de-embedded and renormalized to 50Ω. The output waveport was not renormalized, which presents a perfect matched condition, and the S-parameters are normalized to a frequency-dependent impedance to present a clear difference between the isolation and coupling. The results would not be consistent with the measurements of a constant 50Ω instrument, as in the previous simulation, but it is easier to see the difference between the coupling and isolation in two cases. Coupling and isolation in CPW lines is lower than the Striplines. This is beneficial if the lines do not carry differential signals.

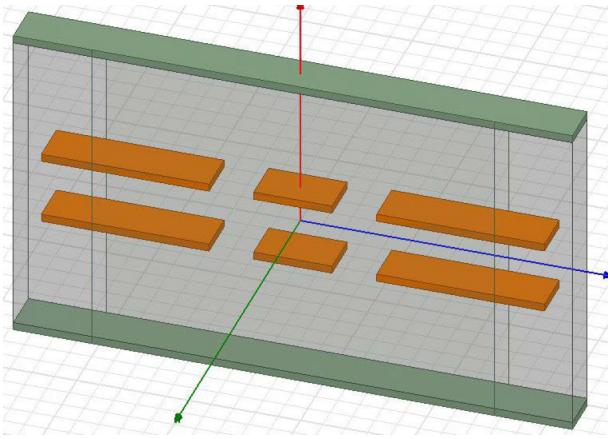

Fig. 8. Broadside coupled CPW lines.

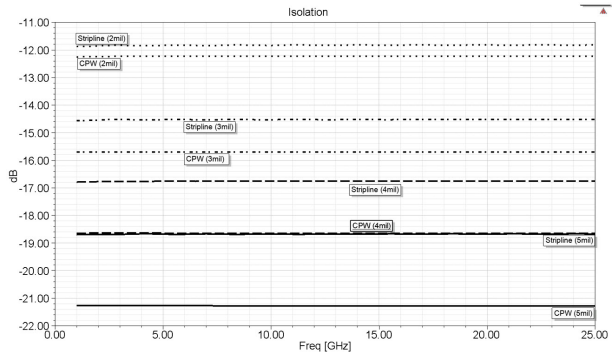

Fig. 9. Isolation for two broadside-coupled CPW lines.

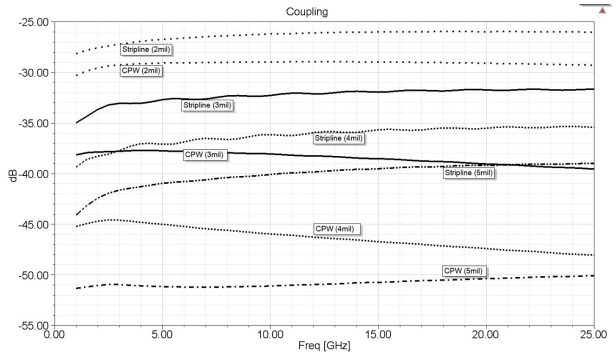

Fig. 10. Coupling for two broadside-coupled striplines.

V. Conclusion

It is of interest in high-speed digital circuits to minimize the number of signal layers, limit layer transitions and to remove isolating ground layers in stripline to decrease layer count and therefore the price and weight of the multilayer board. We show that the embedded CPW with a cover shield offers greater design flexibility and higher packaging density than stirpline for comparable coupling and isolation performance.

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