Electronic Design Innovation
Conference & Exhibition

Mark Gurries FAE

EPC EFFICIENT POWER CONVERSION

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Agenda

1. **Low Voltage eGaN® Section**
   - Intro to EPC & eGaN®
   - Why eGaN® FETs?
   - Gate Drive Voltage

2. **Rethink Server Power Architecture with eGaN® Technology**
   - Telecom/Datacenter Server Rack Design Evolution
   - 48V – POL DC-DC Architectures
   - 48V – 1V TI Demonstration System Specifications

3. **Appendix**
   - EPC 48V to POL Application Demoboards
   - Growing ECO System for High Frequency eGaN®
     - Gate drivers
     - Magnetics
     - Controllers
   - Reliability

EPC's Key Team members are Innovators

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Alexander Lidow (Founder):
- Ph.D. Stanford University, 1977
- Co-Inventor of HEXFET Power MOSFET Transistor 1978
- CEO of International Rectifier 1995-2007
- Wrote textbook on GaN

Jianjun "Joe" Cao (Founder):
- Ph.D. University of California at Berkeley, 1996
- Power MOSFET and GaN innovator at International Rectifier

Robert A. Beach (Founder):
- Ph.D. Caltech, 2001
- Co-Founded GaNRose to produce gallium nitride transistors
- Sold GaNRose to International Rectifier in 2003

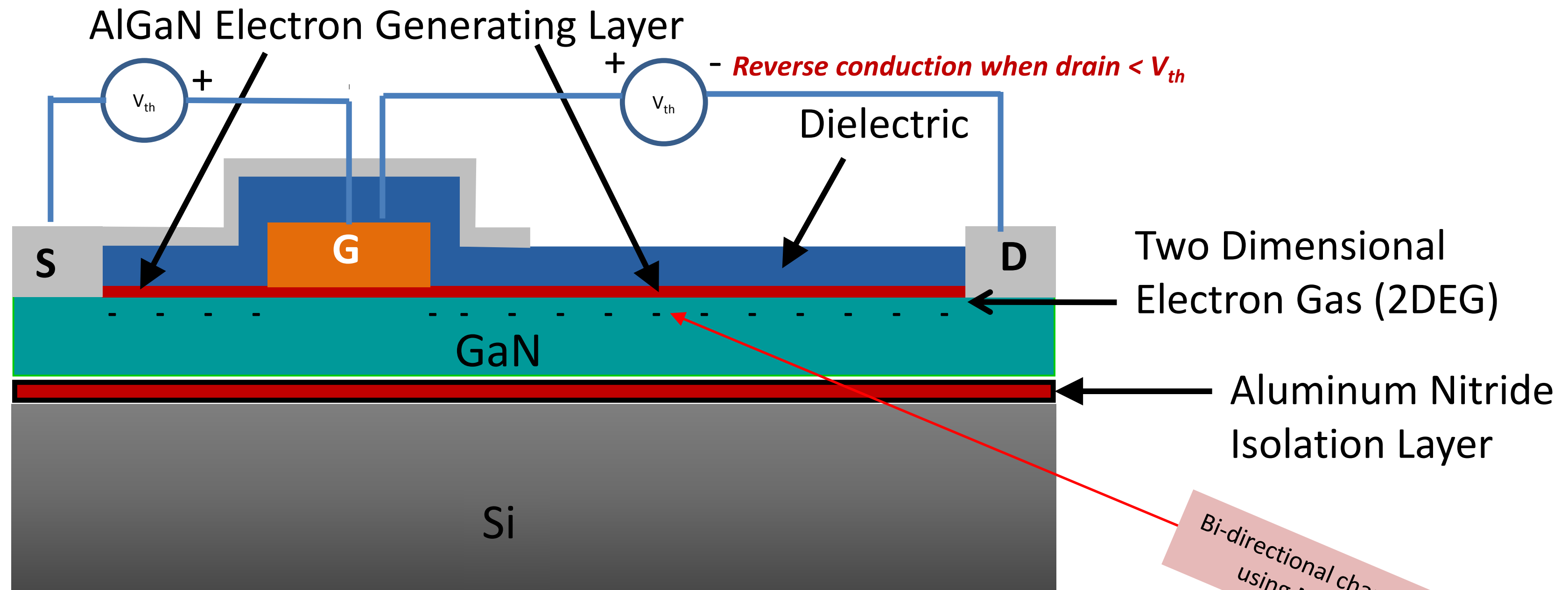
Thomas Herman:
- MSEE Stanford University
- Co-Inventor of HEXFET Power MOSFET Transistor 1978
- Director of IC development of International Rectifier 1977

The founders are obsoleting the Silicon MOSFET they helped create.

eGaN® Is …

- Efficient
  - Most applications show that GaN is more efficient at higher frequency.
- Mature
  - GaN was first commercialized in 2004 for RF transistors.
  - Enhancement mode eGaN® FETs were commercialized in 2009.
- Easy to use
  - eGaN® FETs are enhancement mode just like N-channel MOSFETs, except a lot faster.
- Cost effective
  - eGaN® FETs are built on silicon wafers using standard CMOS foundries.

eGaN® FET Structure



- **Works like a MOSFET**
  - Positive Vgs Voltage turns on bidirectional channel
  - Gate shorted to Source blocks Drain to Source conduction
  - Reverse polarity diode conduction function
- But **better** because:
  - **Lower Capacitance & Inductance** for a given $R_{DS(on)}$ (Higher switching speed)
  - **Zero Q_{RR} Reverse Conduction** (No MOSFET PN diode recovery issues)

Product Selection Overview

- 15 V to 350 V single FETs
- 30 V to 100 V dual (half bridge) asymmetric and symmetric families
- 0.9 mm x 0.9 mm to 6.1 mm x 2.3 mm Wafer Level Package (BGA/LGA)
- ½ bridge development boards and selection of demo circuits available
- MSL Level 1 and 100% ROHS 6 of 6 compliant
- AEC-Q101 Parts are available.
- Price points from $0.25 to $5.00

Why eGaN® FETs? Typical Customer "WISH LIST"

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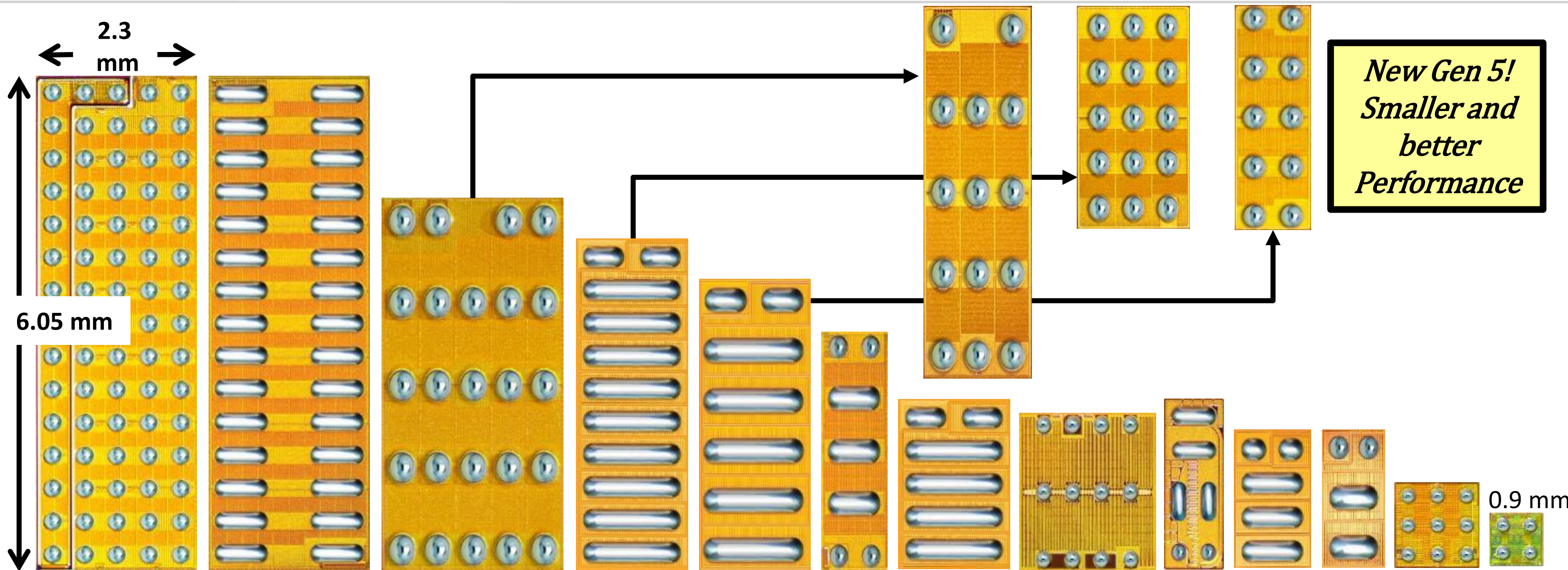
- Smaller Packages
- Simpler Part Construction
- Lower On Resistance
- Faster Switching
- Lower Thermal Impedance

Why eGaN® FETs?
Smaller BGA/LGA CSP FET Packages



- Absolute minimum lead resistance and inductance
- Minimum footprint on PCB
- Use PCB board as default heatsink
- RoHS 6 of 6
- MSL level 1 sealed package
- AEC-Q101 versions are available.

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Why eGaN® FETs?

New Generation 5

~Same Rdson, ≥40% Smaller, ≥40% C_{oss} Reduction

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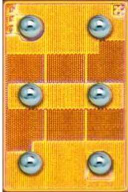
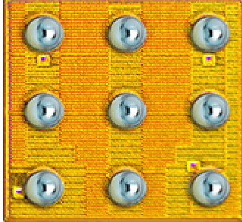
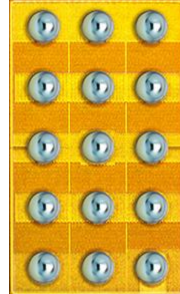
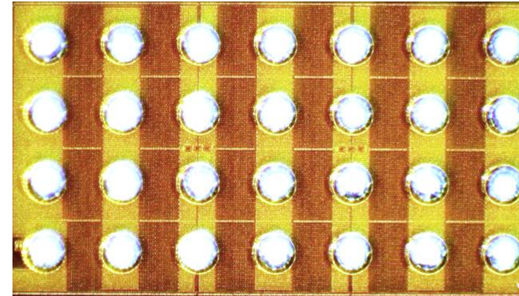
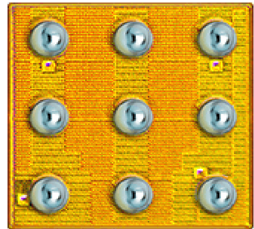
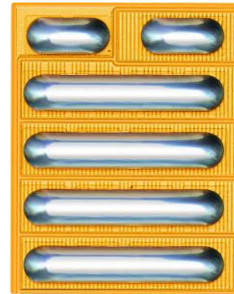
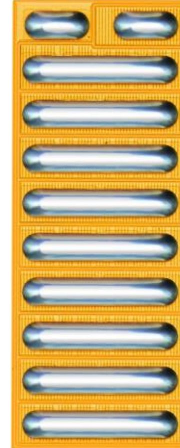
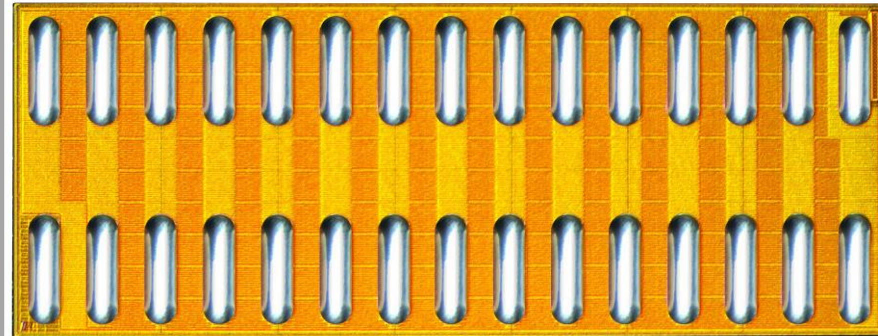
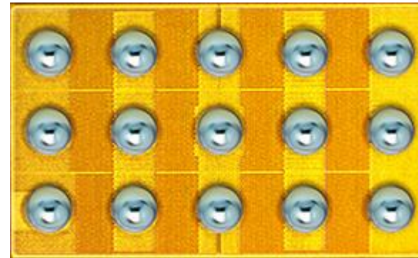
EPC2051	EPC2052	EPC2045	EPC2053	
				**New Gen 5**
21 mOhm 1.11 mm² 40% Smaller	10 mOhm 1.82 mm² 46% Smaller	5.6 mOhm 3.75 mm² 44% Smaller	3.2 mOhm 6.83 mm² 51% Smaller	
				Gen 4
EPC2039 20 mOhm 1.82 mm² (80V Part)	EPC2016C 12 mOhm 3.36 mm²	EPC2001C 5.6 mOhm, 6.70 mm²	EPC2022 2.4 mOhm 14.03 mm²	Parts not shown to any scale.

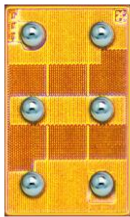
Why eGaN® FETs?

Some have BGA Compatible Footprints

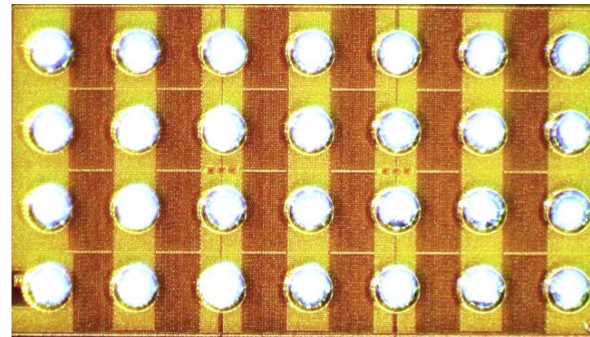


EPC2045

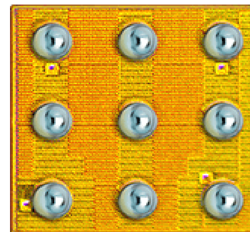
EPC2051



Unique Footprint



EPC2053



EPC2052

Why eGaN® FETs?

Monolithic Integrated FET solutions

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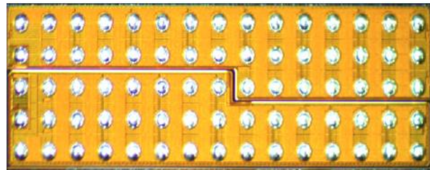
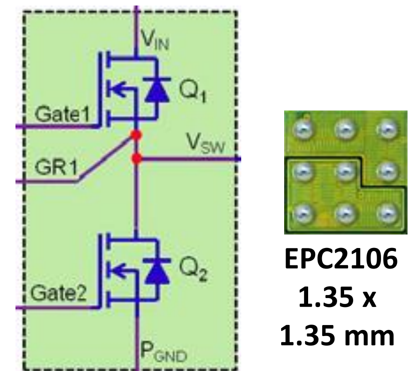
Symmetric Half Bridge (low R_{dson})



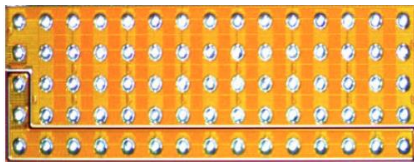
6.1 x 2.3 mm



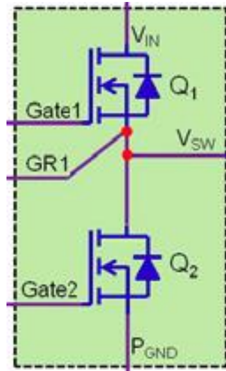
EPC2106 1.35 x 1.35 mm

Part #	Config	Vds	Rdson max
EPC2102	Dual	60	4.4
EPC2103	Dual	80	5.5
EPC2104	Dual	100	6.3
EPC2106	Dual	100	70

Asymmetric Half Bridge (low R_{dson})

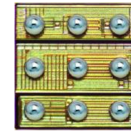


6.1 x 2.3 mm

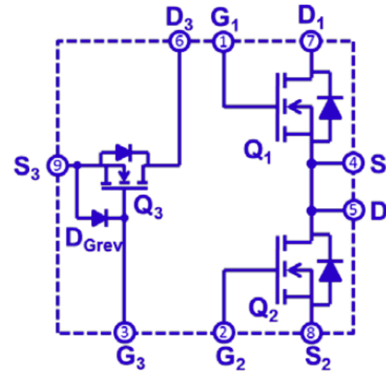


Part #	Config	Vds	Rdson max
EPC2100	Dual Asymmetric	30	8 2
EPC2101	Dual Asymmetric	60	11.5 2.7
EPC2105	Dual Asymmetric	80	14.5 3.5

Dual with Bootstrap

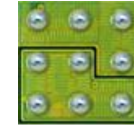


1.35 x 1.35 mm

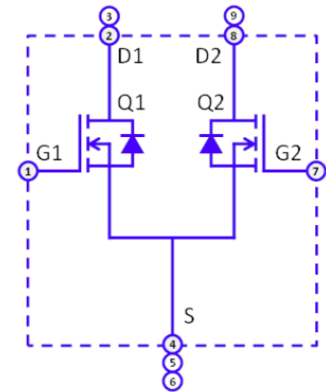


Part #	Config	Vds	Rdson max
EPC2108	Dual with Bootstrap	60	190
EPC2107	Dual with Bootstrap	100	360

Dual Common Source



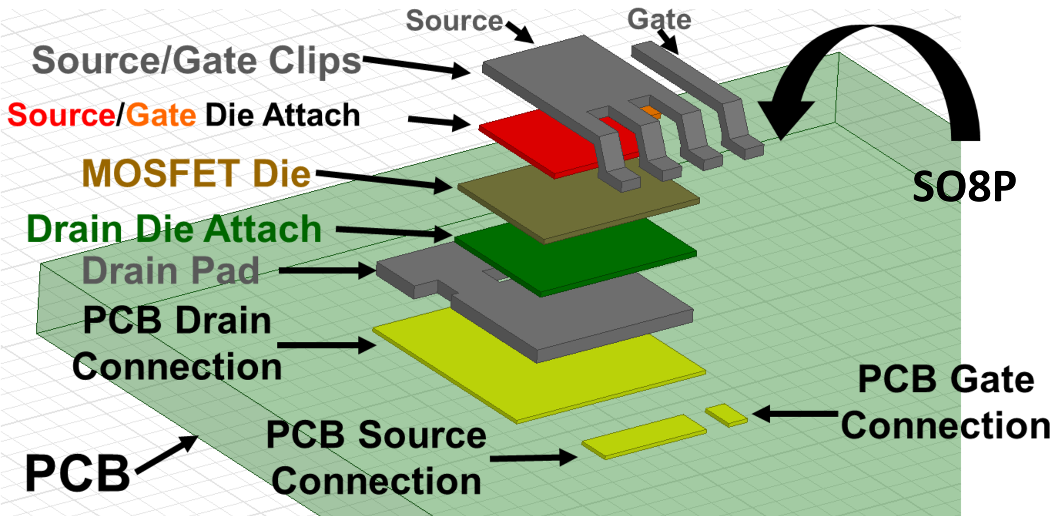
1.35 x 1.35 mm



Part #	Config	Vds	Rdson max
EPC2110	Dual, Common Source	120	60

Why eGaN® FETs?

Simpler more reliable construction of eGaN FETs

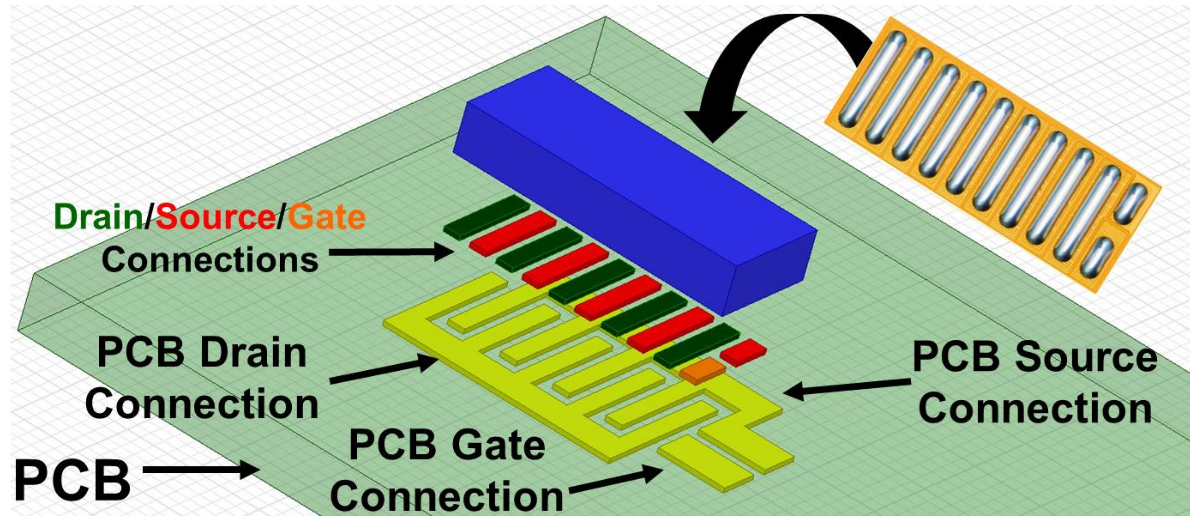


Traditional Silicon FETs

- More steps,
- Package reliability high.

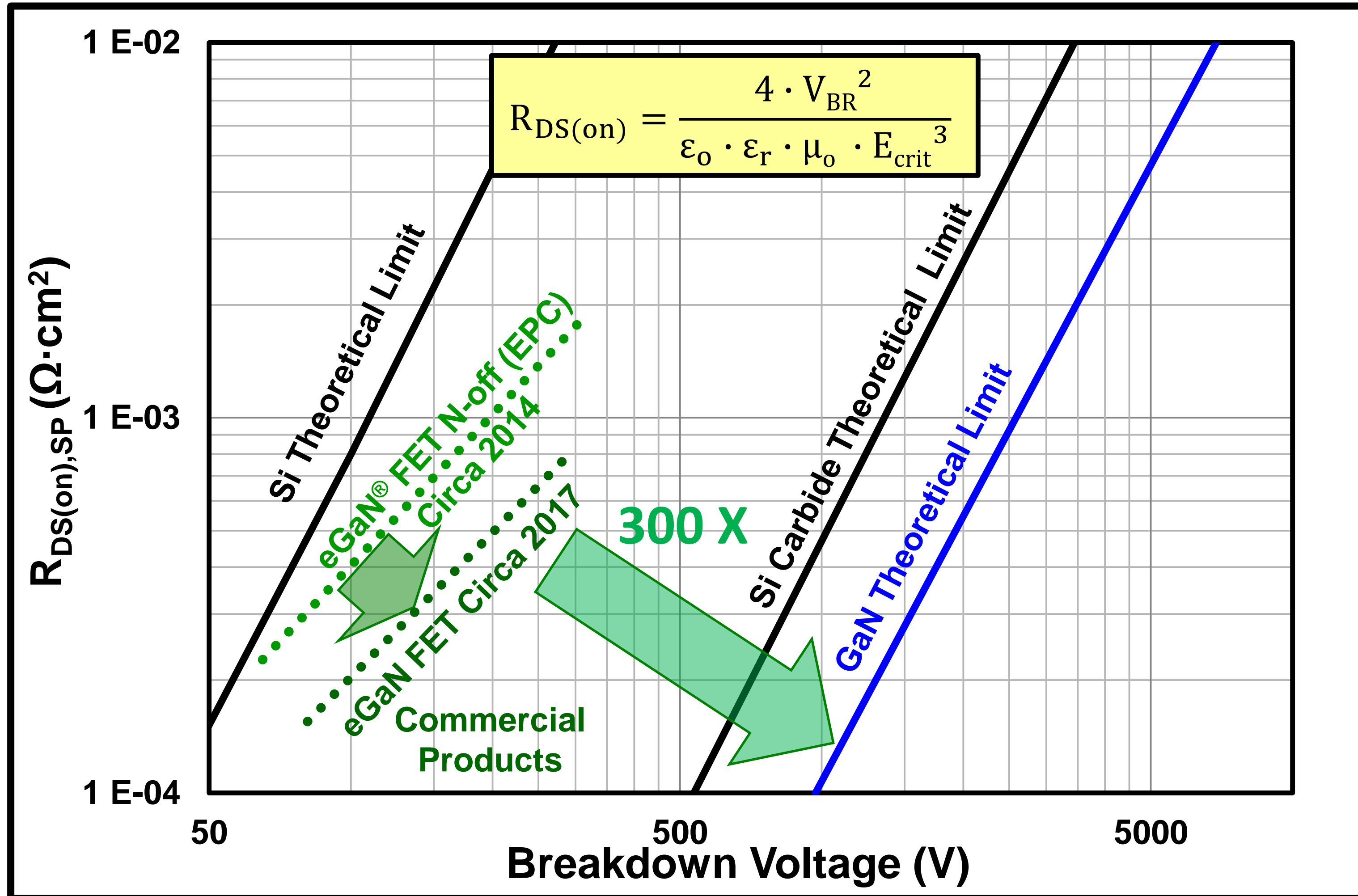
eGaN FET construction

- Less number of steps
- Less package inductance
- Higher reliability



Why eGaN® FETs?

Highest Semiconductor Performance Possible



Theoretical Channel Resistance

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Why eGaN® FETs?

Higher Switching Speeds

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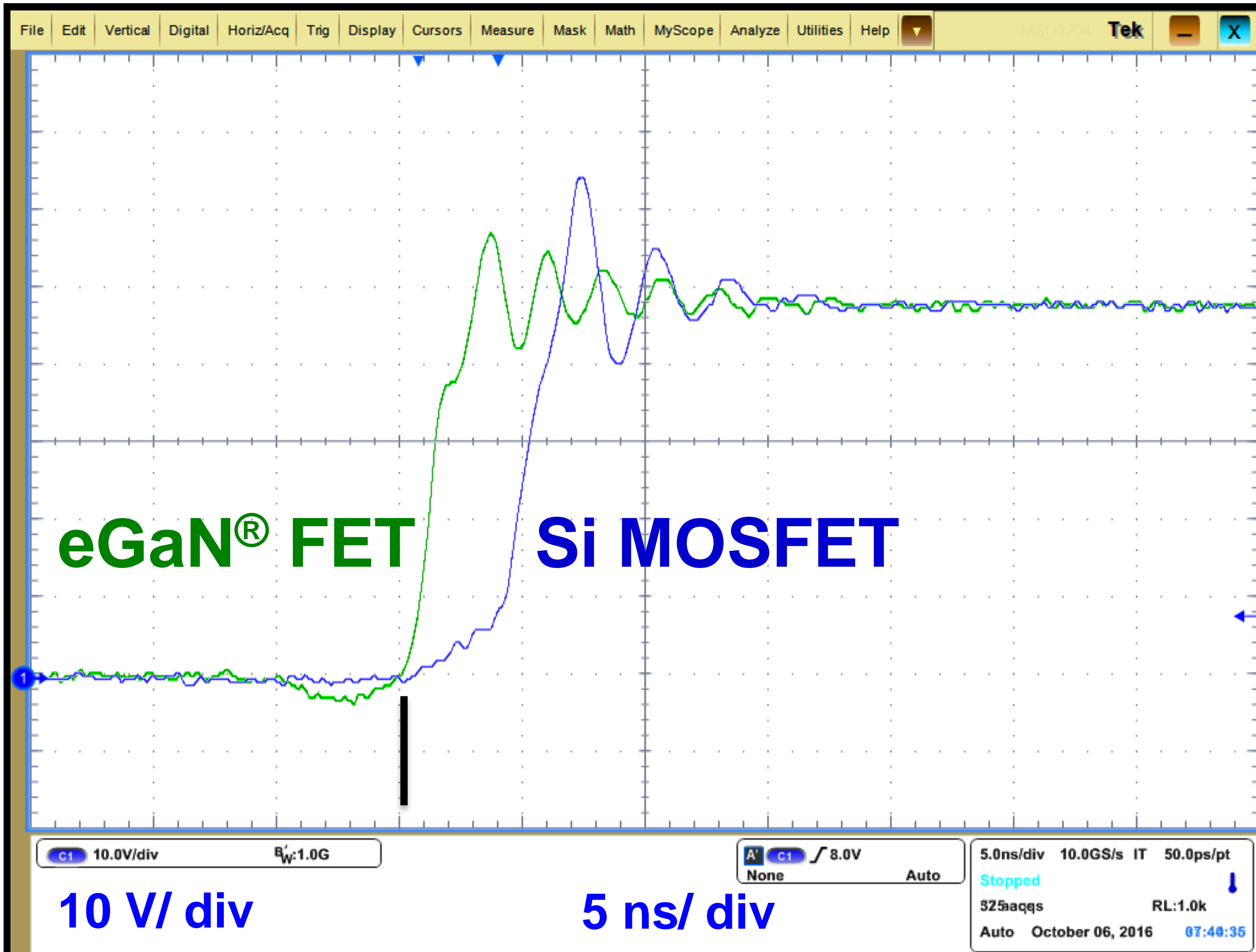
2017 100V FET Comparisons: EPC2045 50V General Switching Waveforms



EPC2045 eGan FET has a **2nS slew rate.**

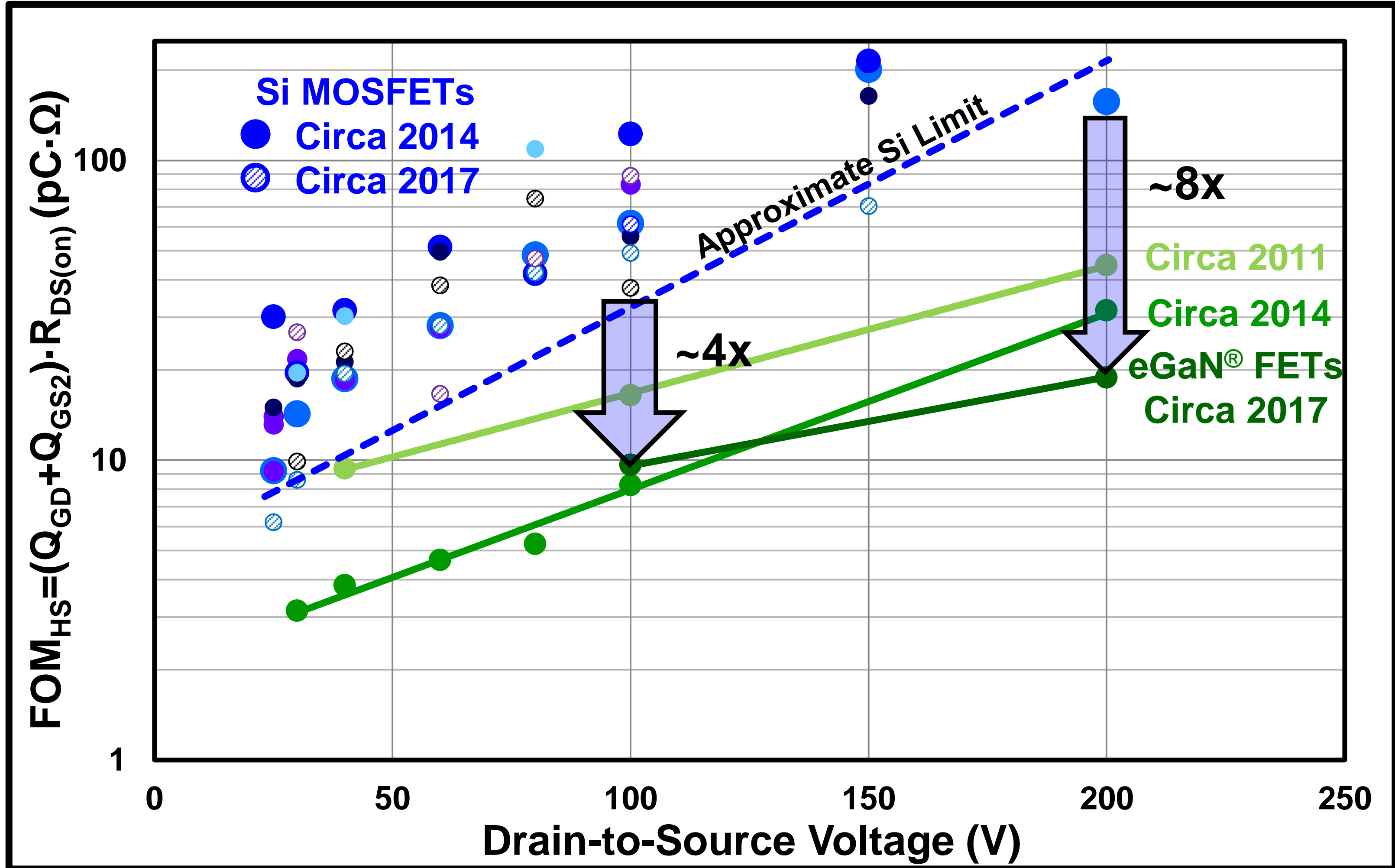
Best in class MOSFET has 4.5ns delay time with a 2nS Slew rate. **6.5nS total.**

3x speed advantage

EPC2045's small chipscale package reduces overshoot voltage.

Why eGaN® FETs?

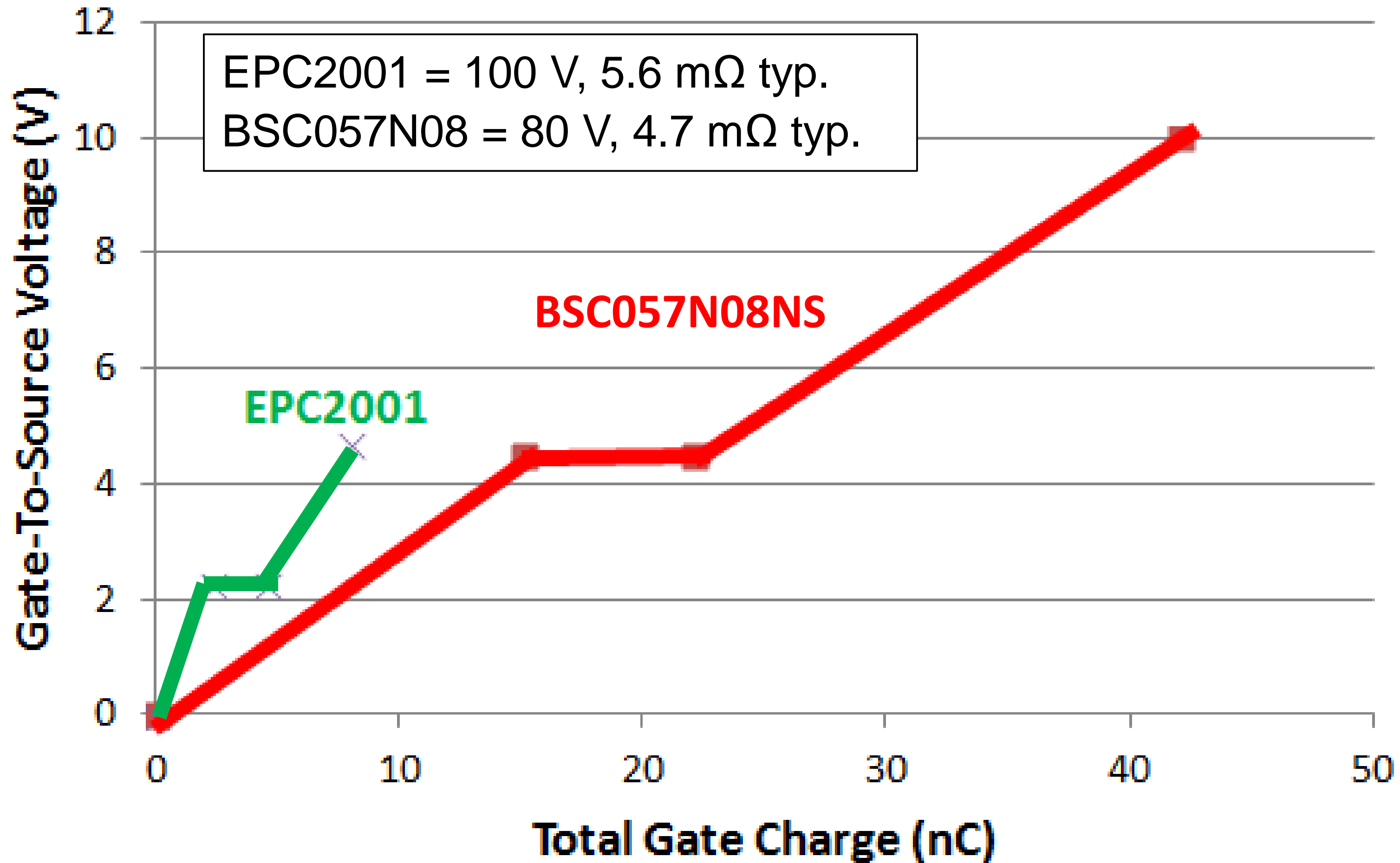
Hard Switching: Lower Qgd & Qgs2 = Lower Switching Losses.



$V_{DS}=0.5 \cdot V_{DSS}$, $I_{DS}=20$ A

Why eGaN® FETs?

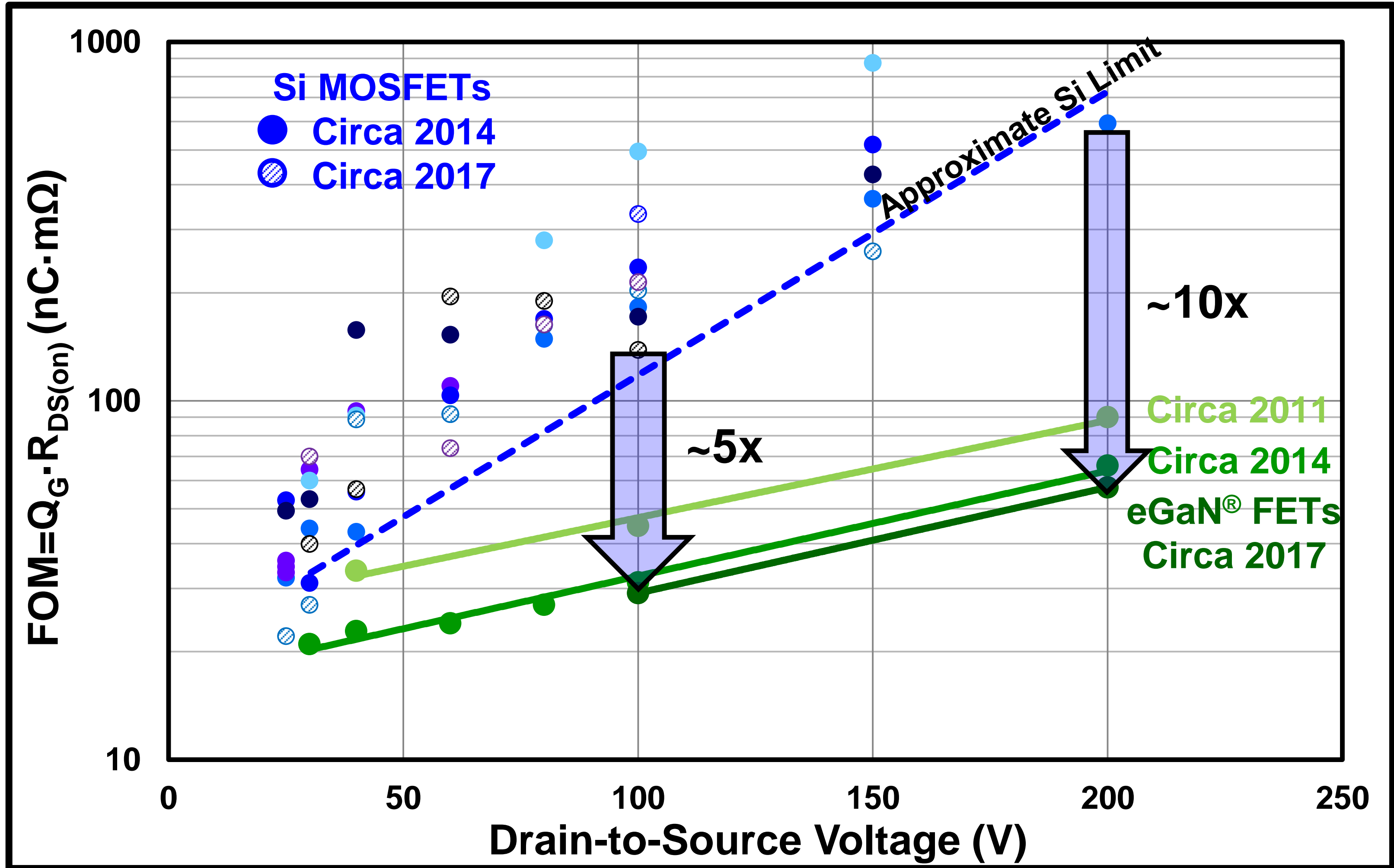
Lower Qg = Faster Switching & Lower Drive Losses



Lower Qg = Less time to reach $V_{gs\text{-}th}$ and finish = Faster Switching.
Lower Qg = Reduced gate drive loss as frequency goes up. P = Vgs * Qg * F

Why eGaN® FETs?

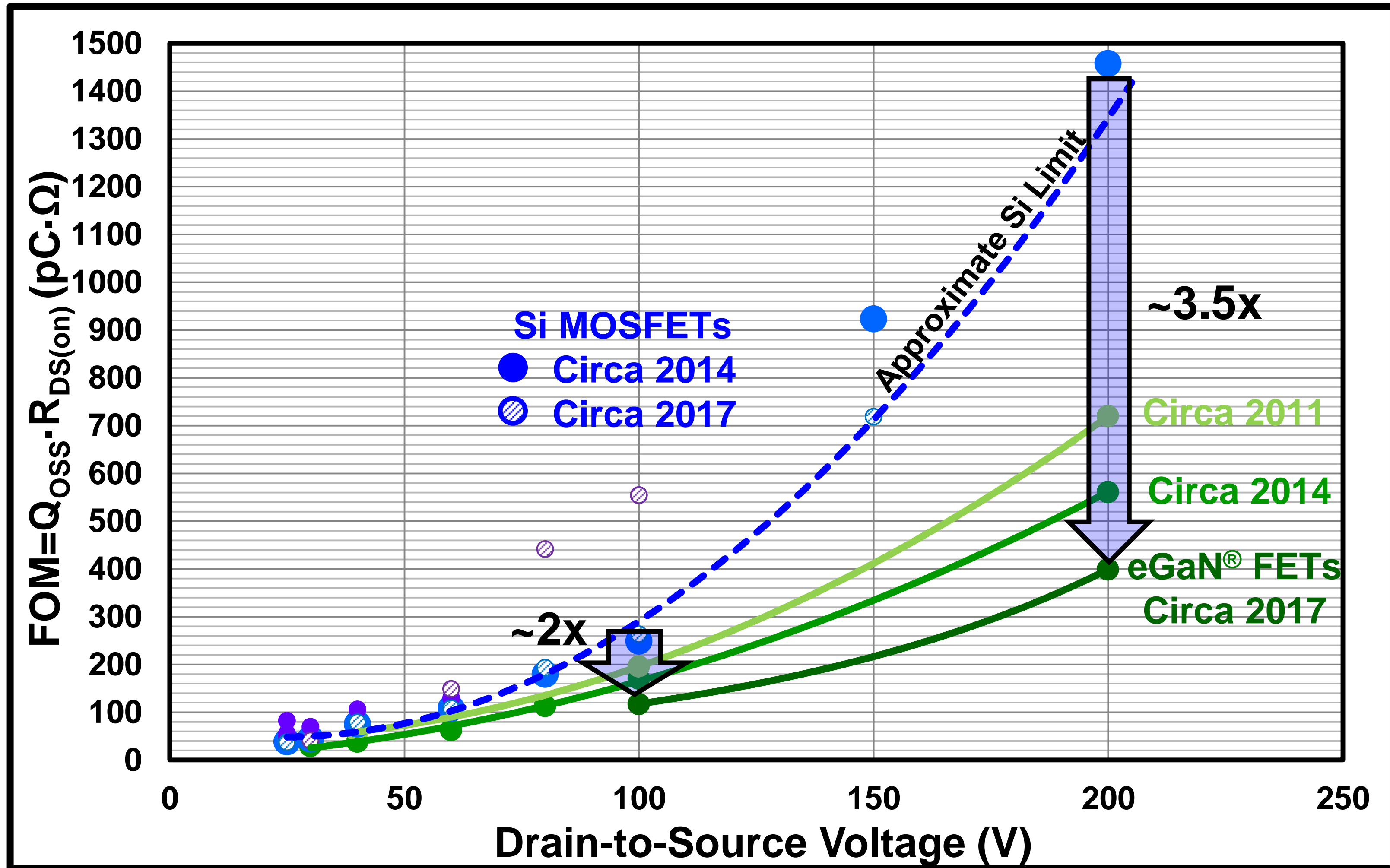
Lower Qg per Ω = Better FOM



$V_{DS}=0.5 \cdot V_{DSS}$, $I_{DS}=20$ A

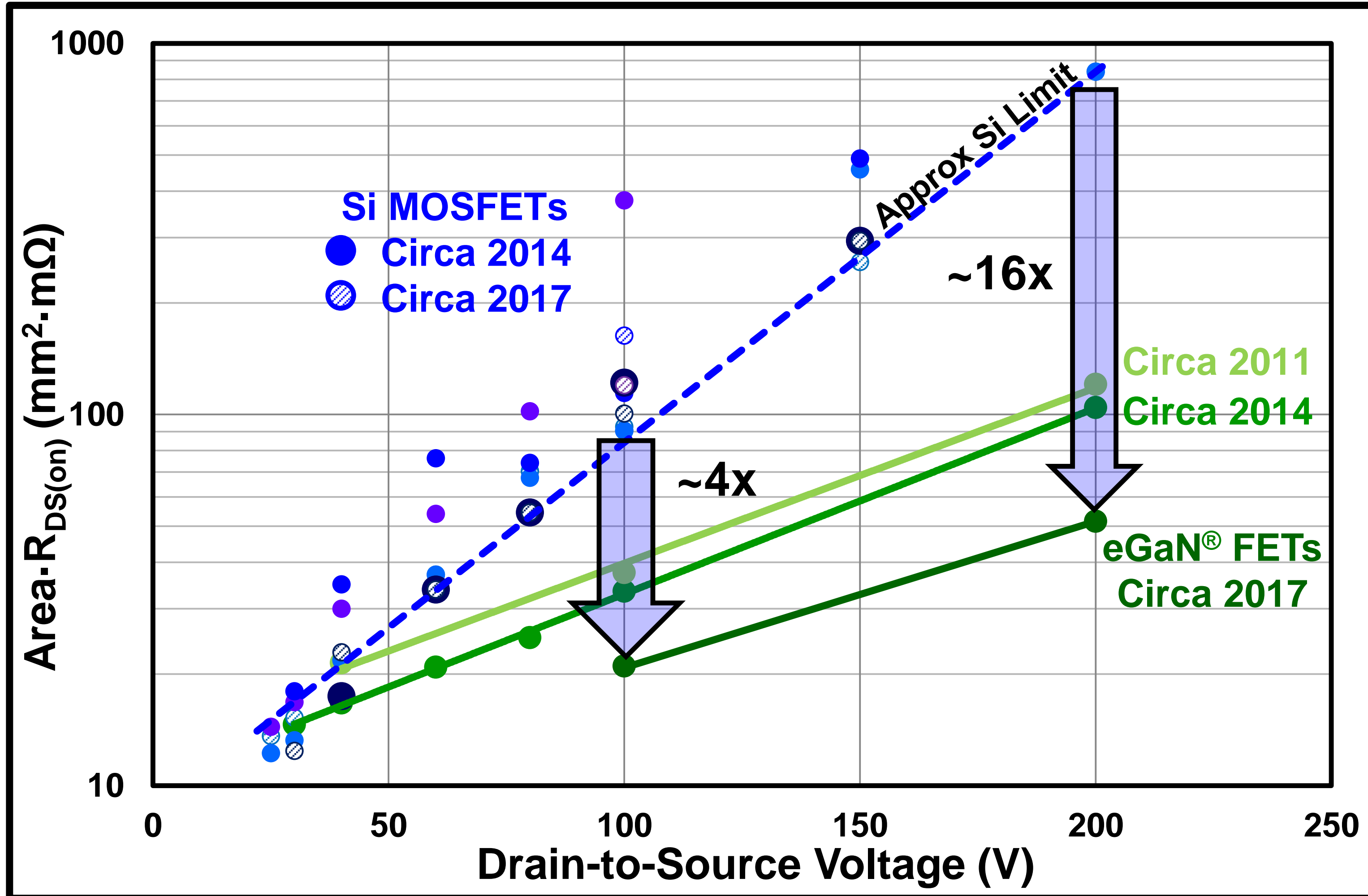
Why eGaN® FETs?

Soft Switching: Lower Qoss Output Charge



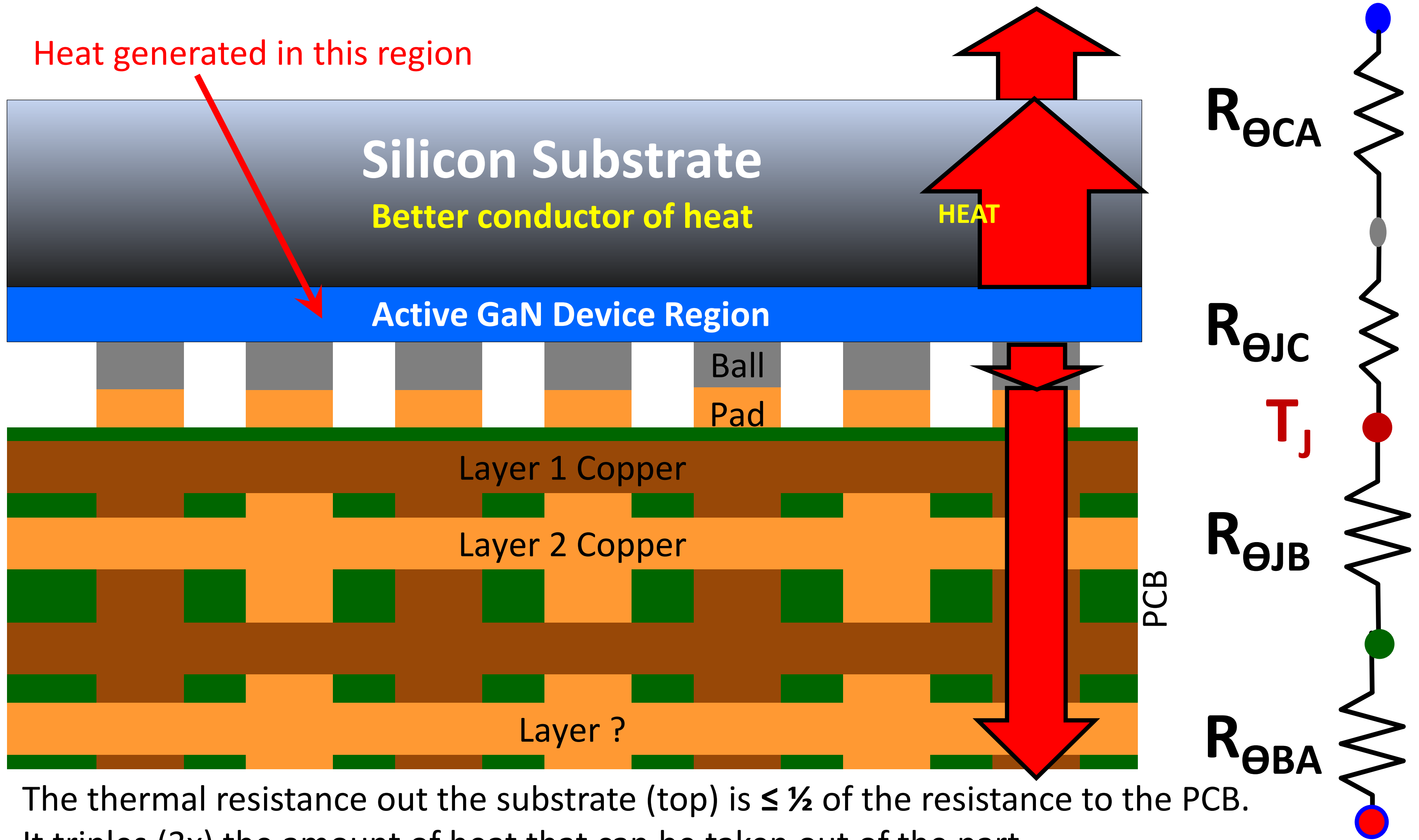
$V_{DS}=0.5 \cdot V_{DSS}$

Why eGaN® FETs?
Smaller Size



Why eGaN® FETs?

Thermals: Heat Has Two Ways Out!



The thermal resistance out the substrate (top) is ≤ ½ of the resistance to the PCB.
It triples (3x) the amount of heat that can be taken out of the part.

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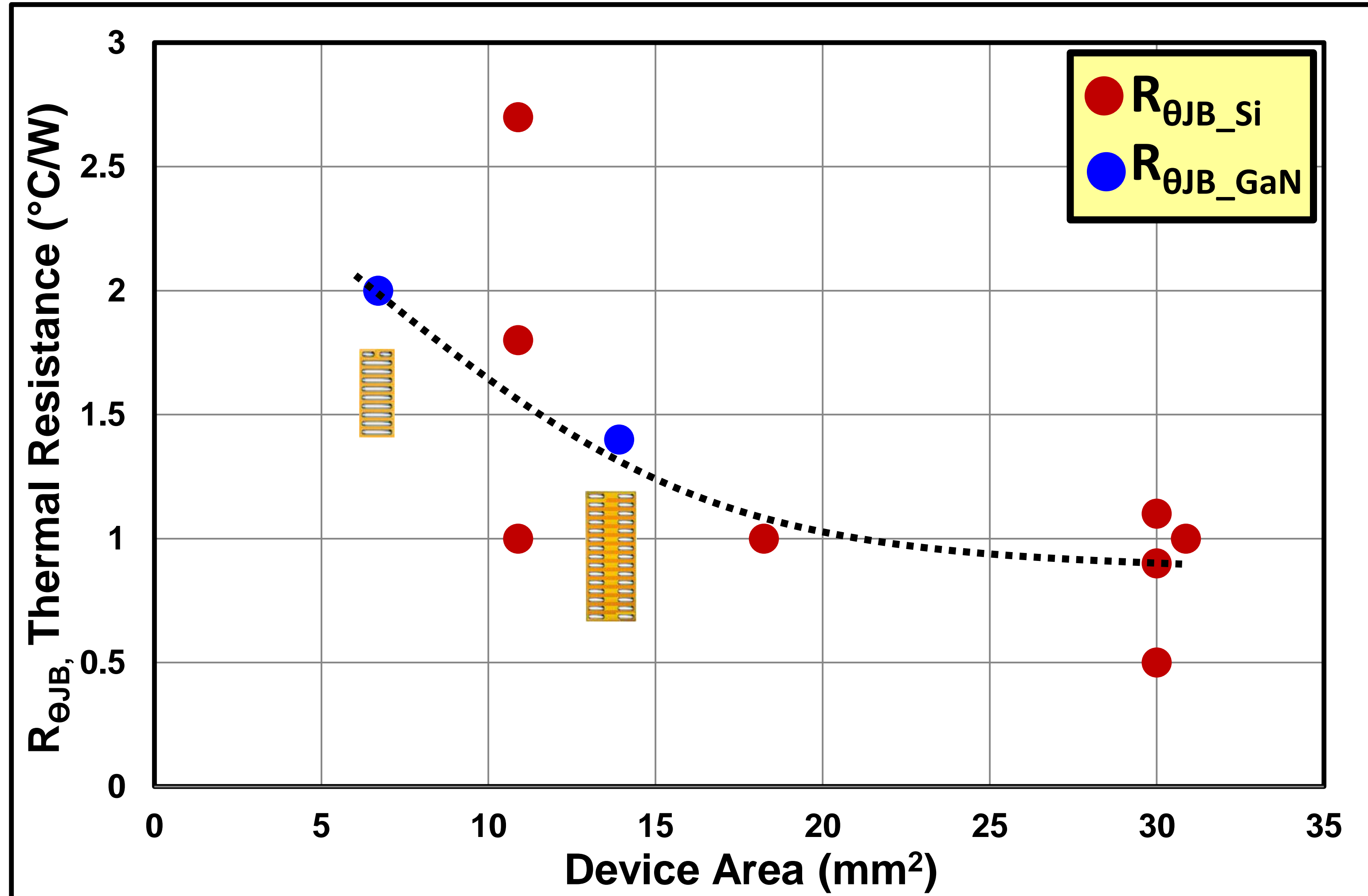
Why eGaN® FETs?

Smaller Size and Thermal Performance

SMD Marketing Package Name	Who?	FootPrint Area (Sq mm)	$R_{\Theta JB}$ (C/W)	$R_{\Theta JC}$ (C/W)	Size (L x W) (mm)	FootPrint Type
PowerPAK® SO8L (Epoxy + Metal Tab)	Silicon	31.62	N/A	**2.7**	6.2 x 5.1	~ SO-8/PQFN
SuperS08 (Epoxy + Metal Foot Pkg)	Silicon	30.00	0.9	**20**	6.0 x 5.0	~ SO-8/PQFN
Can/Direct M (Metal Pkg)	Silicon	30.00	N/A	**1**	6.0 x 5.0	MG-WDSON
Can/Direct S (Metal Pkg)	Silicon	18.72	N/A	**2.9**	4.8 x 3.9	MG-WDSON
Pwr SOT89-3 (Epoxy + Metal Tab Pkg)	Silicon	18.00	N/A	**10**	4.5 x 4.0	~SOT89-3
CSP	EPC	14.03	1.1	**0.4**	6.1 x 2.3	LGA
CSP	EPC	11.96	3.9	**0.45**	4.6 x 2.6	BGA
S308 (Epoxy + Metal Foot Pkg)	Silicon	10.89	N/A	**2.1**	3.3 x 3.3	TSDSON-8
CSP	EPC	6.56	2.0	**1**	4.1 x 1.6	LGA
CSP	EPC	5.76	2.7	**1.1**	3.6 x 1.6	LGA
PowerPAK® SC70-6L (Epoxy + Metal Foot Pkg)	Silicon	4.00	N/A	**11**	2.0 x 2.0	~ SC70-6
CSP	EPC	3.75	8.5	**1.4**	2.5 x 1.5	BGA
CSP	EPC	3.36	4.0	**2**	2.1 x 1.6	LGA
CSP	EPC	1.87	9.3	**3.6**	1.7 x 1.1	LGA
CSP	EPC	1.82	31, 28	**3**	1.35 x 1.35	BGA
CSP	EPC	0.81	65	**6.5**	0.9 x 0.9	BGA

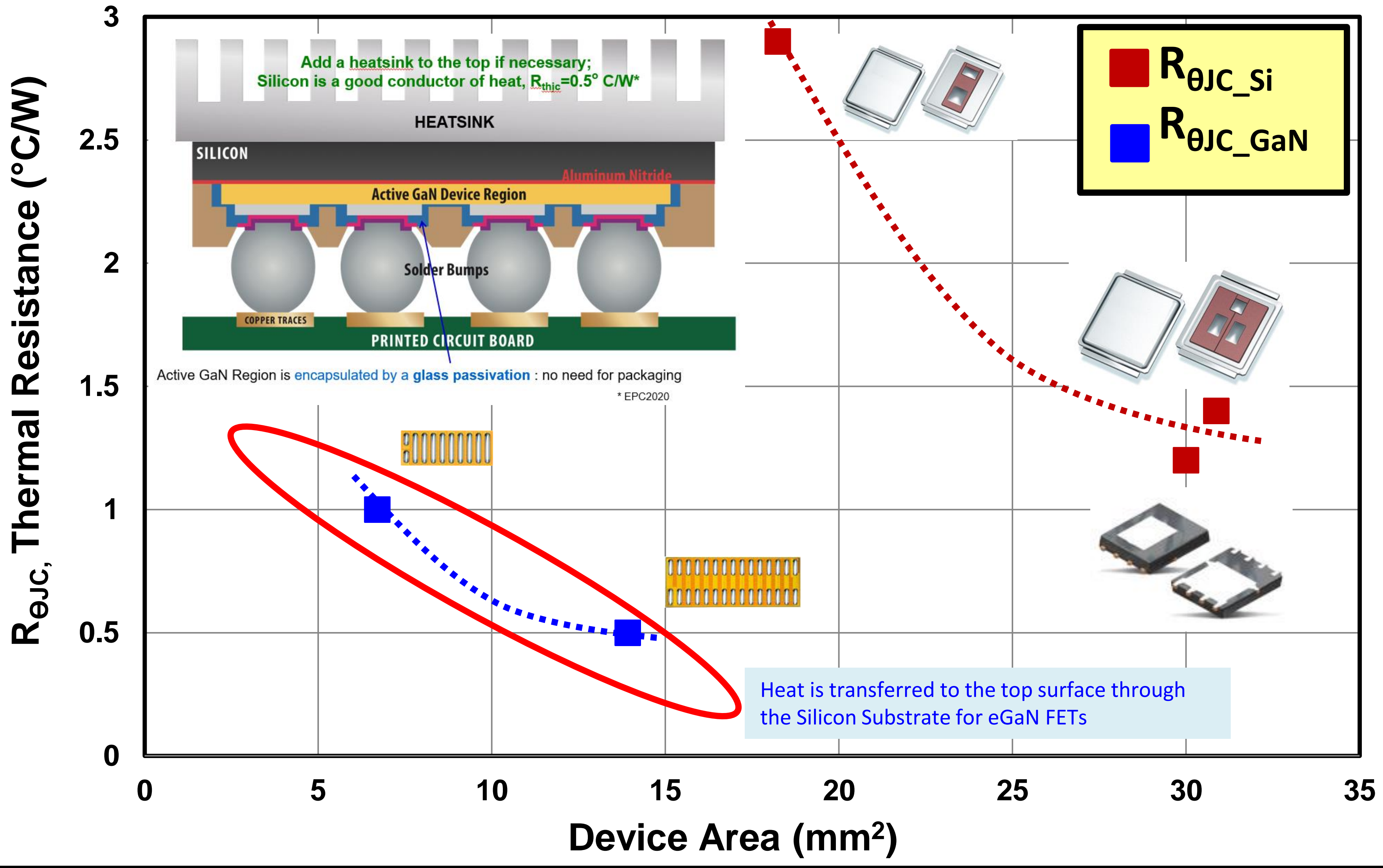
Why eGaN® FETs?

Thermals: Heat into PCB is the same.



Why eGaN® FETs?

Thermals: Heat transfer to top surface superior!



Why eGaN® FETs?

Higher Power for same op temp!

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Q1=98° C

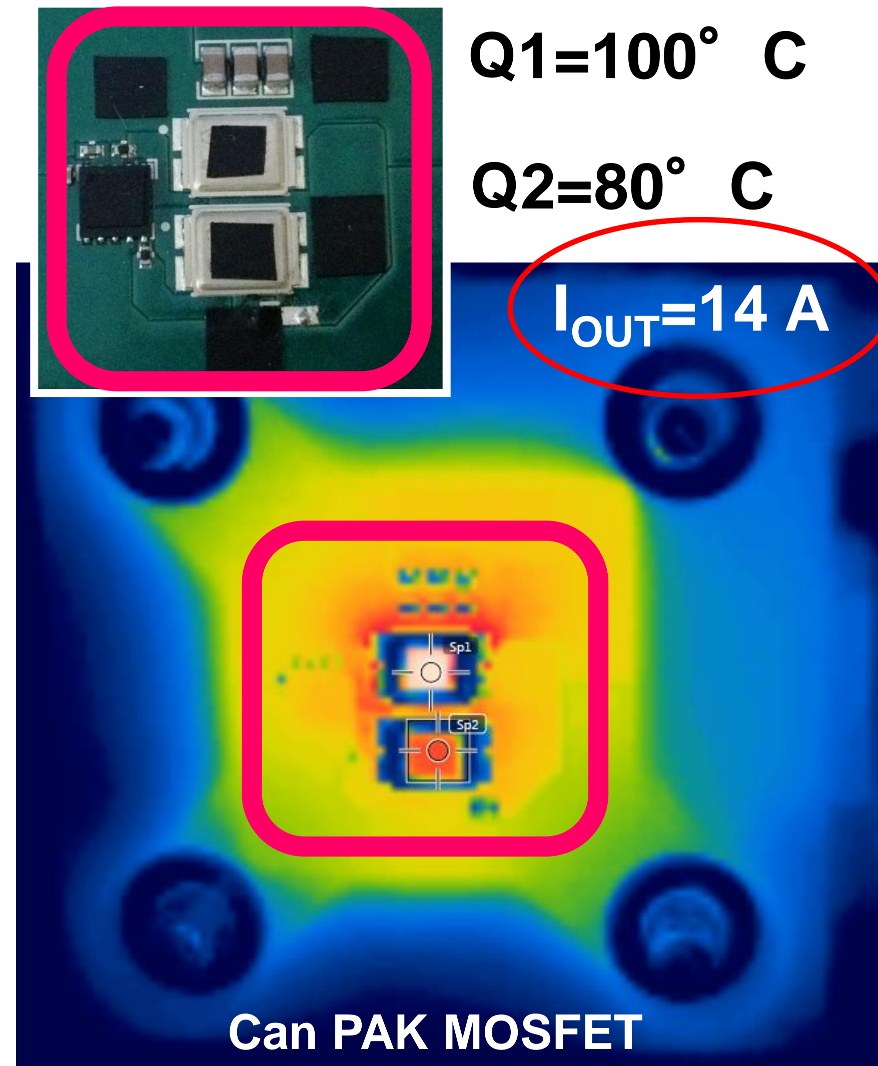
Q2=84° C

I_{OUT}=22 A

100° C

25° C

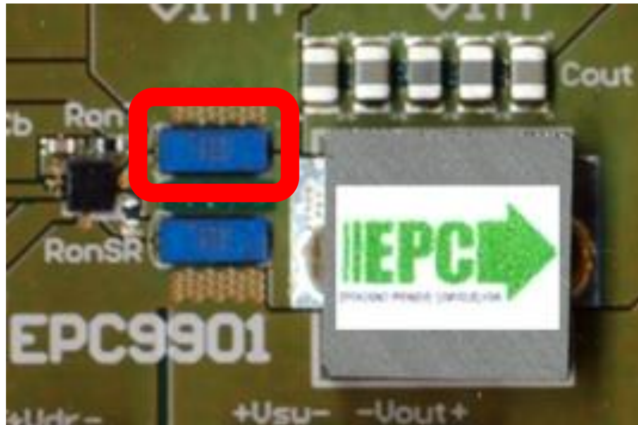
eGaN FET



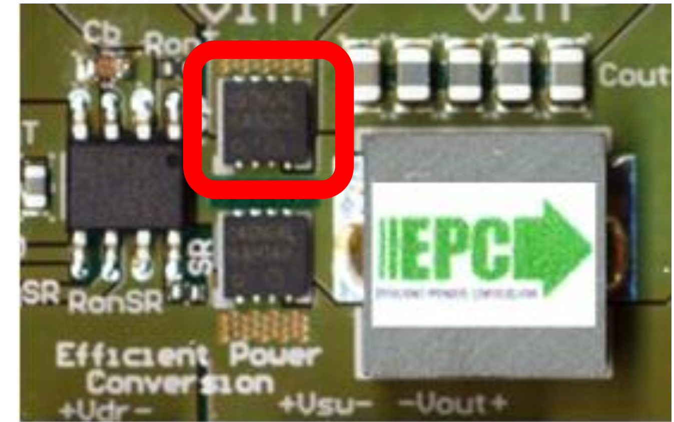
Fan Speed=200 LFM V_{IN}=48 V V_{OUT}=12 V f_{sw}=300 kHz L=4.7 µH

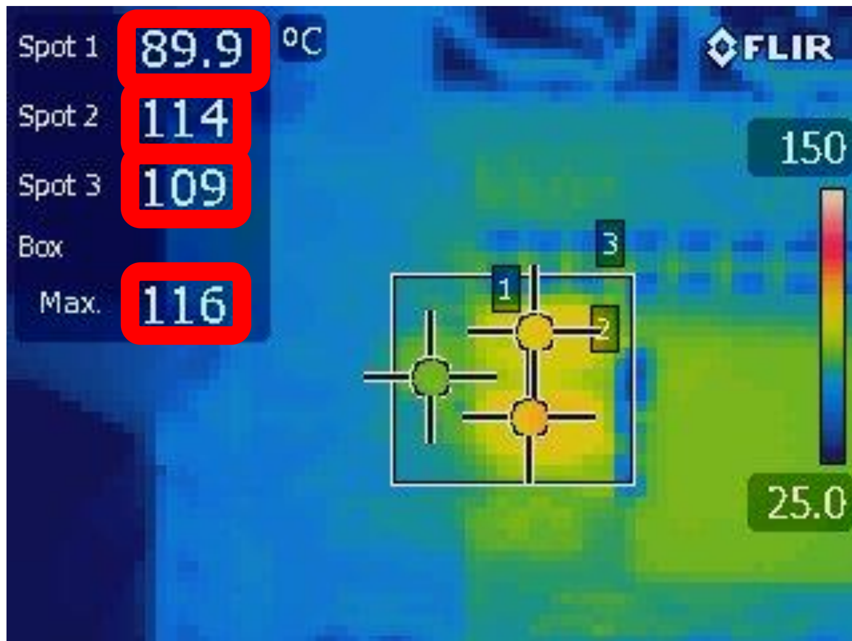
Why eGaN® FETs?

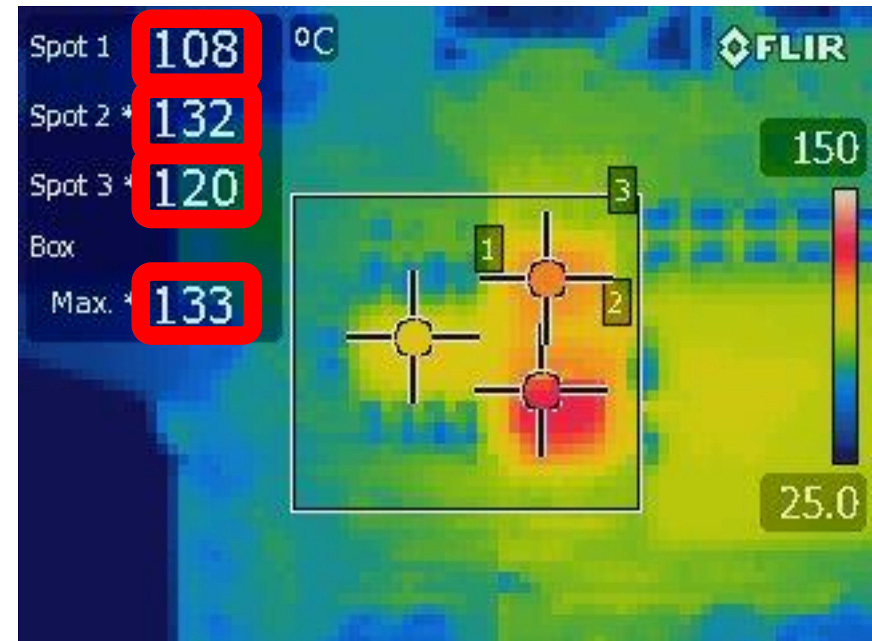
Smaller with Lower Op Temp for same power!



GaN is
38% Smaller
13% Cooler







V_{IN}=12 V, V_{OUT}=1.2 V, I_{OUT}=20 A, f_{sw}=1 MHz, L=300 nH

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eGaN® Gate Drive

Vgs rating and example $R_{ds(on)}$ curve

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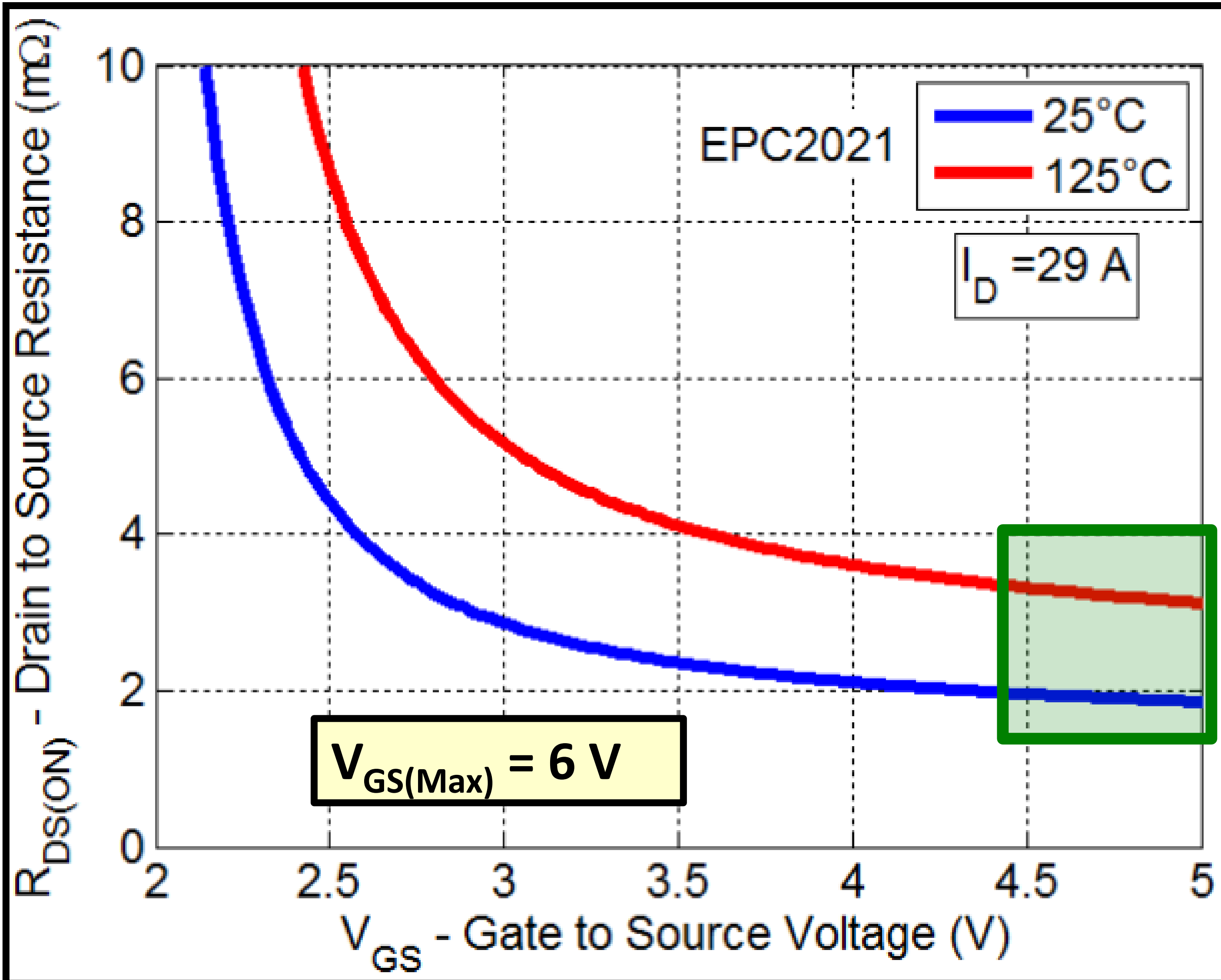

Rds-on spec is specified at 5Vgs.

<u>There is no guarantee of Rdson performance below 5Vgs.</u>

<u>eGaN® FET's are not 3.3V compatible.</u>

Voltages as low a 4.5Vgs will have minimum Rds-on impact.

The Vgs voltage is independent of the Vds rating of the FET.

Why eGaN® FETs? Summary

Ultra Small CSP format with no packaging

- Eliminates package parasitic/lead inductance
- Avoids package related reliability issues

Extremely fast switching (~2nS)

Superior Specifications

- Lower switching losses (Qgd, Qgs, Qoss)
- Lower driver losses (Qg)
- Zero Qrr losses (no reverse recovery charge)

Can operate at much higher frequencies

- Reduce size of passive elements
- Improve the power density

Superior dual side cooling for better thermal performance

Easy to use: Normally off & works like N-channel FET

eGaN FETs are ahead of silicon and accelerating faster.

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48V to POL
Point Of Load DC-DC

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Rethink Server Power Architecture with GaN Technology

The following presentation has simplified some things in order to focus on the key topic in the time allowed.

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48V to POL

Presentation Notes and Background

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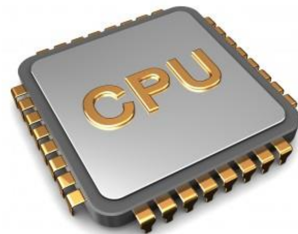
- DC-DC Design Challenges:
  1. Large step down voltage ratios
     - The higher V_{IN} / V_{OUT} ratio, the more difficulty in achieving high efficiency.
       - AC losses go up with higher V_{IN} for the same switching frequency and load
       - **This is a key area where eGaN® beats MOSFET.**
  2. High Current Low V_{OUT} (0.8 to 1.8V)
     - I_{OUT} Load Current can range as high as 160 Amps (or more).
     - I_{OUT} current limit is driven by the peak current requirements.
     - I^2R losses force the high current DC-DC to be located next to the load.

The DC-DC that goes next to the load is called the **Point Of Load (POL)**

The POL Loads:

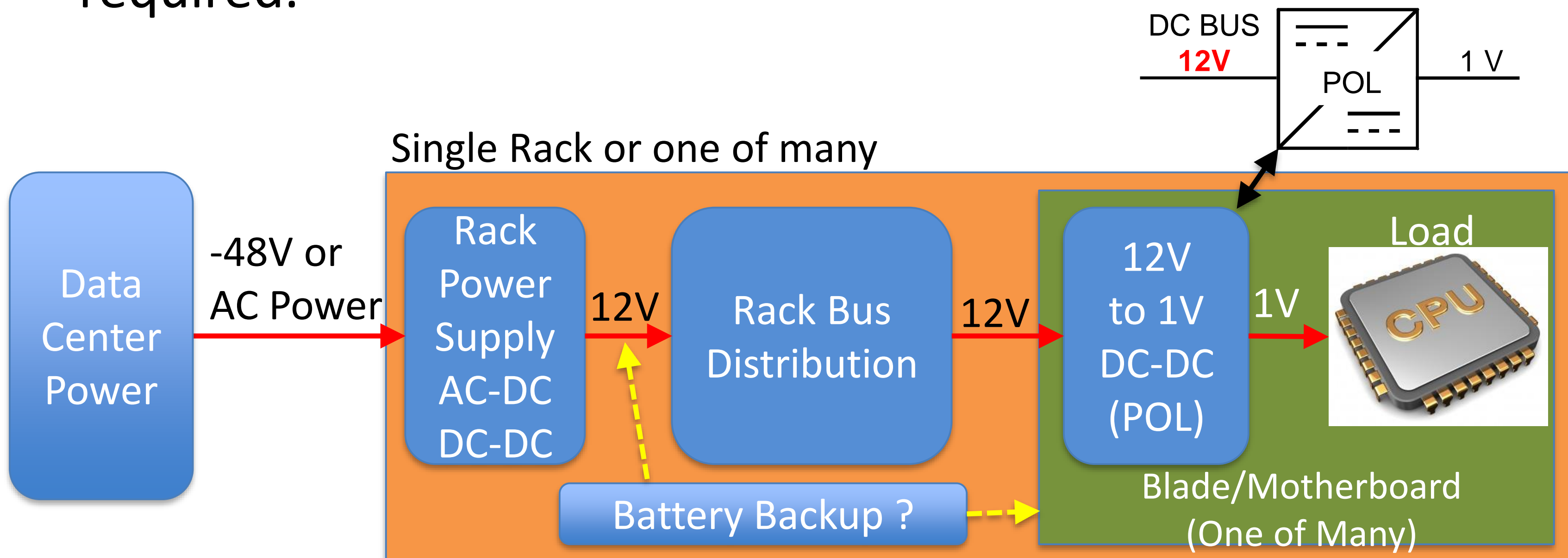


More information: http://powerpulse.net/48v-to-1v-conversion-the-rebirth-of-direct-to-chip-power/

48V to POL

Telecom/Datacenter: Traditional Design

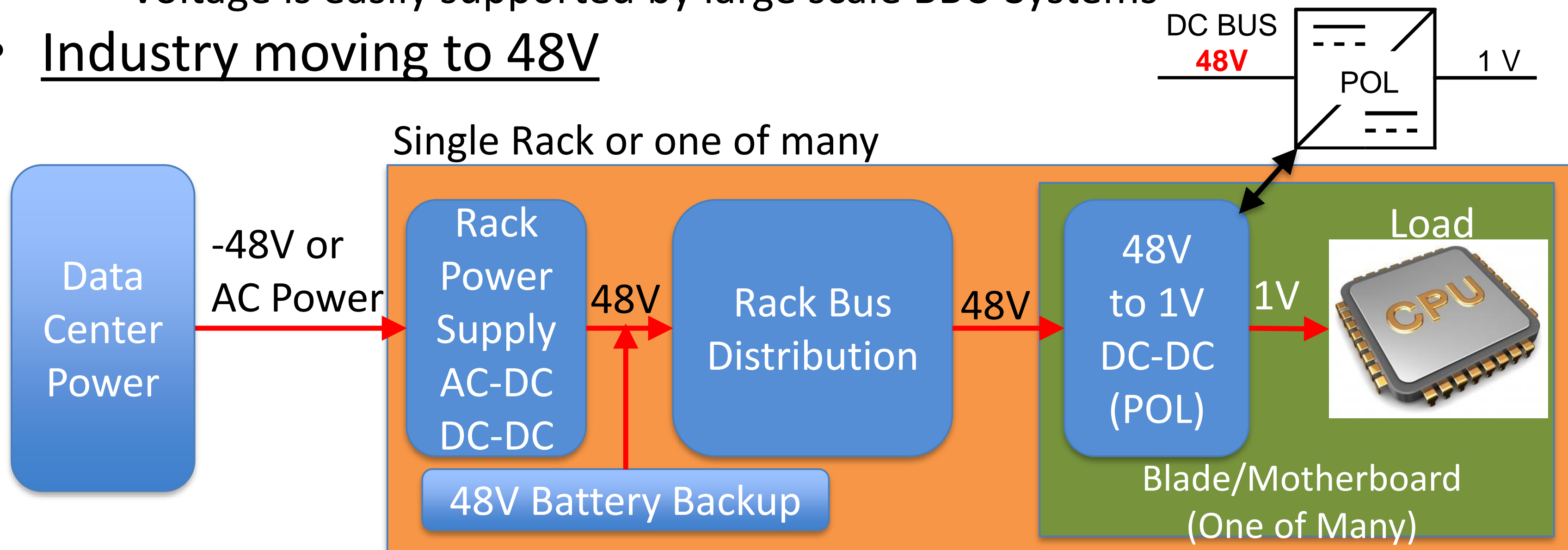
- Typical Rack Power Today
  - Rack Vin: -48VDC Telecom or AC power.
  - Rack Bus Distribution: +12VDC using heavy copper bars
  - Motherboard Distribution: +12VDC using multiple copper planes and/or traces in parallel.
  - Non standard expensive Battery BackUp (BBU) systems if required.



48V to POL

Telecom/Datacenter: Future Goals

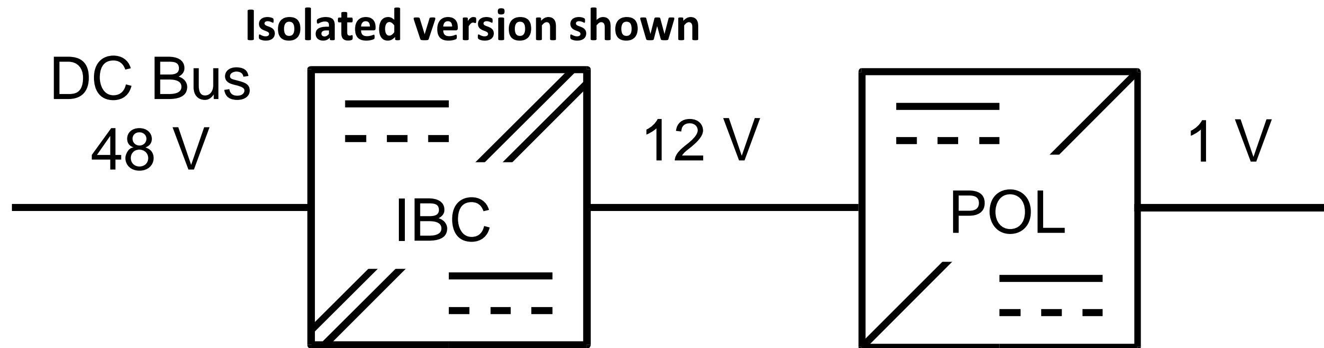
- Goals:
  - Establish one voltage for whole rack system. Rack Bus = Motherboard Bus
  - Improve distribution efficiency
  - Lower power distribution cost by <u>getting rid of the expensive copper</u>
  - Use a voltage that easily supports direct high power Battery Backup
- Raising 12V to 48V:
  - 16X reduction in I^2R losses
  - Reduces $$ Copper Cost for system and motherboards
  - Voltage is easily supported by large scale BBU Systems
- <u>Industry moving to 48V</u>



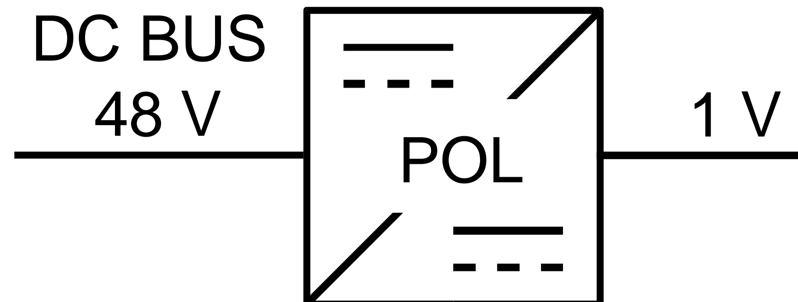
48 V_{IN} to POL

Two Design Approaches

1. **Two stage Isolated Intermediate Bus Converter IBC + POL Architecture** (Two DC-DC's in series)

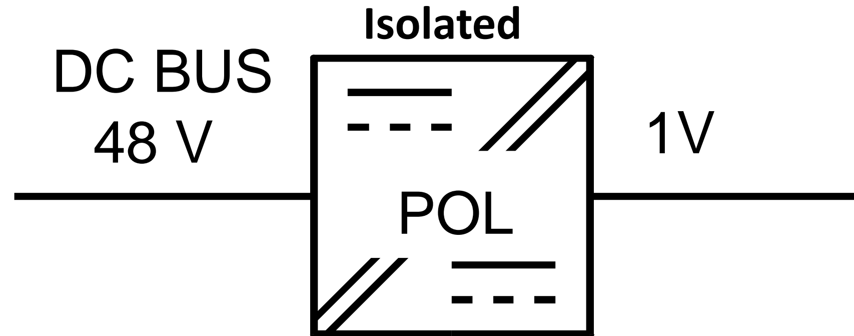


2. **Single Stage Non Isolated Bus POL Architecture** (One DC-DC)

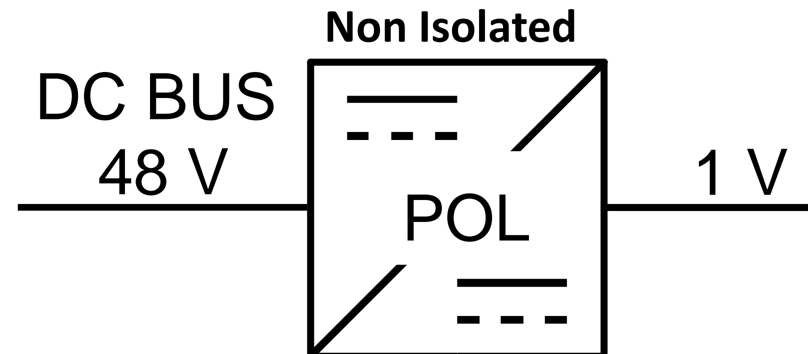


Single Stage POL can come in two Topologies

1. Transformer based such as using a Half Bridge Converter offers isolation and better efficiency (TI Demo).

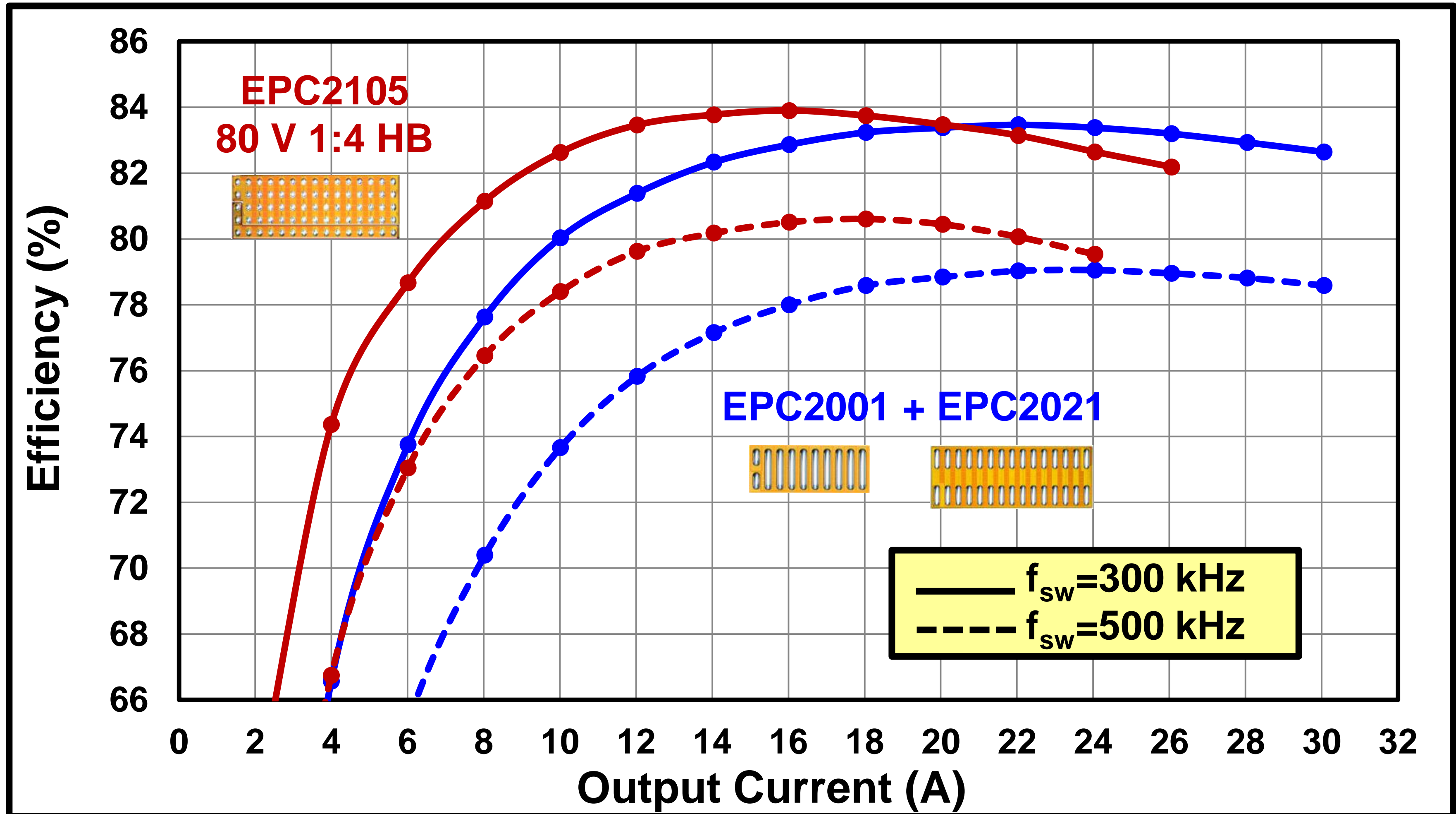


2. Buck Converter offers the smallest solution footprint at the lowest cost. Multiphase capable.



48 V_{IN} to 1V POL Single Stage Buck

Different eGaN FET combinations offer different peak efficiency sweet spots.



V_{IN}=48 V V_{OUT}=1 V L=330 nH

48 V_{IN} to 1V POL

1 vs 2 Stage Power Architecture Comparison

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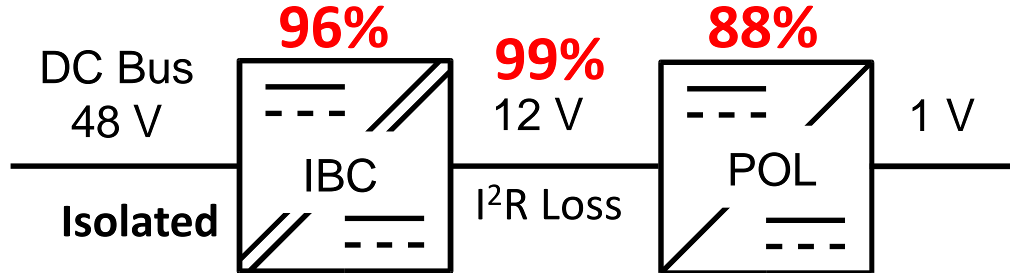
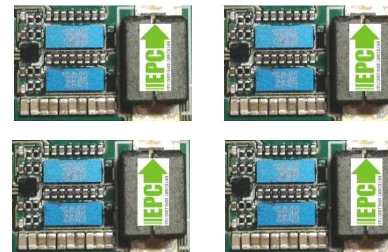
2 Stage: IBC + POL Architecture



EPC9115



f_{sw}=300 kHz 550 W/in³

f_{sw}=1 MHz 500 W/in³

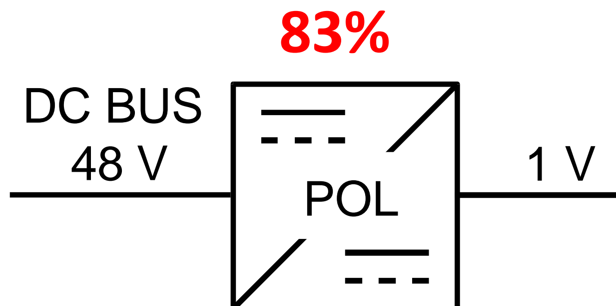
96% x 99% x 88%

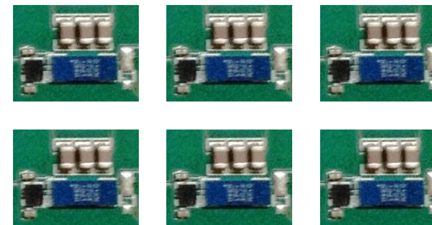
≈ 83-84%

≈250 W/in³

Same

1 Stage: POL Buck Architecture





f_{sw}=300 kHz 300 W/in³

Optimized H bridges

≈ 83-84%

≈300 W/in³

48V to 1V

1 Stage POL Archecture Choices

- Single DC-DC POL Topology Summary:
  - Buck Converter
    1. Lowest Cost
    2. Uses simple but large inductor. Depends on switching frequency.
    3. Use the least amount of PCB space.
    4. Efficient as dual DC-DC solution.
    5. No Isolation option.
    6. Multiphase easily supported and required for high current.
  - Half Bridge Converter (TI Demonstration Board Next)
    1. Highest efficiency.
    2. Supports Isolation
    3. Takes up less space than dual DC-DC solution.
    4. Large Transformer required
    5. Cost more than a Buck Converter.
    6. Takes up more PCB space than a Buck converter.
    7. Multiphase current increase not good option.

Demonstration System

Texas Instruments PM4497 48V to 1V DC-DC Converter

EFFICIENT POWER CONVERSION

Texas Instruments PM4497

Overview and Specifications

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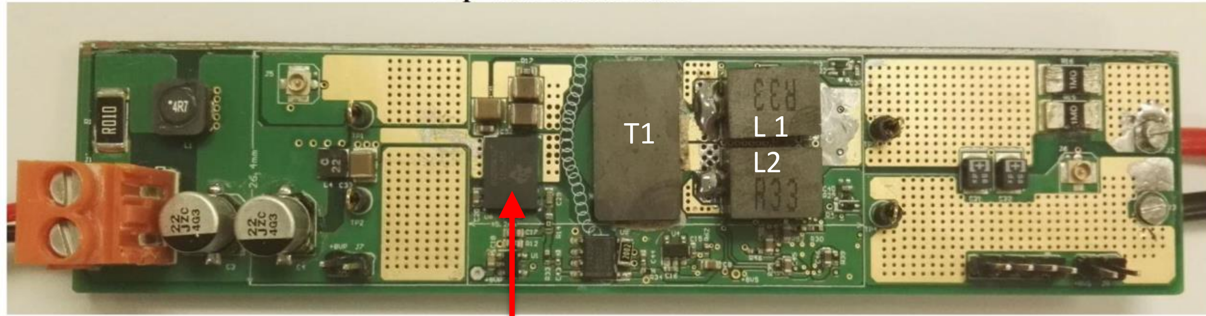
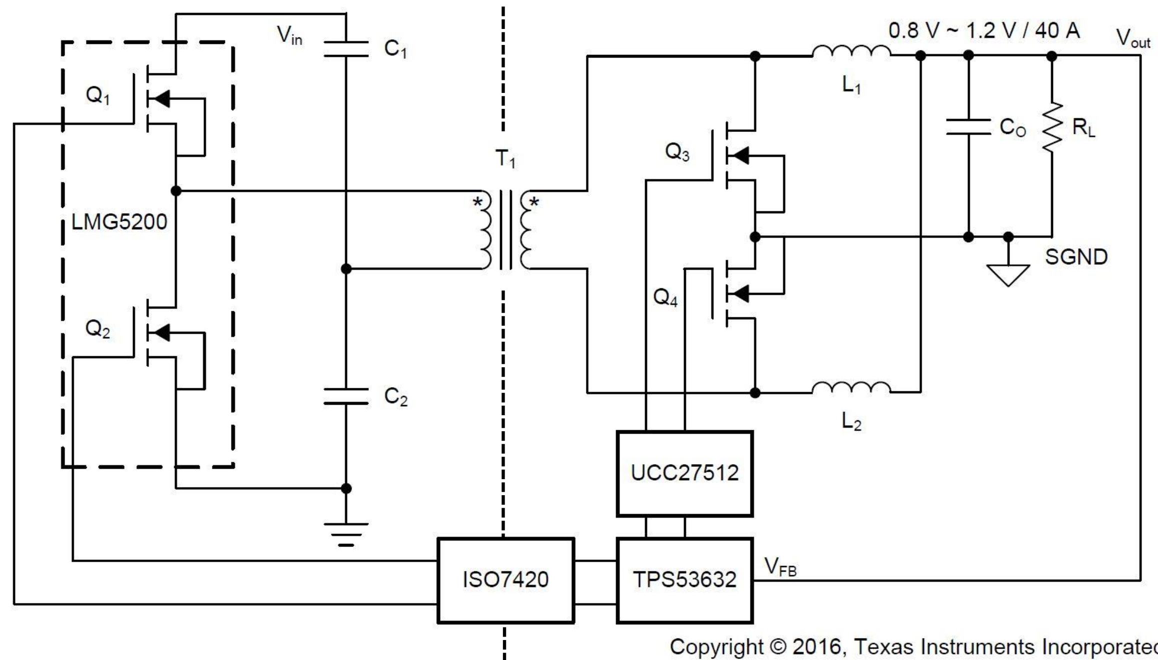
Specifications:

- Vin: 36 – 60V
- Vout: 1V
- Iout (max): 40Amps
- Isolation: Yes, Transformer
- Topology:
  - Half Bridge,
  - Dual inductor with Synchronous Rectifiers
- Peak Efficiency*:
  - 92.9% @ ~15 Amps
  - 48Vin @ 600 kHz
- Footprint Size:
  - 45 x 26 x 11 mm
- GaN FET: LMG5200



TI LMG5200: Dual GaN FET + Driver



* TI Test Report July 2016 http://www.ti.com/lit/ug/tiduc86/tiduc86.pdf

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Texas Instruments PM4497

LMG5200: Half Bridge Power Stage

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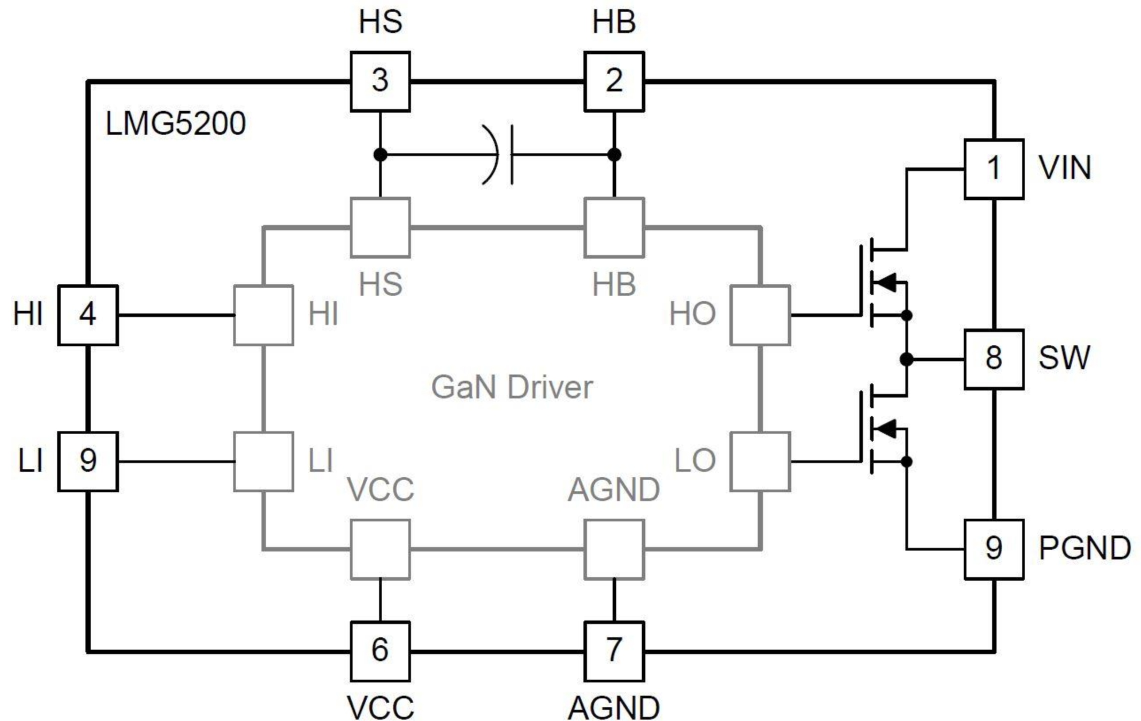
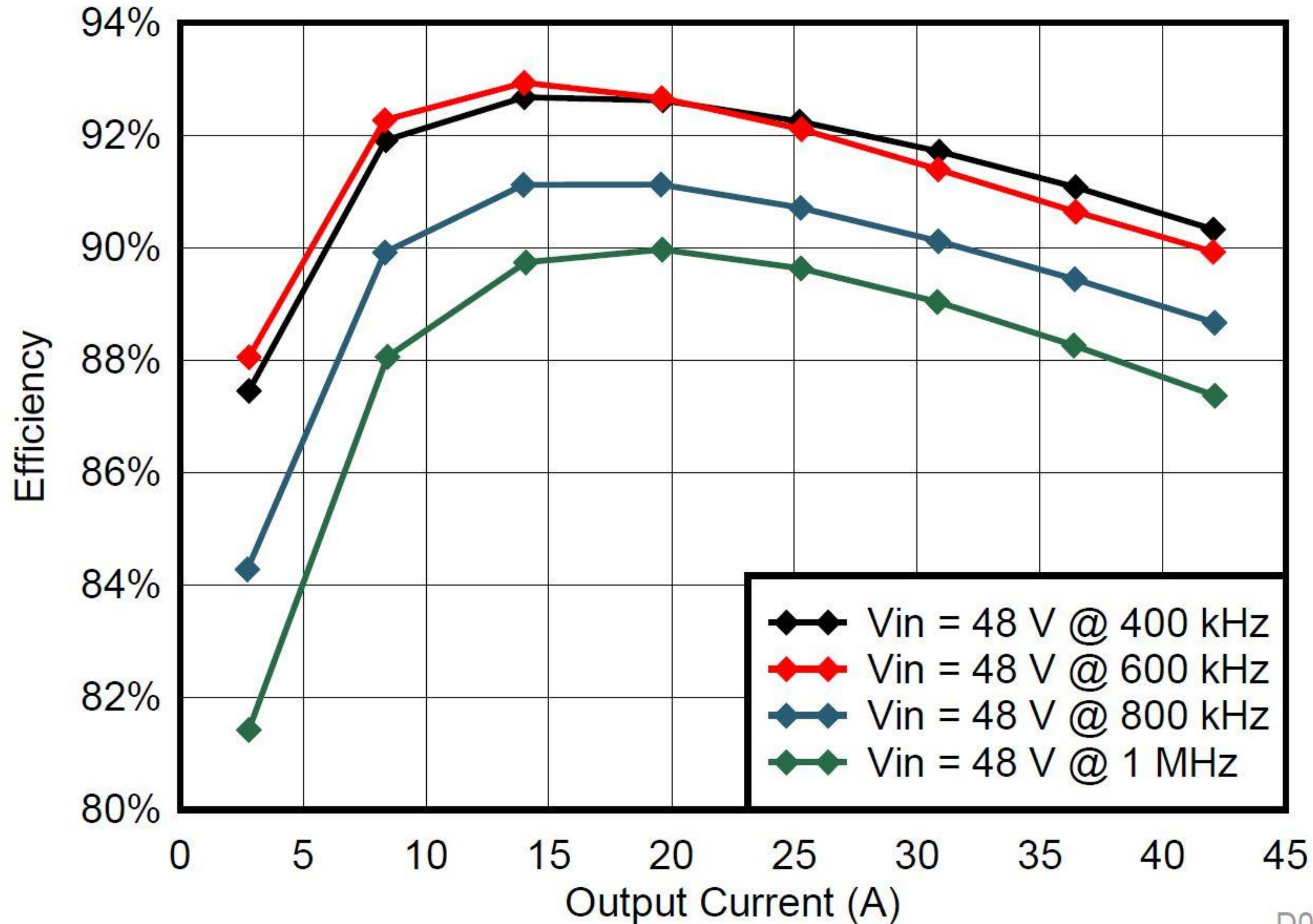
- **Specifications:**
- Two GaN FETs + Gan Driver
- 80V 40A 18mOhm FETs
- Internal Bootstrap Supply
- 2nS Propagation Delay Matching
- Hysteretic Input eliminates chattering or unwanted turn on.
- Creepage and Clearance Compliant footprint.
- 10 nS dead time.
- 6 x 8 mm Footprint.
- Integrated Package:
    - Minimizes gate path current loop.
    - Eliminates high side gate drive Common Source Inductance (CSI)
    - Minimizes High Speed Loop Inductance.



Texas Instruments PM4497

Efficiency @ 48V

Power Conversion Stage Only. Efficiency does not take into account controller losses.

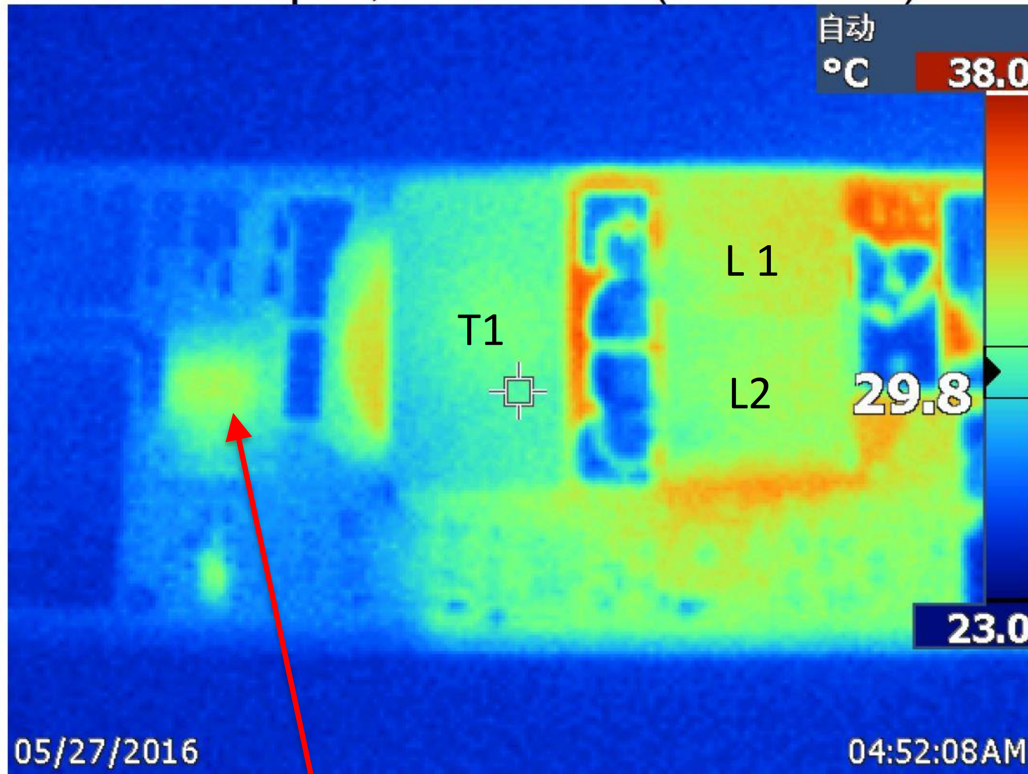


Texas Instruments PM4497

Thermal Overview

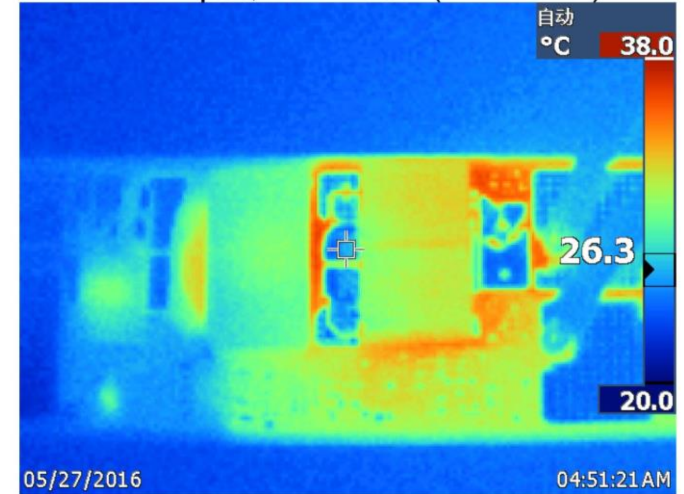
Images taken with Fan Cooling ~ 1m/sec rate

48V Input, Full Load (1.0V/40A)

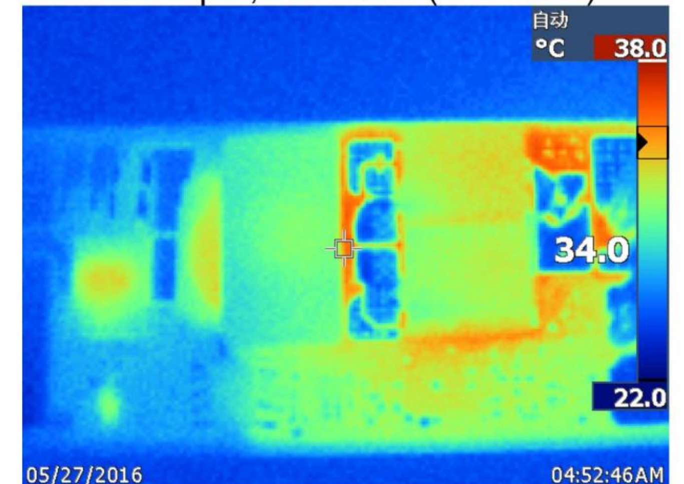


LMG5200 (U1)

36V Input, Full Load (1.0V/40A)



60V Input, Full Load (1.0V/40A)



* TI Test Report July 2016 http://www.ti.com/lit/ug/tiduc86/tiduc86.pdf

48V to 1V

eGaN® FETs offers Solutions

- Performance: up to 30% over MOSFET.
- All DC-DC Power FET locations can benefit
  - Up to 50% lower Q_{oss} @ 100Vds rating gives you a design tradeoff choices
    - Lower AC losses for same low 300kHz MOSFET frequency
    - Same AC losses at 600-700kHz but get reduce magnetics size
  - Lower Qg and Qgd = Faster Switching (~2nS):
    - Lower Transition Losses
    - Enables Lower Dead Time = Lower Sync Rectification Losses
  - No Qrr Losses in reverse conduction.
    - No MOSFET PN diode recovery issues
  - Smaller FET Size allows smaller solution footprint.

EPC Resources & Support

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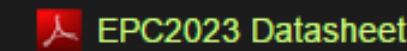
- Design Review & Layout Support
- Demo Boards
  - We share Gerber files, schematics and BOM for ease of adapting the design
- Comprehensive Web with
  - Device specifications and models
  - Application notes
  - Reliability data
- Digi-Key availability at time of Introduction

Datasheet



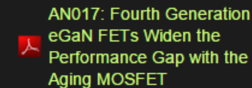
Demo/Development Boards

EPC9031
EPC9018
EPC9201

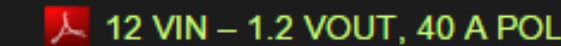
Quality & Reliability

Reliability Reports
RoHS Statement
REACH Statement

Application Notes



Design Examples



Device Models

PSPICE (.net)
TSPICE (.sp)
LTSPICE (.zip)
Spectre Model (.scs)
Altium Library (.zip)
Thermal Model

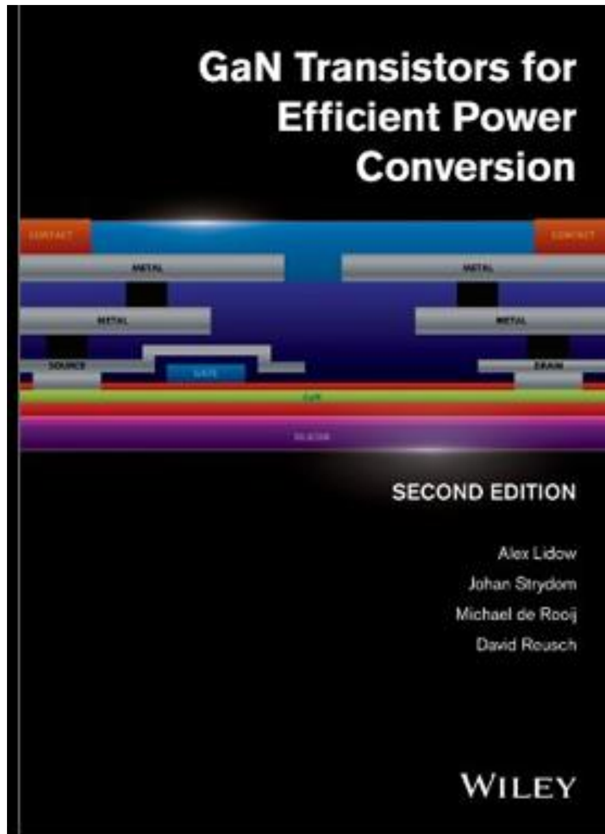
Training Videos

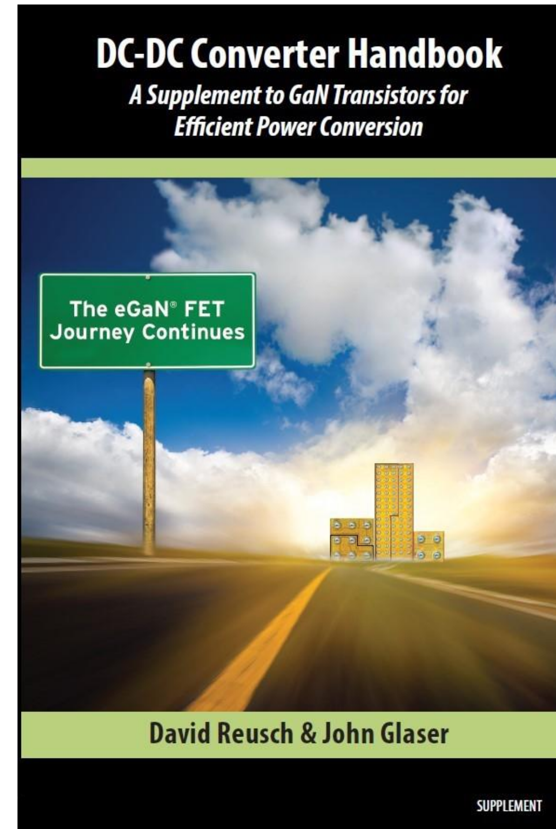
Generation 4 eGaN® FETs

Mark Gurries
Field Applications Engineering:
mark.gurries@epc-co.com
408-580-7827

Andrea Mirenda
Vice President of Sales, Americas
Andrea.Mirenda@epc-co.com
408.332.2651

Communicating the Learning Curve





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Summary

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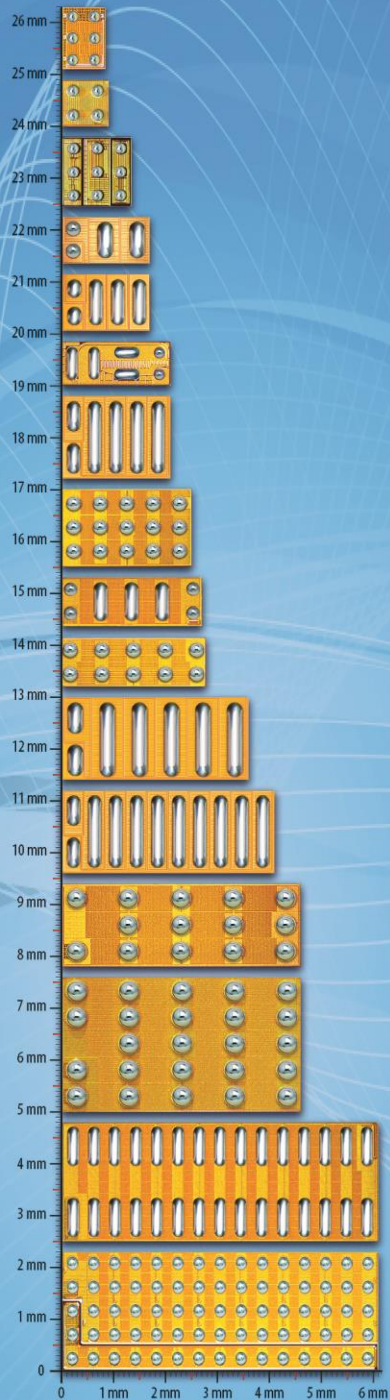
- EPC is a reliable partner
- Product offering and road map quite exciting for efficiency improvements
- Reliability results are robust
- Have Inherently Rad hardened products
- Applications and MFG support



Thank you!

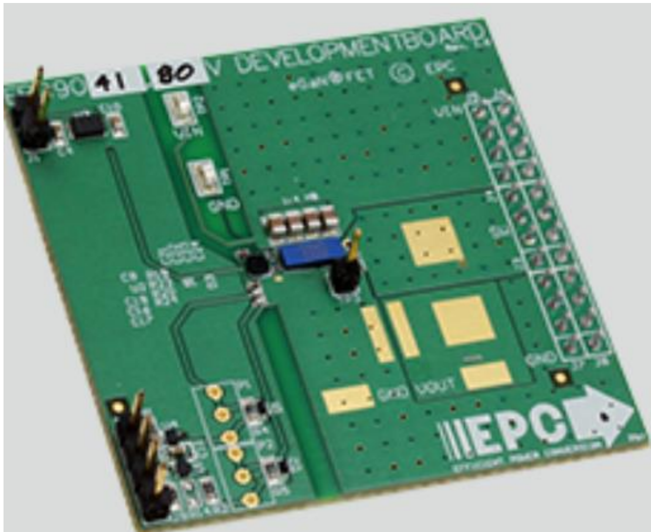
Appendix

- EPC 48V to POL Application Demoboards
- Growing Eco System for Low Voltage eGaN®
  - Gate driver
  - Magnetics
  - Controllers
- Reliability

48V to POL Demoboards

48V to POL Demoboards

Non isolated FET demoboards for testing.



EPC2105*
80 V 1:4 HB

http://epc-co.com/epc/Products/DemoBoards/EPC9041.aspx

http://epc-co.com/epc/Products/DemoBoards/EPC9019.aspx

EPC2001 + EPC2021

48V-> POL Applications

eGaN® Fets for Single Stage Conversion

Part #	Config	VDS max	VGS max	Max RDS(on) (mΩ)	Qg typ (nC)	QGS typ (nC)	QGD typ (nC)	QOSS typ (nC)	ID (A)	Pulsed ID (A)	Tj max	Package (mm)	DemoBoard
EPC2202	AEC Single	80	5.75	17	3.2	1	0.55	18	18	75	150	LGA 2.1 x 1.6	See EPC2016C
EPC2103	Half Bridge	80	6	5.5	6.5	2.2	1.1	30, 34	30	195	150	BGA 6.05 x 2.3	EPC9039
EPC2029	Single	80	6	3.2	13	3.4	1.9	53	48	360	150	BGA 4.6 x 2.6	EPC9046
EPC2105	Half Bridge	80	6	14.5, 3.6	2.7, 11	0.9, 3	0.5, 2.1	11, 51	10, 40	70, 300	150	BGA 6.05 x 2.3	EPC9041
EPC2021	Single	80	6	2.5	15	3.4	2.3	63	90	420	150	LGA 6.05 x 2.3	EPC9034
EPC2016C	Single	100	6	16	3.4	1.1	0.55	16	18	75	150	LGA 2.1 x 1.6	ECP9010C
EPC2001C	Single	100	6	7	7.5	2.4	1.2	31	36	150	150	LGA 4.1 x 1.6	EPC9002C
EPC2045	Single	100	6	7	5.2	1.7	1.1	21	16	130	150	BGA 2.5 x 1.5	EPC9080
EPC2104	Half Bridge	100	6	6.8	6.8	2.3	1.4	35, 41	30	180	150	BGA 6.05 x 2.3	EPC9040
EPC2032	Single	100	6	4	12	3	2	66	48	340	150	BGA 4.6 x 2.6	EPC9062
EPC2022	Single	100	6	3.2	13.2	3.4	2.4	71	90	390	150	LGA 6.05 x 2.3	EPC9035

eGaN® Optimized Gate Drivers

eGaN® Optimized Gate Drivers

Single Gate Drivers

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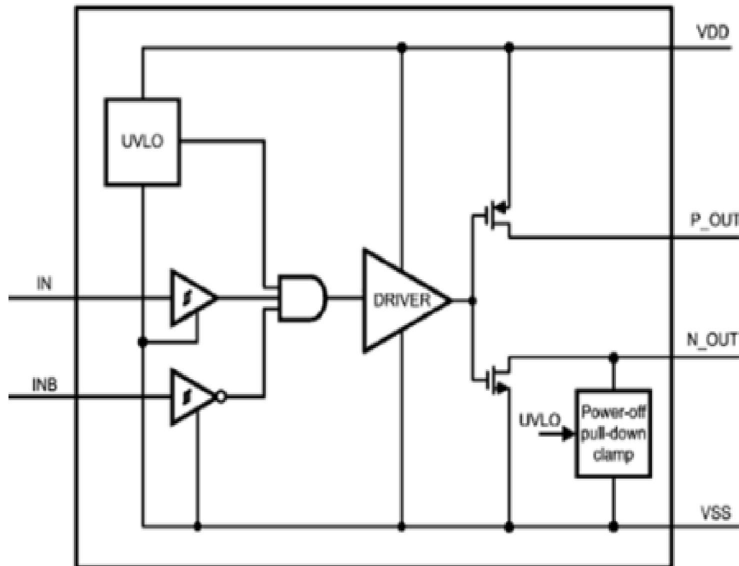
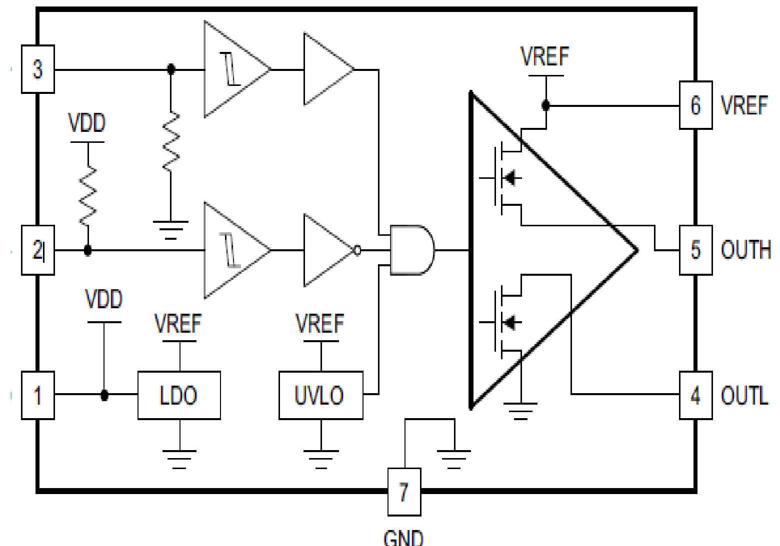
UCC 27611

- 4-18V supply with UVLO
- **Internal 5V Supply Regulator.** **Ready for eGaN**
- Sink 6A & **Source 4A** (0.35Ω & 1.0Ω)
- Split output for adjustable rise/fall time control for each FET.
- 2x2mm package with thermal pad
- Inverting input option.
- 14ns propagation delay



LM5114

- 4 to 12.6V supply. **Must use 5V for eGaN FETs.**
- **Sink 7.6A** & Source 1.3A (0.23Ω & 2.0Ω)
- Split output for adjustable rise/fall time control for each FET.
- LLP-6 and SOT23-6
- Inverting gate input option
- UVLO
- 12ns propagation delay.



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eGaN® Optimized Gate Drivers

LMG1020 Single Gate Drivers

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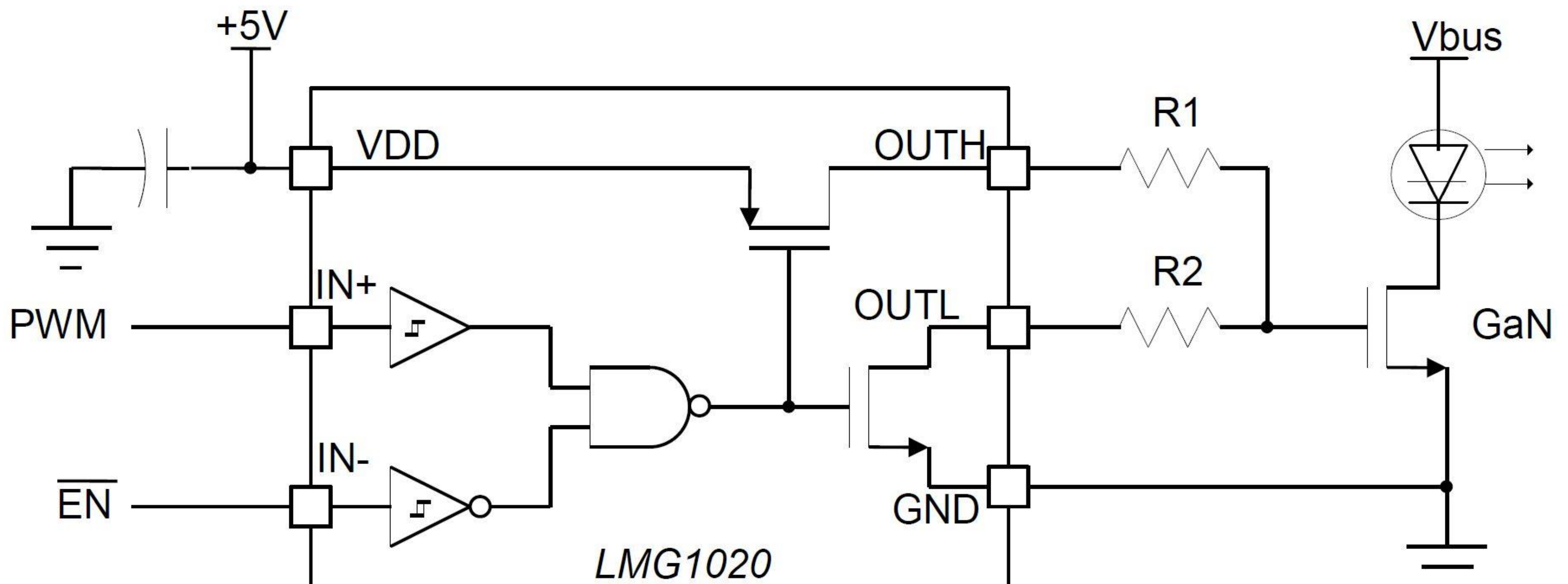
- Sink 5A & **Source 7A**
- 1.2 x 0.8 mm 2 x 6 BGA package
- 400pS Rise time.
- 4.5ns propagation delay (2.5ns typ)
- Up to 60MHz @ 50% Dutycycle

- 1nS typical minimum pulse width
- Split output for adjustable rise/fall time control for each FET.
- 150K input resistors force default off state.
- 0.5V input hysteresis to reject spikes.
- UVLO & Overtemp

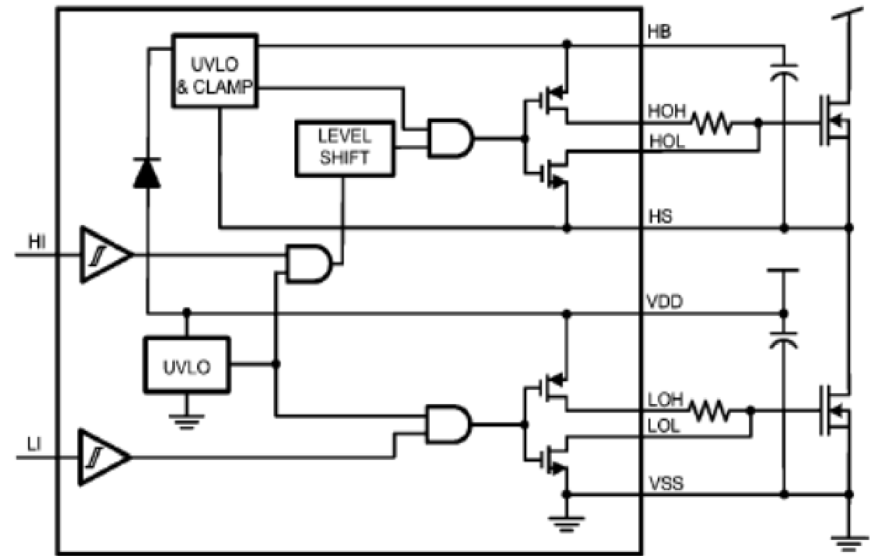


eGaN® Optimized Gate Drivers
LMG1205 Half Bridge Driver

- Internal bootstrap supply voltage
  - **5V clamping for High Side driver**
- 107V max at Switch Pin (HS)
- 5 A sink & 1.2A Source (0.6Ω & 2.1Ω)
- Split output for adjustable rise/fall time control for each FET.
- 28ns propagation time
- **1.5nS high side low side delay matching**
  - **Very important for dead time**
- 2 x 2mm 12 pin BGA
- **Up to 2MHz**
- **Up to 14 MHz with GaN Sync Bootstrap modification.**
- **No interlocking between inputs.**
  - **Can be used as a dual low side driver.**
- 200K Pulldowns on inputs.
- UVLO

LM5113 vs LMG1205 Comparison:

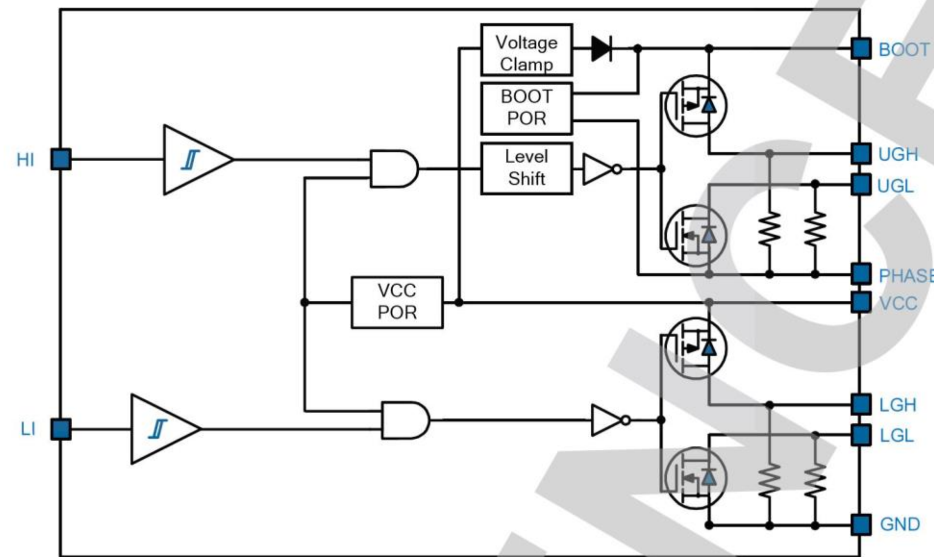
- Replaces LM5113 Driver
- Pin compatible.
- Improved Design.
- Better Physical Performance.



eGaN® Optimized Gate Drivers
UP1996A Half Bridge Driver

- Internal bootstrap supply voltage
  - **5V clamping for High Side driver**
- 100V max at Switch Pin (HS)
- Driver Resistance 0.7Ω on & **0.4Ω** off.
- Split output for adjustable rise/fall time control for each FET.
- **15ns** propagation time
- **1.5nS high side low side delay matching**
  - **Very important for dead time**
- 2 x 2mm 12 pin BGA
- **Up to 3MHz**
- **Up to 14 MHz with GaN Sync Bootstrap modification.**
- **No interlocking between inputs.**
  - **Can be used as a dual low side driver.**
- 200K Pulldowns on inputs.
- UVLO

Better Performance than LMG1205



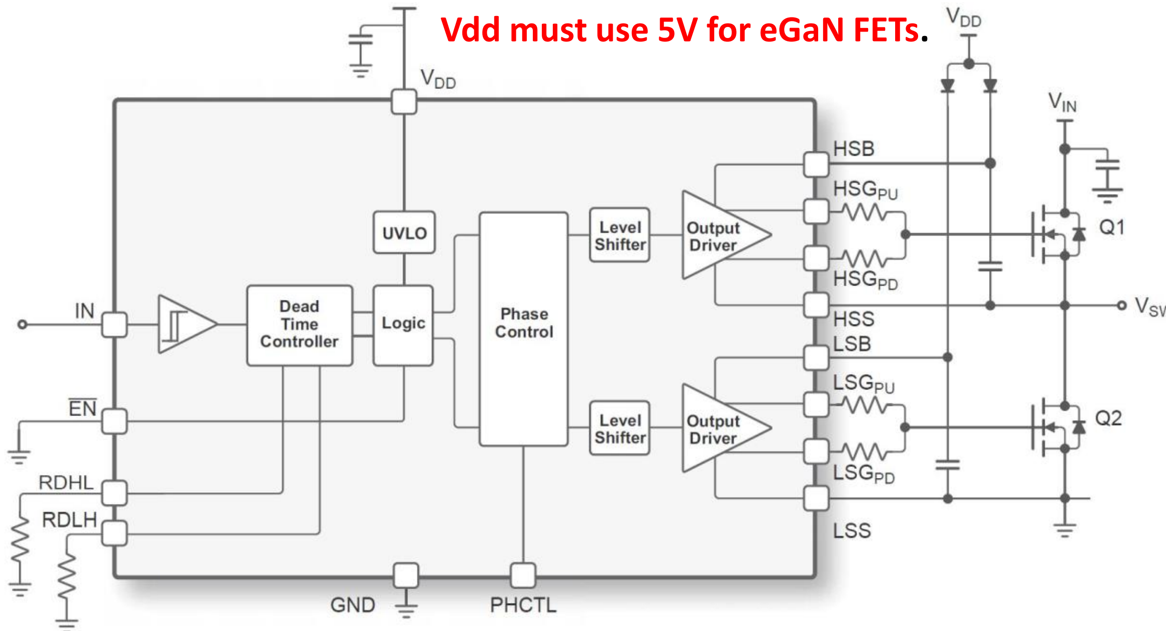
eGaN® Optimized Gate Drivers

PE29102 DrGaN type Half Bridge Driver

- 100V max at Switch Pin (HSS to LSS)
- 4 A sink & 2A Source
- Resistor programable Dead Time control
  - 1.8nS to 23nS
- < 1nS rise/fall time
- 9.1ns propagation delay time
- 5nS minimum input pulse width

- Split output for adjustable rise/fall time control for each FET.
- Small 2 x 1.64 mm 16 pin 5x4 BGA
- Up to 40MHz @ 50% dutycycle
- Single PWM Input control both FETs
- Phase and Enable control inputs
- UVLO

Vdd must use 5V for eGaN FETs.



Bootstrap Diode: Use very small schottky diode such as BAS40LP.

Must place schottky "Catch" diode in parallel with Q2 to protect Q1 gate drive from overvoltage.

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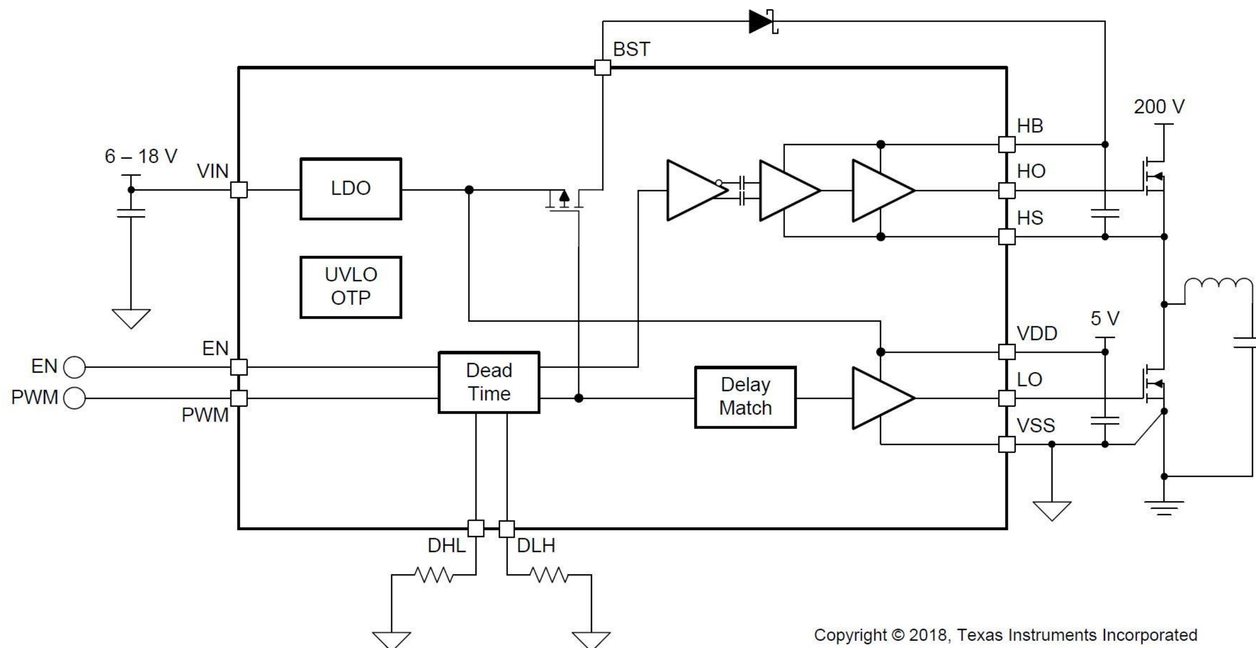
eGaN® Optimized Gate Drivers
LMG1210 Half Bridge Driver

- **200V** max at Switch Pin (HSS to LSS)
- 3.1 A sink & 1.5A Source
- Resistor programable Dead Time control
- 0nS to 20nS
- 0.5nS rise/fall time unloaded. 5.6/3.3ns @ 1nF
- 10ns propagation delay time
- 1.5nS High Side to Low Side delay matching.
- 2.7nS minimum input pulse width
- Up to 50MHz @ 50% dutycycle
- 300V/ns + 1pF switch node cap = High Noise Immunity

- 6 – 18V Vcc supply
- On Board 5V supply regulator
- Synchronous Bootstrap eliminates Top FET Vgs overcharge
- External Schottky eliminates bootstrap switching losses at high operating frequency. No Diode Qrr losses.
- Small 3 x 4 mm 20 pin WQFN
- **Dual input operating modes:**
- Single PWM Input + Enable control inputs (DrMOS/GAN)
- Separate Hi and Lo inputs like LMG1205.
- UVLO



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New Industry-First IHLP-1616BZ-0H High Frequency IHLP® Inductor Series Boosts DC/DC Efficiency

Devices Feature High Frequency Performance Up to 10 MHz With Lowest Losses of Any Composite Inductor at 1 MHz and Above

Product Benefits:

- High frequency performance up to 10 MHz
- Industry-low losses for frequencies ≥ 1 MHz
- Typical DCR from 5.5 mΩ to 26.6 mΩ
- Low inductance values from 0.10 µH to 1.0 µH
- Rated current to 45.0 A
- Handle high transient current spikes without saturation
- RoHS-compliant, halogen-free, and Vishay Green

Market Applications:

- Notebook and desktop computers, sensors, cameras, POL converters, and various battery powered devices that require one or more regulated voltages

EFFICIENT POWER CONVERSION

Growing Eco System For eGaN®
GaN Compatible Controllers

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- **Synchronous Buck**
  - Analog Devices: LTC7800
  - Microchip: MIC2103/4, MIC2127A
  - TI: LM5140, TPS40400
- **General Purpose/Multiphase**
  - Microchip: dsPIC33xxxxxxxx series
  - TI: Delfino TMS320F283xxx Series. Piccolo TMS320F280xxx Series.
  - On Semi: NCP81111
- **Synchronous Rectifier**
  - On Semi: NCP4305/9
  - NXP: TEA1993/5/8

Existing PWM/FET controllers: Basically, if you have a MOSFET controller that can run on or be configured for 5V gate drive, it would be possible to use eGaN FET with it. Contact EPC for additional <u>important</u> information on other compatibility considerations to get the most out of the eGaN FET.

EFFICIENT POWER CONVERSION

Reliability

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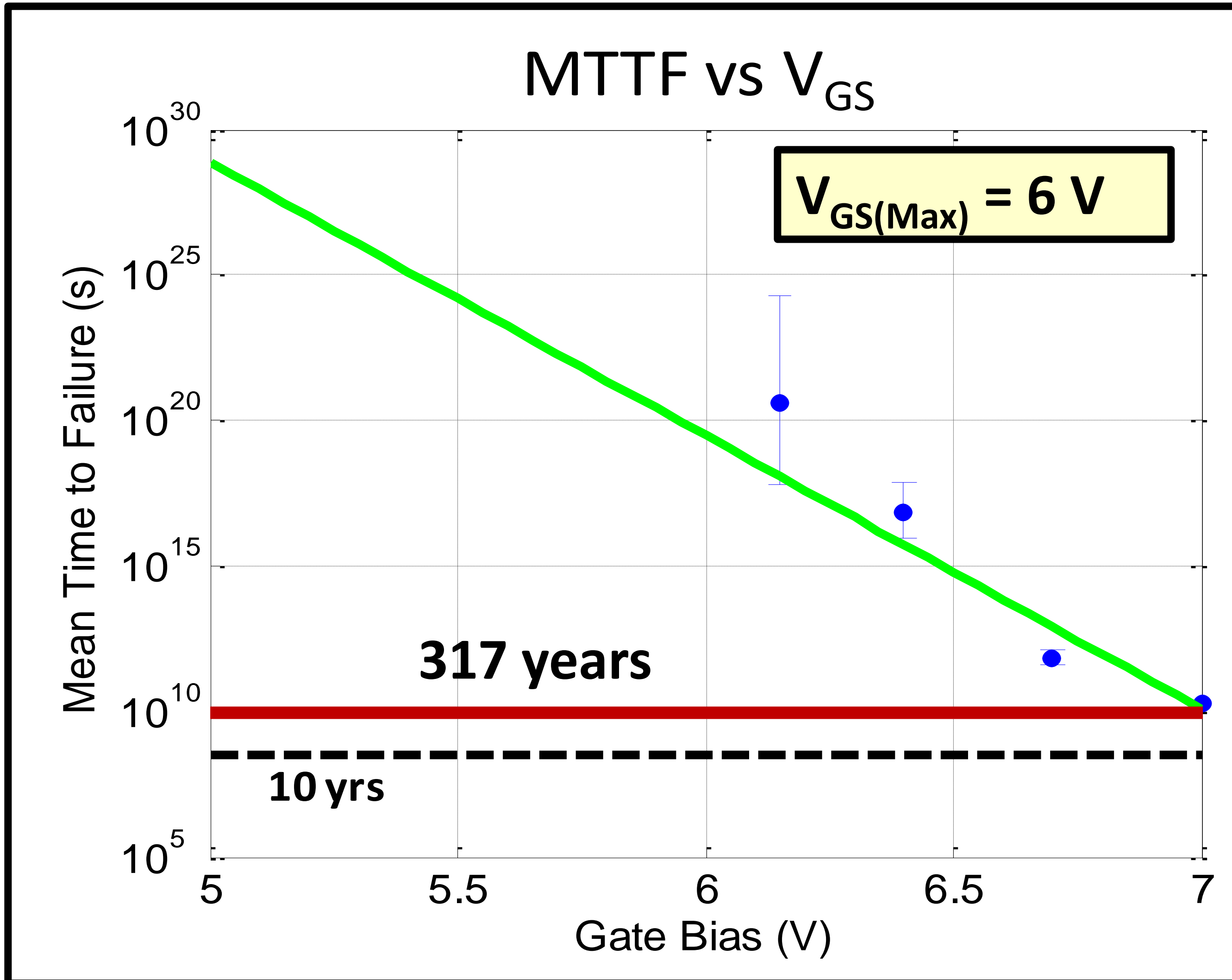
eGaN® Reliability

Gate Drive Voltage Characteristics



Unlike a MOSFET, GaN does not have gate oxide to damage and cause an instant FET gate failure.

GaN FET gate failure mechanism is off state I_{dss} leakage current goes up.

Failure = I_{dss} exceeding datasheet specification.

This graph is **NOT** giving you permission to exceed 6V Vgs Max in design.

Data is for static DC Vgs operating conditions only.

Data based on HTGB DC voltage bias test results @ 150C and projected. See EPC Phase 5 Reliability Report for more information.

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eGaN® Reliability

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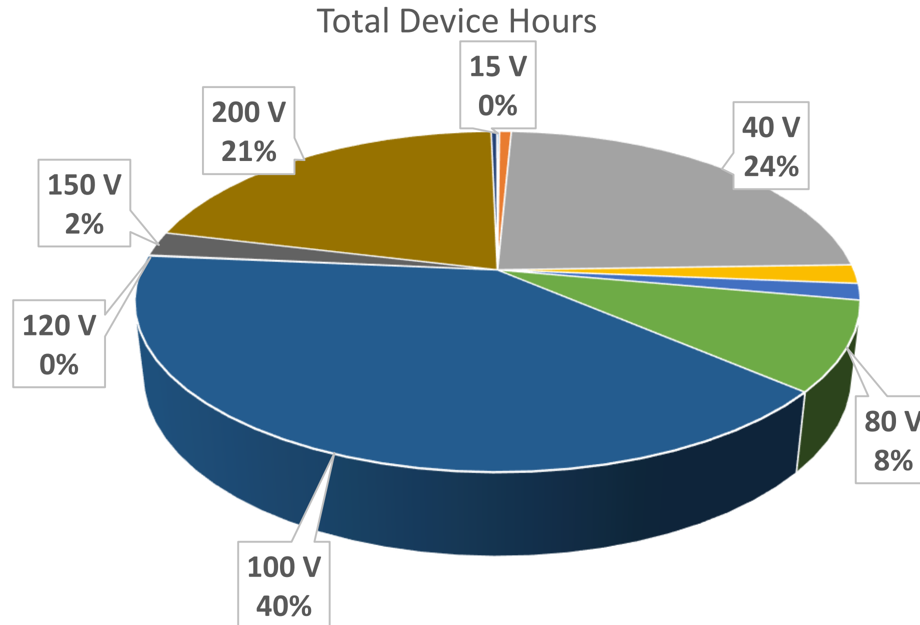

Data: July, 2016

24B total device hours in the field

259 Field Returns (42 Good, 217 Failed)

- 22 Layout Related – Addressed with Layout Section of Design Support
- 186 Assembly & Handling Related – Addressed with Assembly Web Page
- 3 Device degradation (addressed in Gen 4 and screening)

3 Device Failures in 24B Hours equals 0.17 FIT (60% confidence)

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Reliability Report Phase 9

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- **PHASE 9 SUMMARY**
  - Complete table report found in Appendix of this presentation
- Overall device reliability test hours extended to **> 9 million hours**
  - Each phase report builds on this cumulative number of stress test hours

Stress Test	Sample Quantity	Fail Quantity	Equivalent Device (hrs)	Upper Bound Failure Statistic (60% Confidence)	Notes
HTRB	2062	0	3063000	299 FIT (MTTF = 381 yrs)	$V_{DS} = 80\% V_{DS;max}$
HTGB	2079	0	3234000	283 FIT (MTTF = 402 yrs)	$V_{GS} \geq 5.5V$
TC	1380	0	1585867	NA	$\Delta T \geq 100°C$
H3TRB	708	0	708000	1294 FIT (MTTF = 88 yrs)	—
ELFR_HTRB	8366	0	401568	110 ppm	First 48 hrs
ELFR_HTGB	4833	0	231984	190 ppm	First 48 hrs
IOL	385	0	157850	NA	—
All Tests	**19813**	**0**	**9382269**		

http://epc-co.com/epc/DesignSupport/eGaNFETReliability/ReliabilityReportPhase9.aspx

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Comparing Reliability eGaN® Vs Silicon

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Technology	Part	Fully Enhanced Gate Voltage (V)	Stress Conditions	HTGB FIT Rate (#/billion hours)
eGaN FET	EPC2016	5	150 °C 5V	<< 1
Silicon n-MOSFET	IRF6795M	10	150 °C 10V	7 [Ref 1]
SiC n-MOSFET	CPM2-1200-0025B	20	150 °C 20V	100 [Ref 2]
Technology	**Part**	**Maximum Drain Voltage (V)**	**Stress Conditions**	**HTRB FIT Rate (#/billion hours)**
eGaN FET	EPC2016	100	150 °C 100V	<< 1
Silicon n-MOSFET	A03160	600	150 °C 480V	20 [Ref 3]
SiC n-MOSFET	CPM2-1200-0025B	1200	150 °C 800V	25 [Ref 2]

[1] International Rectifier, “Low Voltage MOSFETS”, http://www.digitimes.com.tw/tw/b2b/seminar/service/download/051a005110/2ir.pdf

[2] Alejandro Esquivel, “How can Motor Drive benefit from Silicon Carbide Products”, http://www.arroweurope.com/nc/it/servizi/download-center.html?tx_abdownloads_pi1%5Baction%5D=getviewclickeddownload&tx_abdownloads_pi1%5Buid%5D=1522&tx_abdownloads_pi1%5Bcid%5D=9774

[3] Alpha & Omega Semiconductor, “AOS Semiconductor Reliability Report”,www.aosmd.com/res/reliability_reports/AO3160.pdf

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About the Author

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Mark Gurries is a FAE at Efficient Power Conversion (EPC) corporation covering the US west coast. He is based in Silicon Valley helping customers integrate eGaN into their products.   Mark's has over 30 years of work experience which includes 5 years at Apple as a Senior Analog Design Engineer designing PowerBook™ notebook power supply systems and 15 years at Linear Technology as a Senior Applications Engineer and a Group Leader working on DC-DC, power management controllers and rechargeable battery systems.

The end of the road for silicon…..

is the beginning of the eGaN FET journey!