EDI CON 2018
Electronic Design Innovation Conference & Exhibition
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Santa Clara Convention Center
Santa Clara, CA

EM Verification Within a Custom IC Design Platform

Method-of-Moments EM for Silicon Design

Dr. John Dunn Electromagnetic Technologist

AWR Group, NI

Agenda

- Part 1: AXIEM simulator works in Virtuoso RF
  - Who is NI, AWR Group?
  - What is AXIEM software?
- Part II: Why AXIEM software for silicon?
  - Full-wave, planar EM simulator
  - Efficient mesh and solve engines
  - Used for distributed structures such as spiral inductors
- Part III: Important issues when using AXIEM simulator
  - Ports and grounds
  - Meshing and Q
  - How the Simulator Solves
- Conclusions

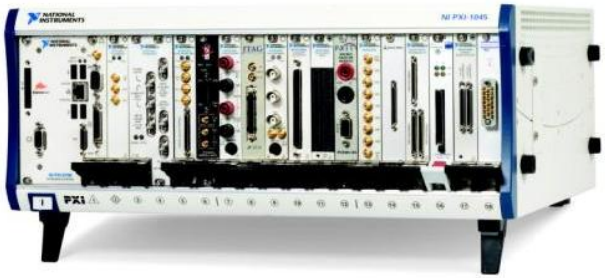
National Instruments

Markets Served Lab & production test systems & control systems

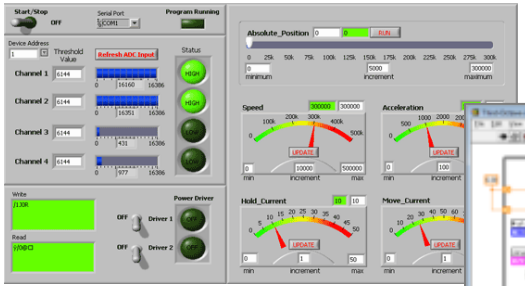
Annual Revenue >$1.3 billion

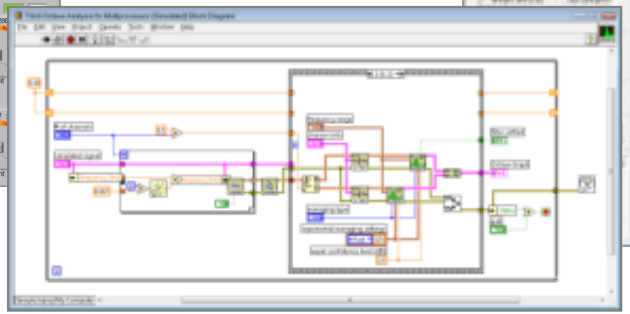
Global Operations > 7,000 employees

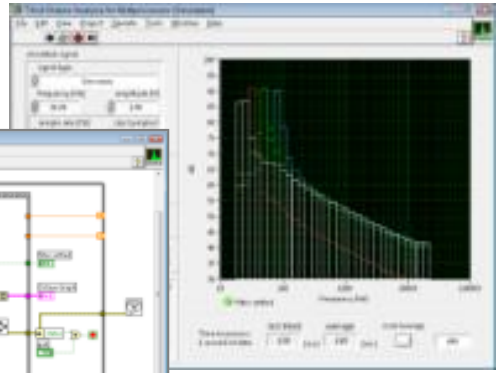
Largest Segment Semiconductor



NATIONAL INSTRUMENTS LabVIEW







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National Instruments Role in Semiconductor & Module Design Flow

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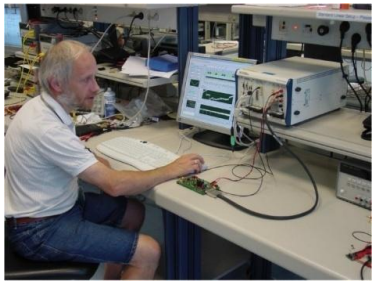
NI playing a bigger role in the semiconductor market

- Many companies using NI in lab characterization
- RF design tools, SDR wireless prototyping
- STS semiconductor production test platform

Design & Prototyping

- Chip
- Module
- System

Lab Characterization



LabVIEW + PXI

Production Test

STS – Semiconductor Test System

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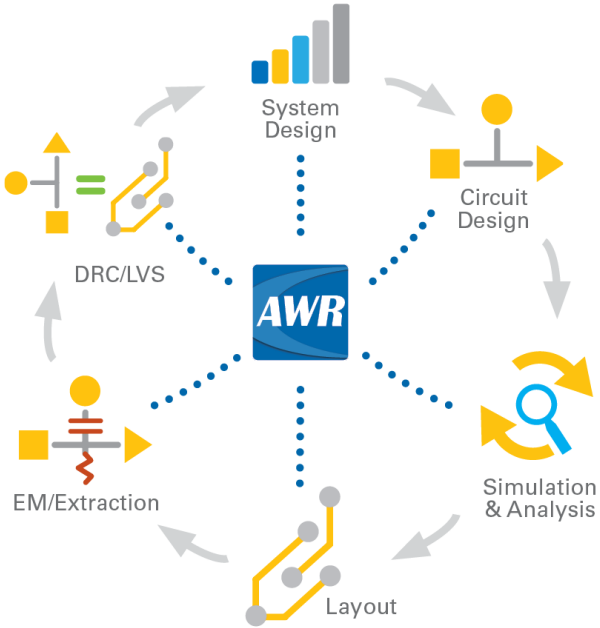
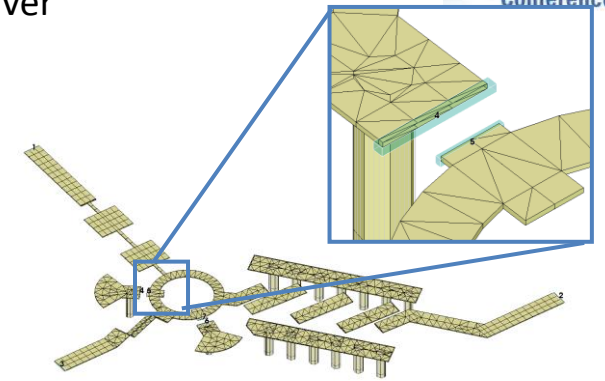
AWR Products

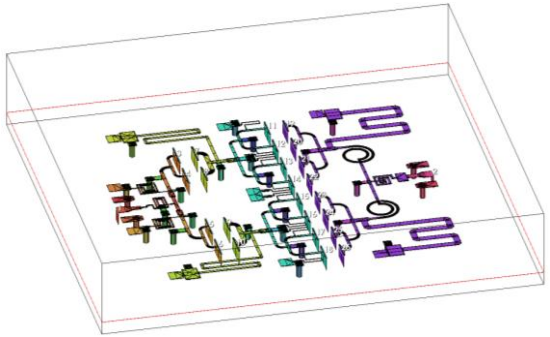


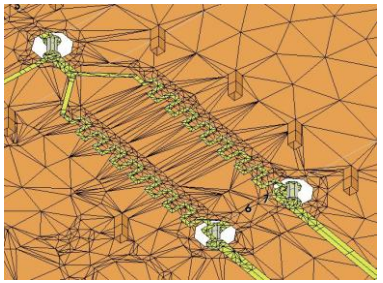
A unified system, chip, board, and module high-frequency design platform

AXIEM EM Simulator

- Gridless, method-of-moments, open boundary 3D planar solver
  - Solves for currents on horizontal metal and vertical vias
  - Planar, dielectric layers
  - **Sounds like a silicon chip! … or a board! … or a package!**
- Generates S-parameters
- Flexible port options
  - Ground references – many options
  - Placement of port – interior or edge
- Mesh
  - Surface of metal meshed
  - Thick or thin metal
- Shape simplification rules
  - Merges vias and simplifies currents
- High capacity / speed solve
  - Iterative multipole – O(NlogN)

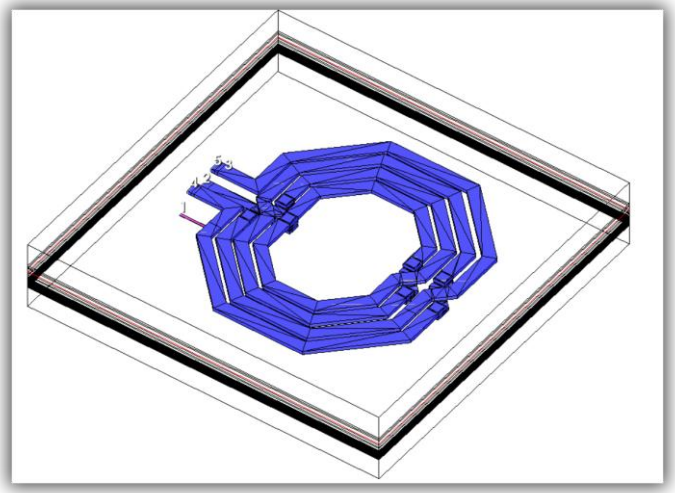




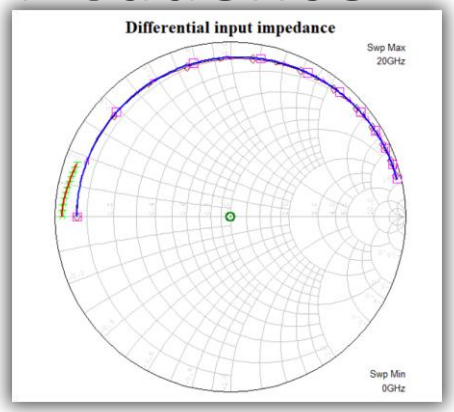


Traditional AXIEM Flow in Microwave Office Software for Cadence

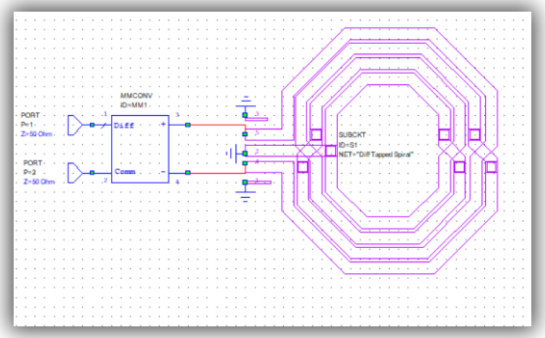
1. Import layout from Virtuoso



2. Set up ports and simulation settings



3. Generate S-parameters



4. Put in circuit simulator

Simulator options

- Export to Cadence
- Import Spectre netlist-run Microwave Office APLAC engine

New Flow in Virtuoso – Golden Schematic Flow (IC Layout)

Design Optimization and Layout Verification via Single Schematic

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Golden Schematic

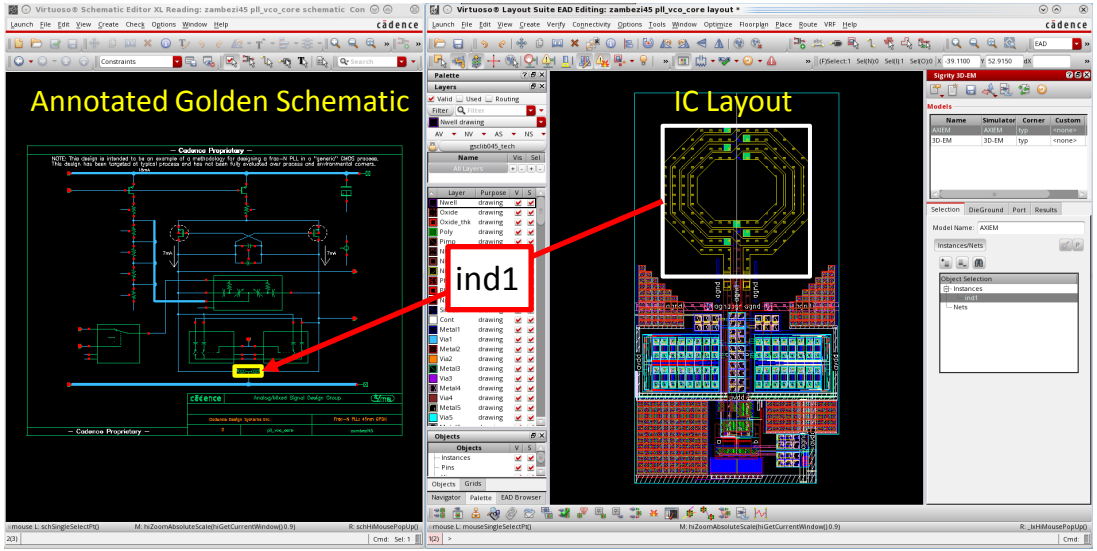
Design Tradeoffs, Optimization

Design Review, Signoff

Layout Generation

Design Verification

Manufacturing



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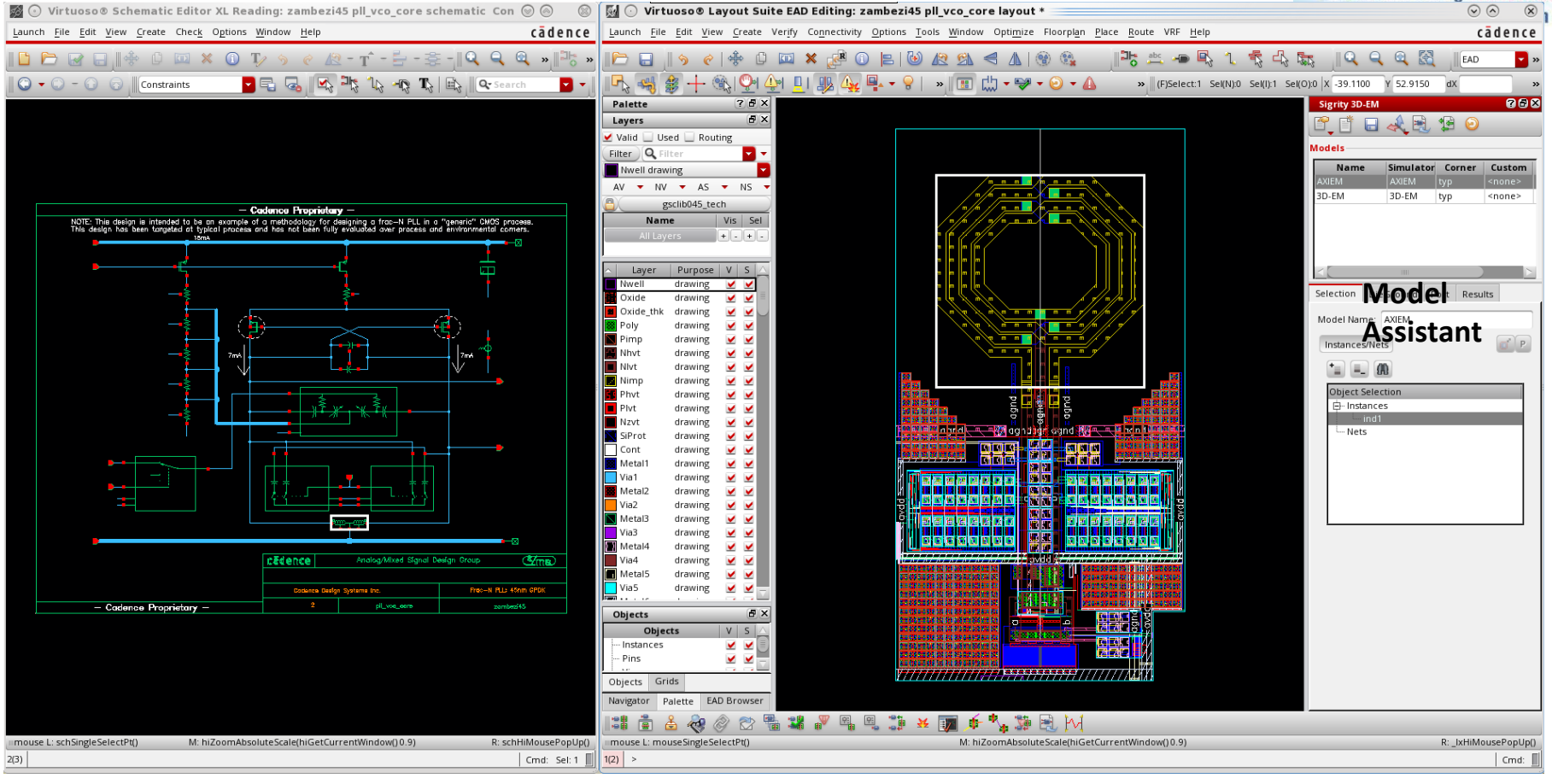
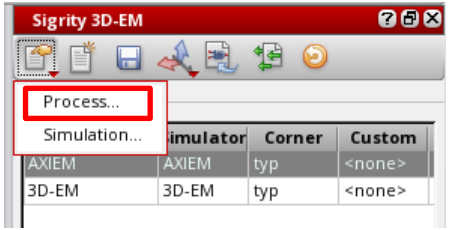
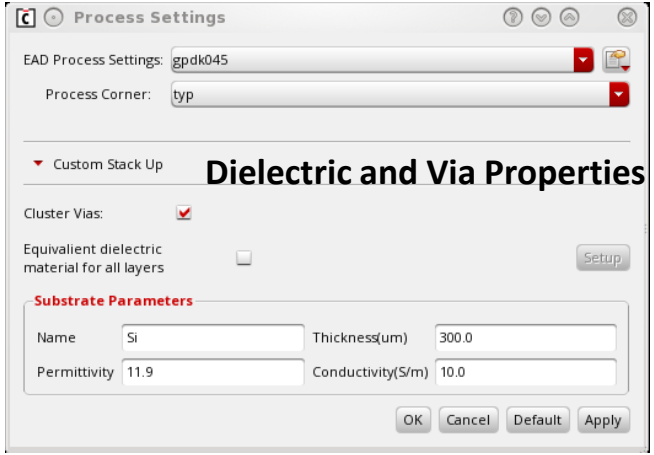
Axiem Model in Virtuoso RF

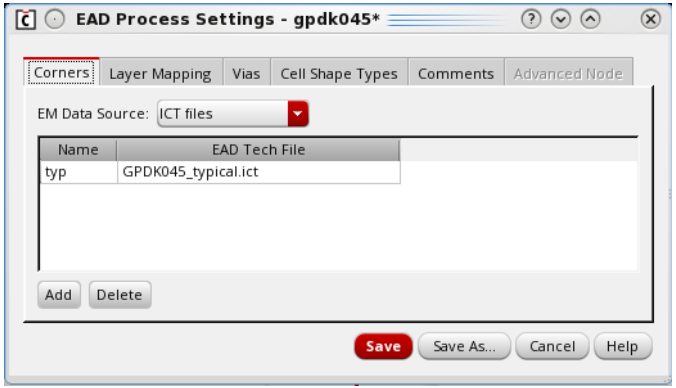


Process Setup: PDK ict/qrcTechFiles



All setup is in Virtuoso Model Assistant





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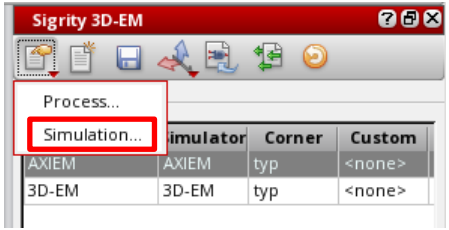
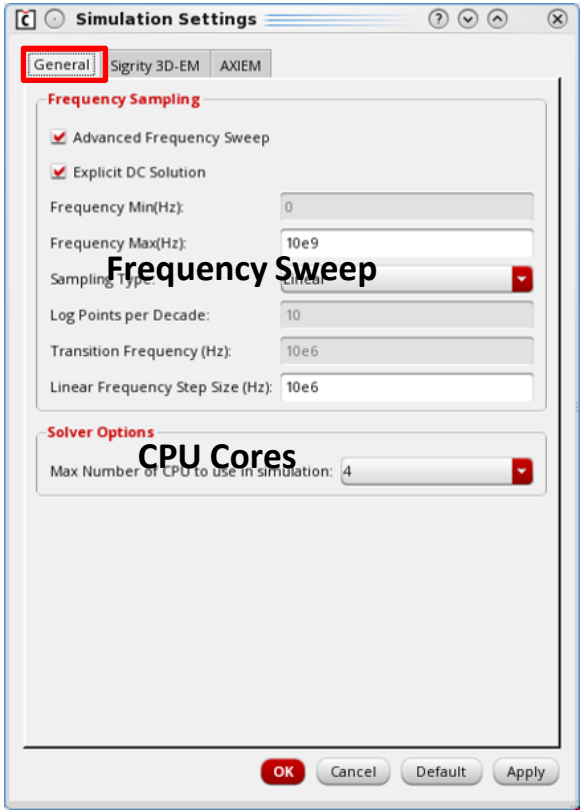
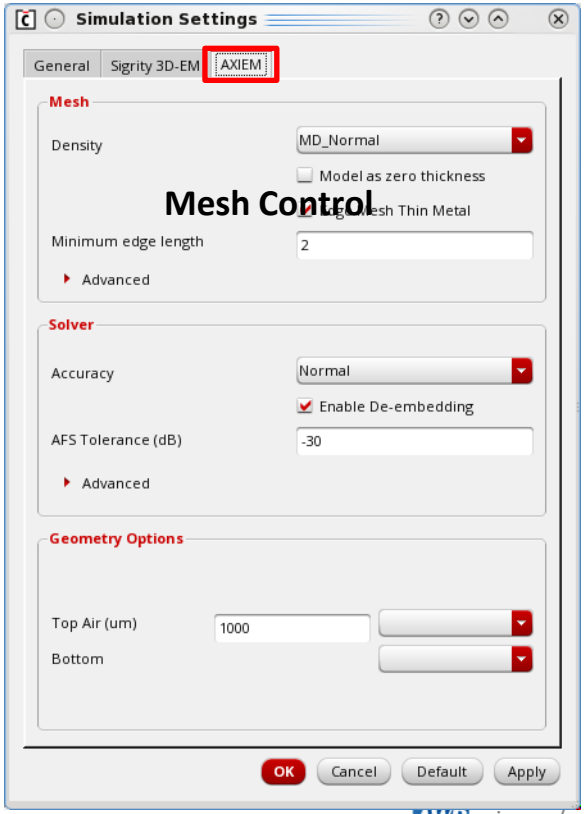
Simulation Settings

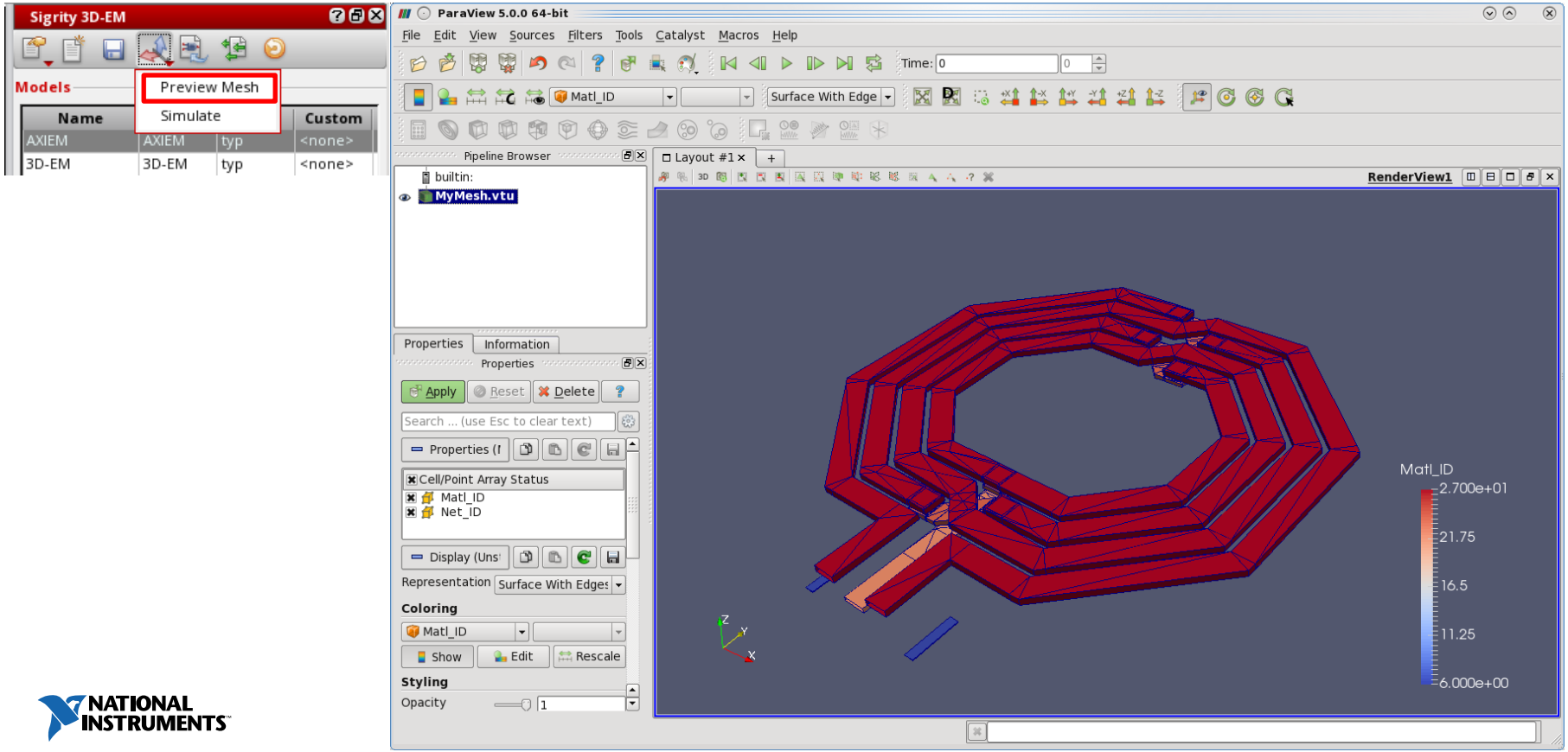


AXIEM simulator is running in the background





Preview Mesh



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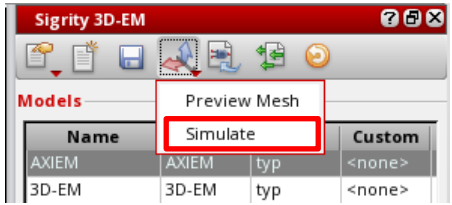
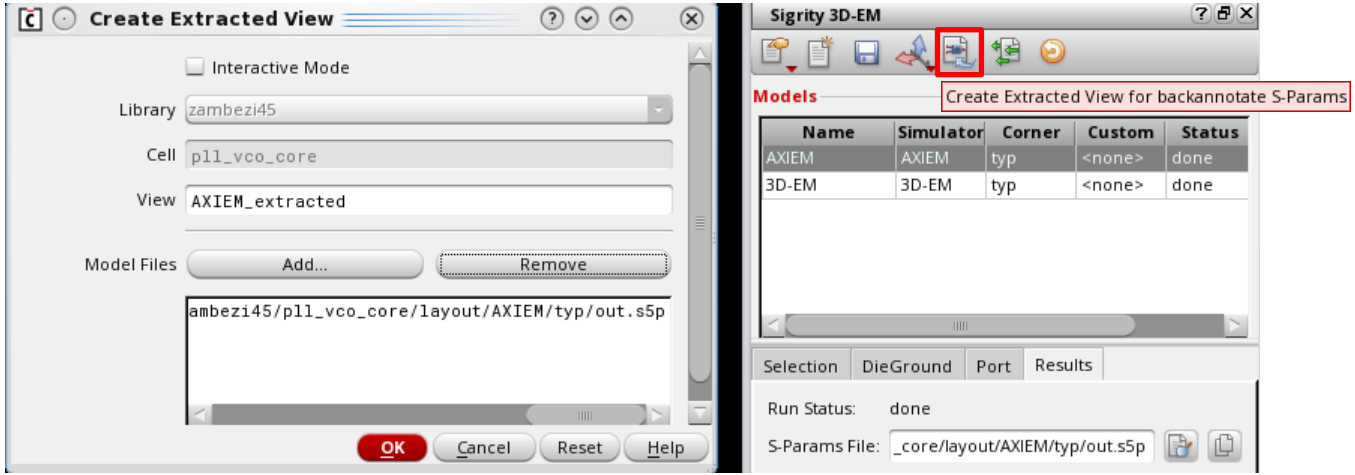
Extract S-Parameters With AXIEM Simulator



axiem model.xml

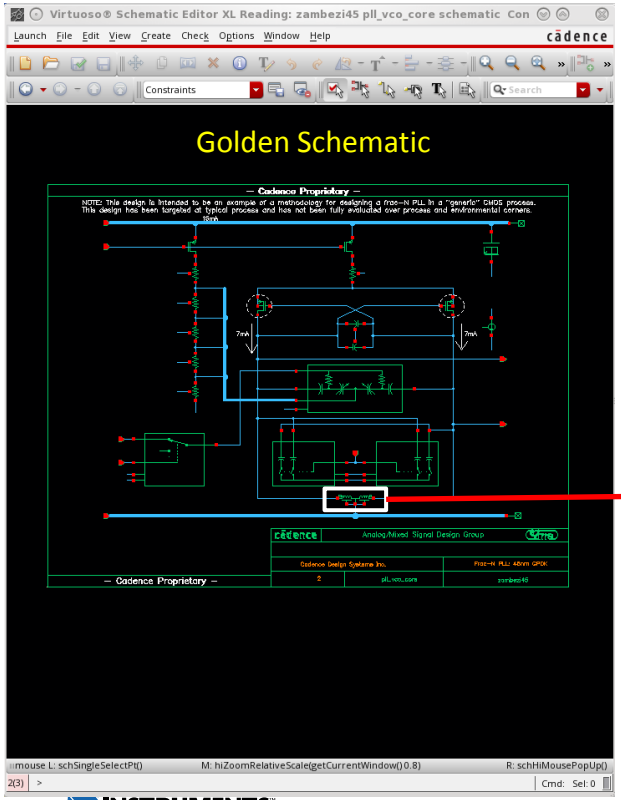
```
Input file: model.xml

-------------------------------------------------------------------------------------------------------------------------

 Simulating model1 using Advanced Frequency Sweep  (64-bit Linux : V14.0.9089) - Reserve 8 Threads

              Meshing Geometry - Elapsed time ( 00:00:0.47 )
                      Mesh Freq = 10 GHz
                      # of Facets = 1118
                      # of Unknowns = 1869
                      # of Nets = 3
                      # of Ports = 5
   --- Calculating DC solution
              ----- Candidate Solver Type : Direct (low frequency)
              ----- Calculating Greens Functions -----
              ----- Matrix Setup -----
                      - Elapsed time ( 00:00:14.27 )
              ----- Matrix Solve -----
                      - Elapsed time ( 00:00:0.01 )
              ----- Simulating DeEmbedding Standards -----
                      Port 1, 2, 3, 4, 5: not de-embedded
                      - Elapsed time ( 00:00:0.00 )
   --- Solution @ DC - Elapsed time ( 00:00:14.29 )
   --- Calculating Solution @ 10 GHz
              ----- Candidate Solver Type : Direct (high frequency)
              ----- Calculating Greens Functions -----
              ----- Matrix Setup -----
                      - Elapsed time ( 00:00:11.28 )
              ----- Matrix Solve -----
                      - Elapsed time ( 00:00:0.01 )
              ----- Simulating DeEmbedding Standards -----
                      Port 1, 2, 3, 4, 5: not de-embedded
                      - Elapsed time ( 00:00:0.00 )
   --- Solution @ 10 GHz - Elapsed time ( 00:00:11.31 )
   --- Solution @ 0 Hz was calculated in a previous simulation
   --- Solution @ 10 GHz was calculated in a previous simulation
   --- Calculating Solution @ 5 GHz
              ----- Candidate Solver Type : Direct (low frequency)
              ----- Calculating Greens Functions -----
```

Extracted View Creation

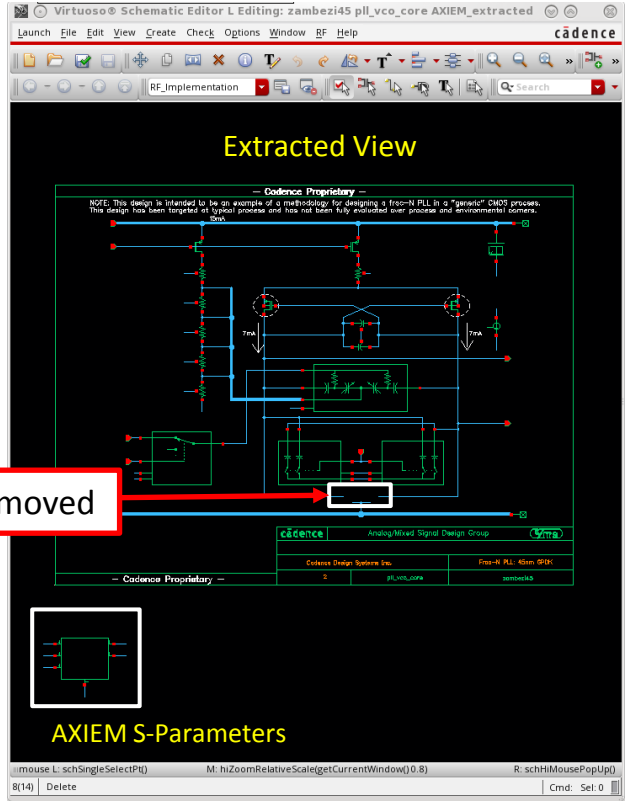


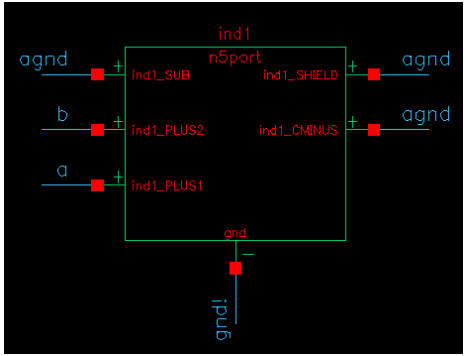
- Replaces model in schematic with S-parameters
- Layout remains – so don't break LVS,…

Extracted View Creation

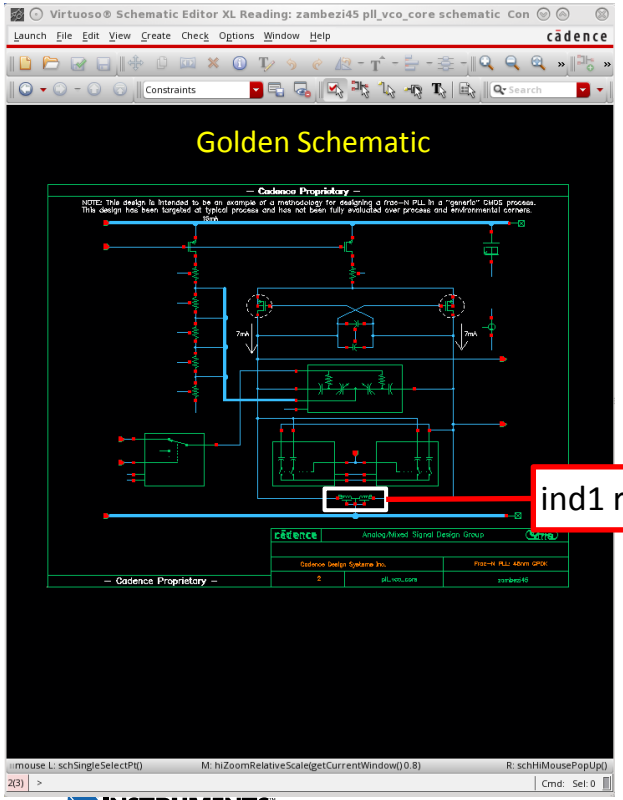


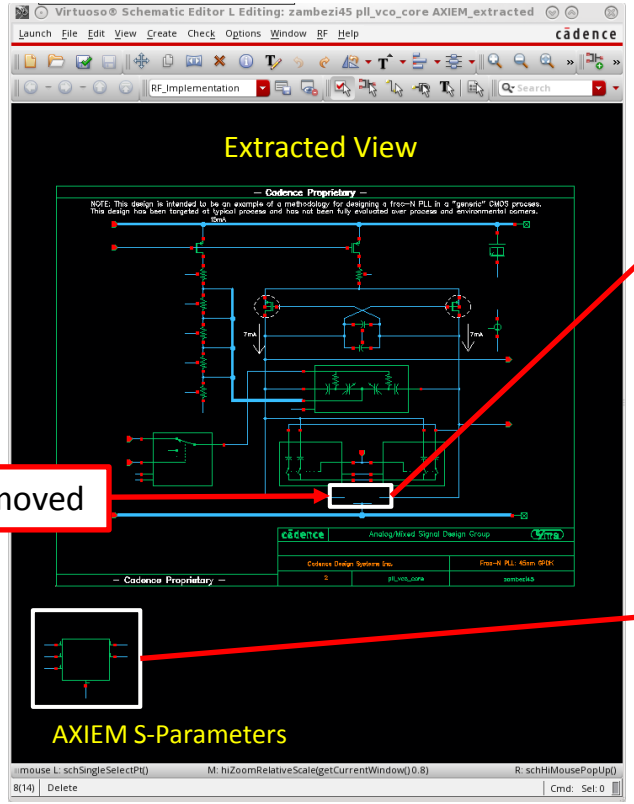
ind1 removed



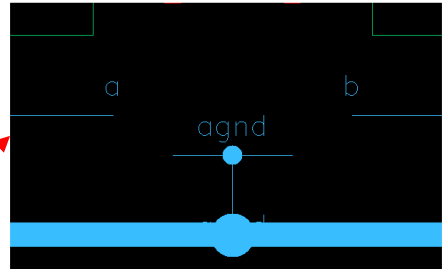


Extracted View Creation

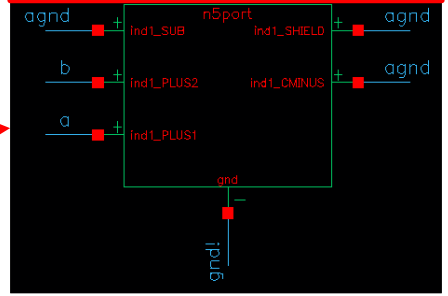




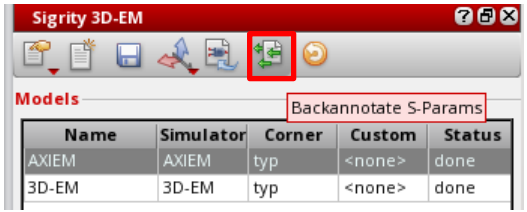
ind1 removed

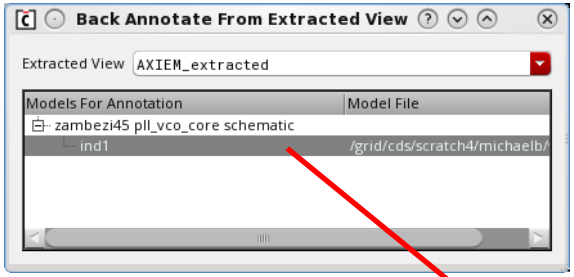


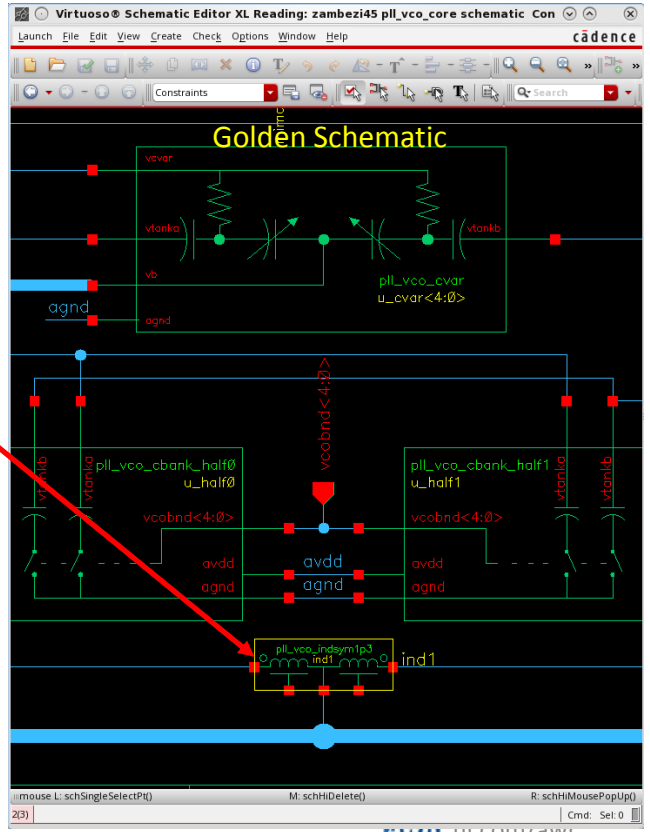
Connectivity automatically maintained with wire stubs



Back Annotation: S-Parameters in Extracted View







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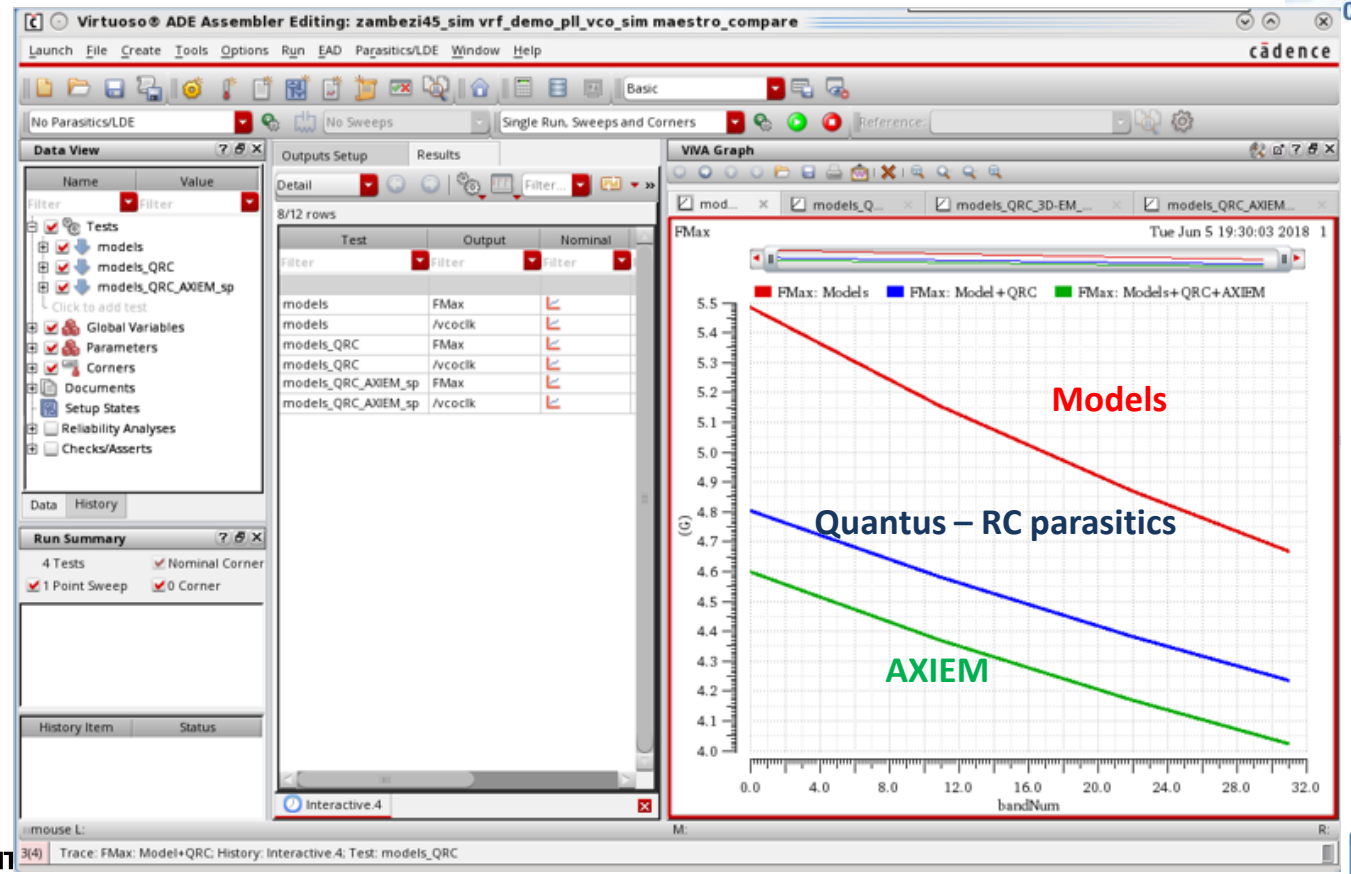
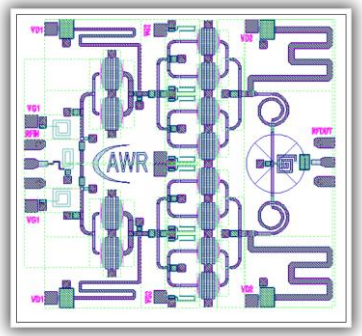
VCO Results

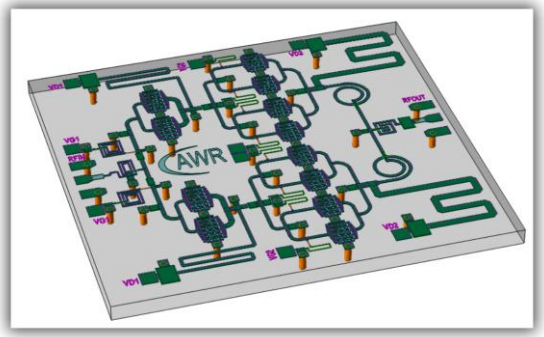


Why EM Simulation for Analog Silicon?

- Traditional analog flow - silicon
  - Device models – field-effect transistors (FETs), …
  - Nets treated as parasitics – modeled as “lumped” elements
    - Traditionally an RC extraction
    - More recently, inductance included – higher frequencies
- Traditional III-V flow – gallium arsenide (GaAs), gallium nitride (GaN)
  - Nets are included as distributed line models
  - EM simulation is used for: checking models, coupling between elements, no model



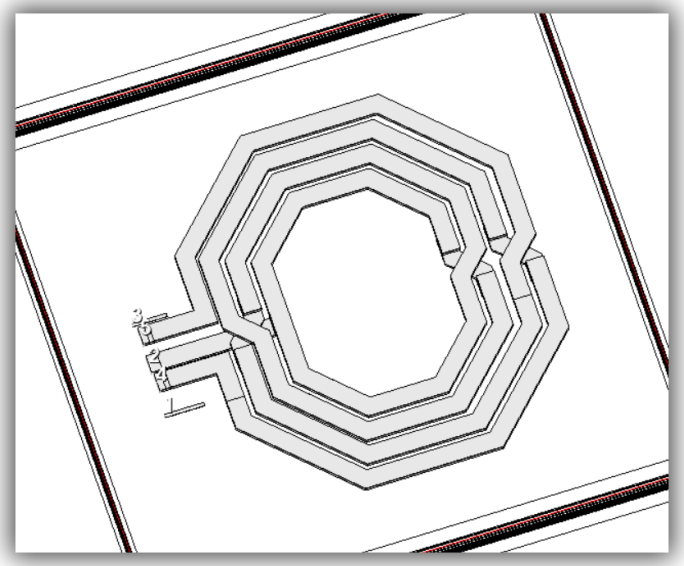
GaAs power amplifier chip

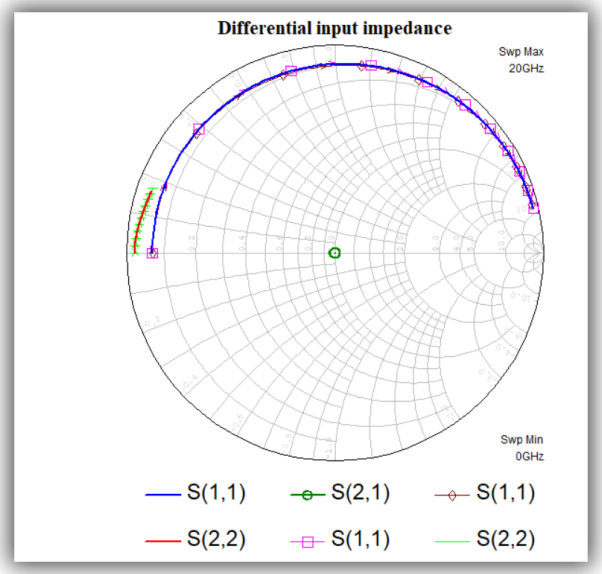


Places Where EM Simulation is Useful for Silicon

- EM simulation in silicon
  - Distributed structures – inductors
  - Coupling between elements – multiple inductors, pads, bond wires, …
  - No model – ground meshes, ground issues, frequency dependent loss
- Effects become more important with higher frequency
  - Electrical length is longer
  - Coupling more likely
  - Imperfect ground more of an issue
  - Skin depth in metal – loss is changing
    - For instance, skin depth of Al at 1 GHZ is ~ 2 microns
- … And of course – getting on and off the chip!
  - Modules and board transitions
  - Bondwires, ball-grid arrays (BGAs), and more

The Spiral … Classic Example



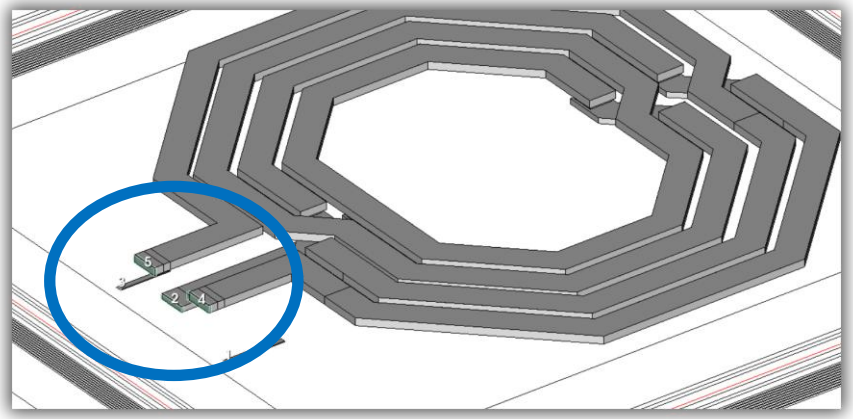


RF Concepts

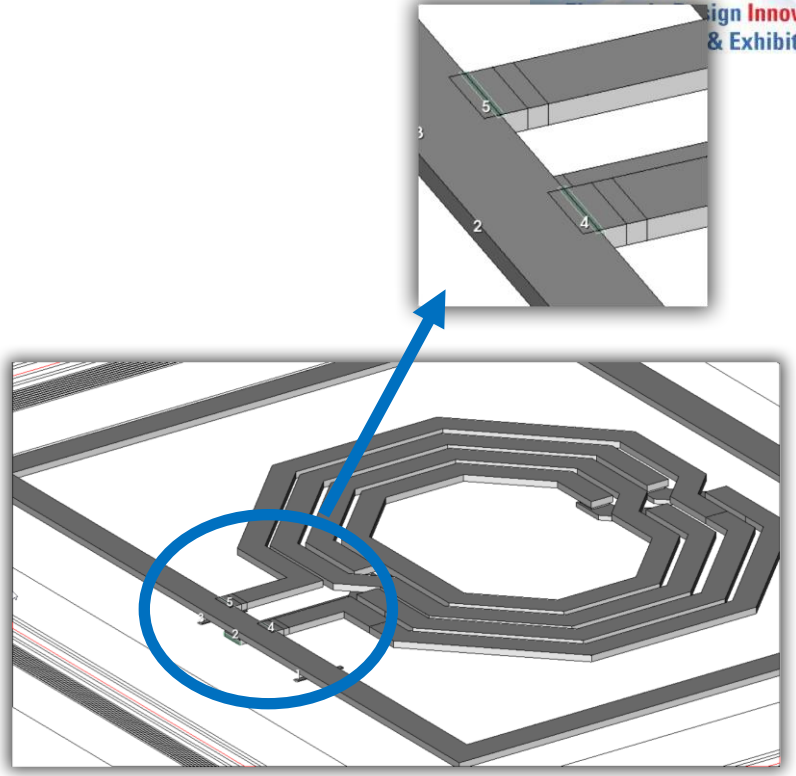
- Smith chart
- Port impedance
- Differential ports

Issues When Using EM Simulators - Ground

- Ground is important for S-parameter definitions
  - Ports need a port ground definition
  - Where current comes from
  - Gives port voltage reference
- RF Concepts: S-parameter

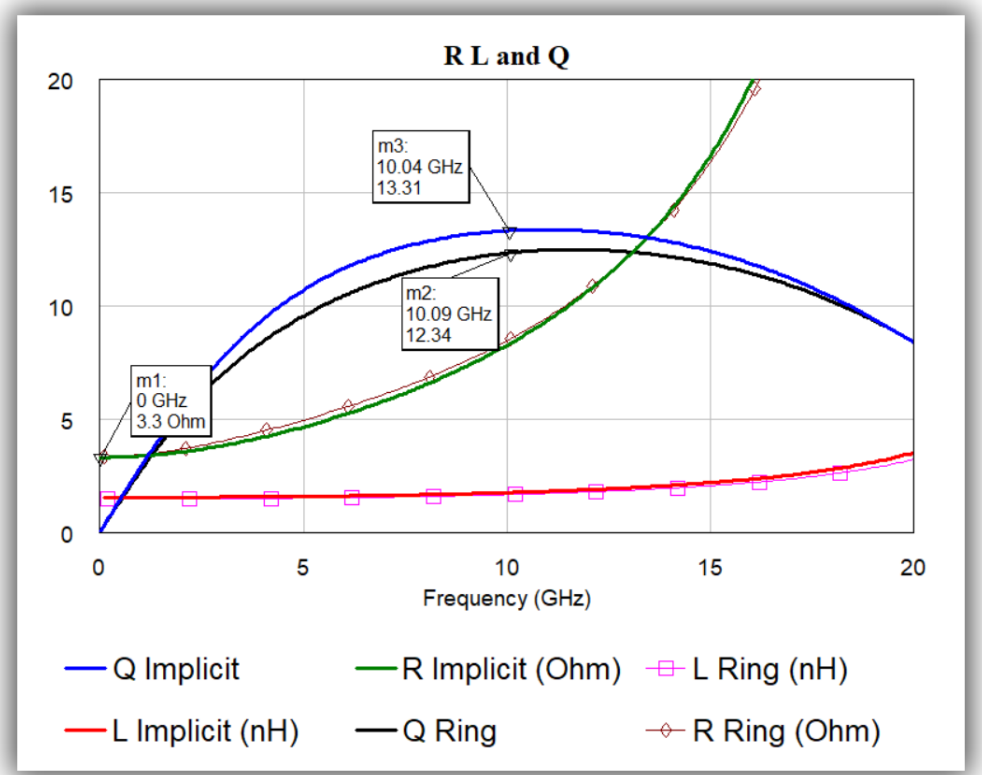


Implicit grounded port



Series port and ground ring

Grounding Results and Q

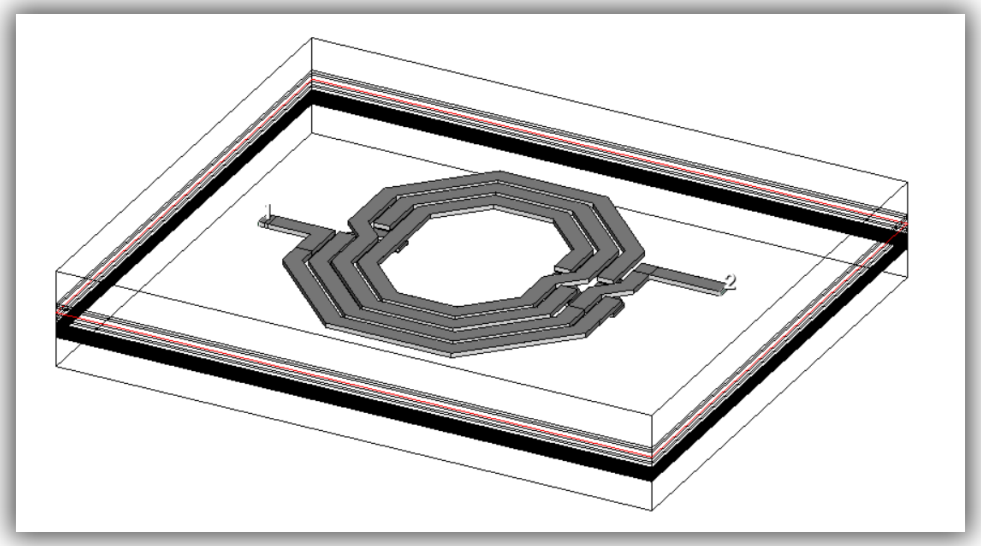


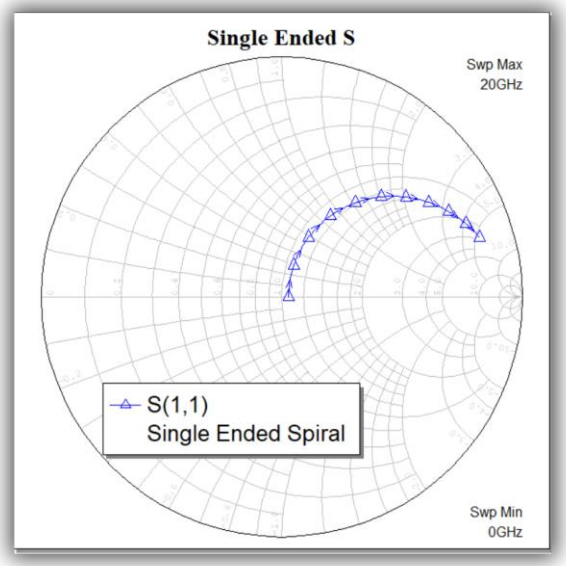
Biggest difference is in the Q calculation, about 6%

RF Concept: Q

- Common figure of merit
- Notoriously hard to calculate
- Stored energy/loss
- Extremely sensitive to R
- Substrate loss usually dominates
- Different definitions of Q
- Grounding / return current matters
- Inductance is loop inductance

A More Single-Ended Example

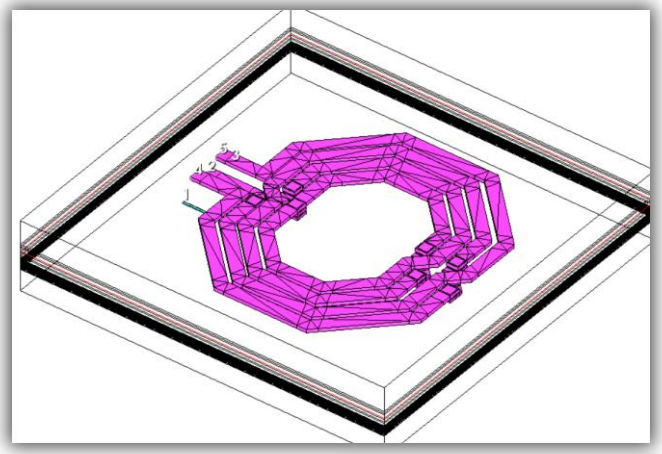


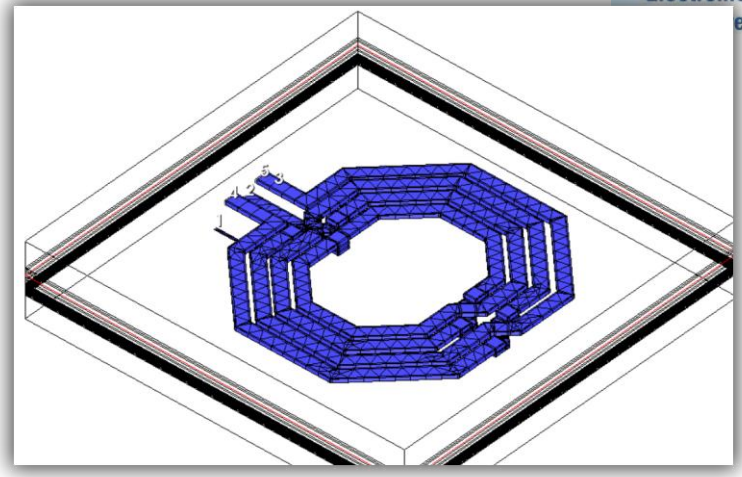


Ports are farther apart
Ground is at infinity

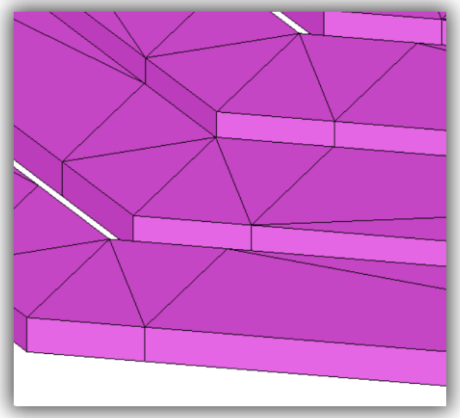
Looks like an R L load – Port 2 is a 50-ohm load

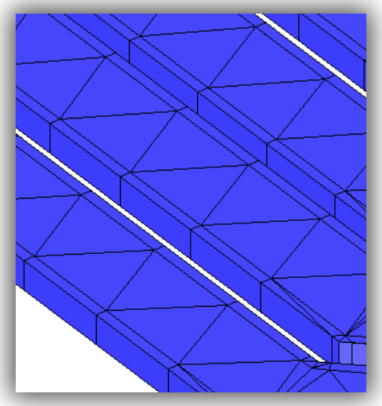
Issues When Using EM Simulators - Mesh





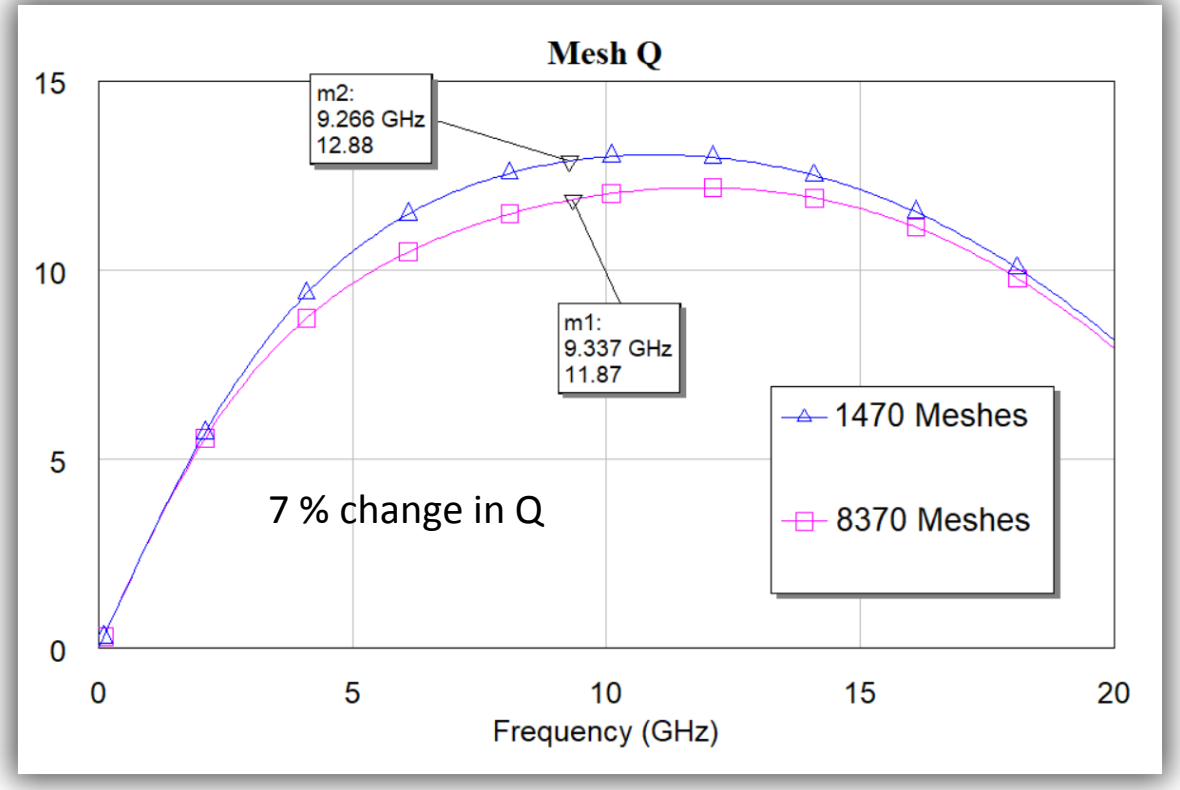
1840 Unknowns





8800 Unknowns

Q Meshing - Results



Conclusions

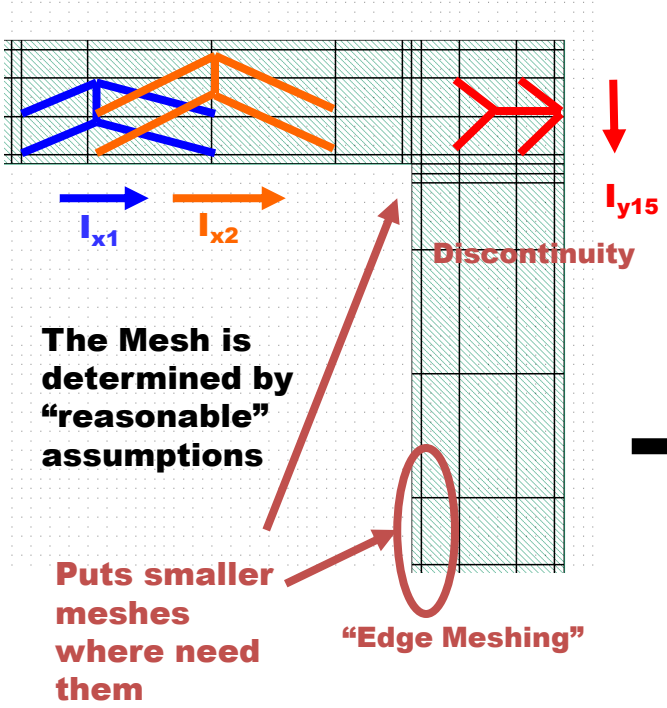
- AXIEM best-in-class planar 3D EM simulator
  - Planar dielectrics, metal and vias – like silicon!
  - Integrated into Virtuoso
- EM simulators can be useful in silicon when:
  - Distributed effects matter - inductors
  - Frequency-dependent effects matter – resistance
  - Grounding issues – ground meshes, rings
  - Coupling effects
- EM simulator results depend on:
  - Grounding definitions of ports
  - Meshing

Appendix

AXIEM simulator and fast solvers

Meshing the Circuit

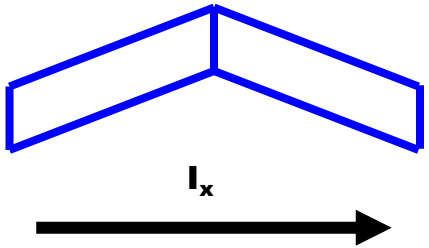
- Can mesh thick or thin metal
- Usually thick metal is used on chip



The mesh should capture the "look and feel" of the current:

- Continuous
- Differentiable - dI/dx = - jwQ
- Both X and Y directions
- Z direction for vias

"Rooftop" Basis Function



- **Varies linearly in x**
- **Constant in y**

Making the Matrix

The Completed Matrix Equation

$$\begin{bmatrix} 0 \\ 0 \\ . \\ . \\ . \\ 1 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} A_{1,1} & A_{1,2} & \dots & A_{1,100} \\ A_{2,1} & A_{2,2} & & . \\ . & & & . \\ . & & & . \\ . & & & \\ & & A_{15,12} & \end{bmatrix} \begin{bmatrix} I_{x1} \\ I_{x2} \\ . \\ . \\ . \\ I_{y1} \\ \\ I_{y2} \end{bmatrix}$$

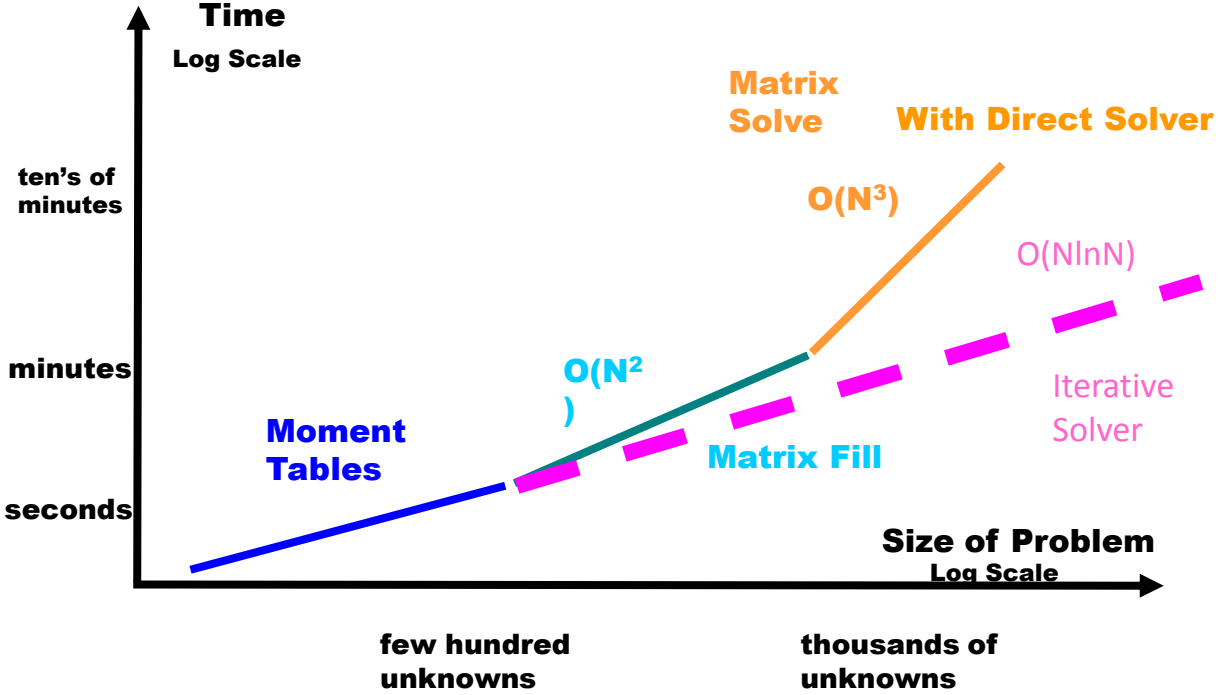
Coupling between rooftops 15 and 12.

Only the cells on the impressed voltage gap give a non-zero contribution

Theoretical Time to Solve the Problem

Typical Problem Sizes

<1K – Very Small
1 – 10K – Seconds
10K ~ 30 seconds
10K – 100K minutes
100K – 500K minutes
>500K – very large



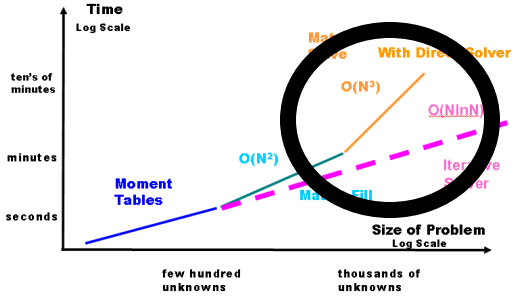
The Matrix Solve – The Old Days

The matrix is NXN for N unknown currents.

-It is dense. … i.e. … all elements are non-zero.

- To fill the matrix takes $O(N^2)$ time.

- To solve the matrix directly … takes $O(N^3)$ time … using Gauss's law.



Mr. Carl Gauss

Iterative Solvers – can work faster than $O(N^3)$.

They can be as fast as O(NlnN).

Details to follow…

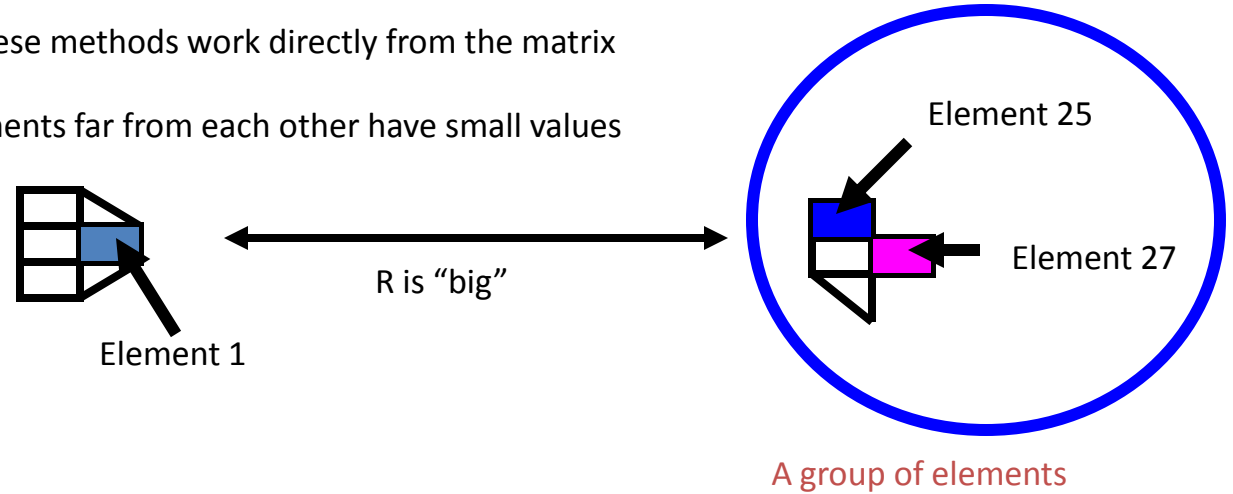
Fast Solvers

Matrix compression methods

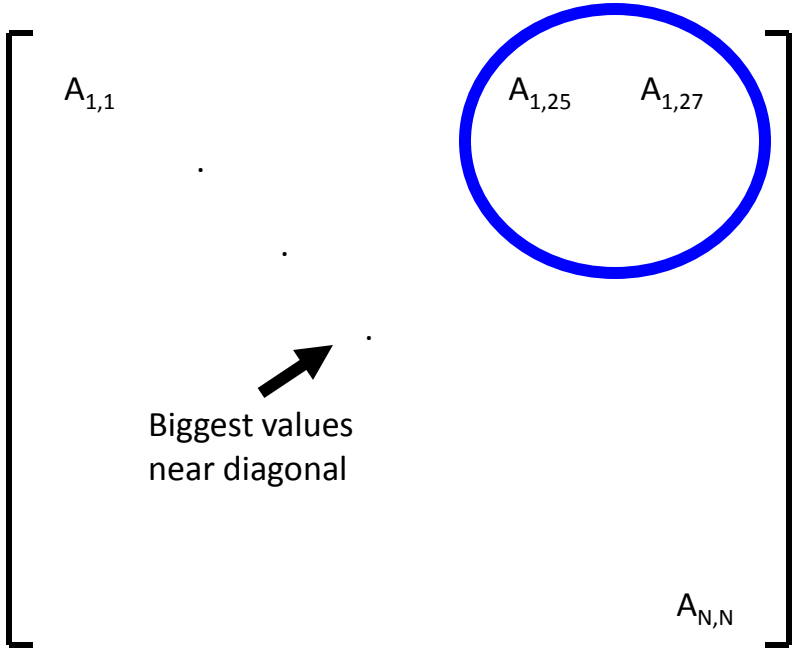
- White et al – 1994 – precorrected FFT method
- Kapur et al – 1997 – IES^3
- Jandhyala – 2005 - PILOT

These methods work directly from the matrix

Elements far from each other have small values

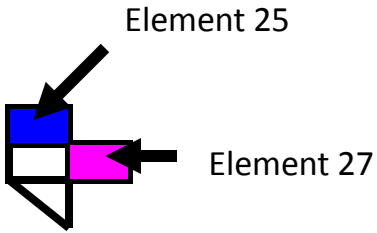


Simplify the Matrix



These values are:

- Small
- All about the same – as all cells in same group.



Note: It is important to number the cells so that close cells have close numbers. Often a renumbering step must be carried out.

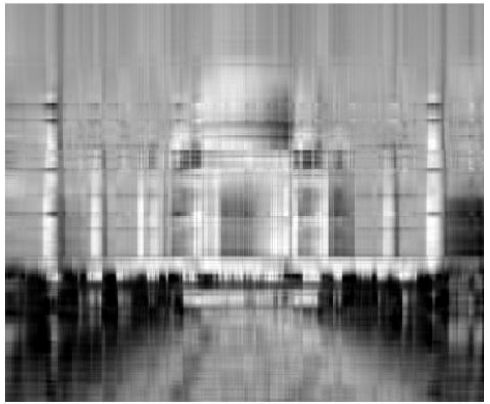
A Smaller Matrix

If the elements of A are about the same … we only need a few terms.

Image Compression

Original Image

572 X 572



k = 8

8*2*572

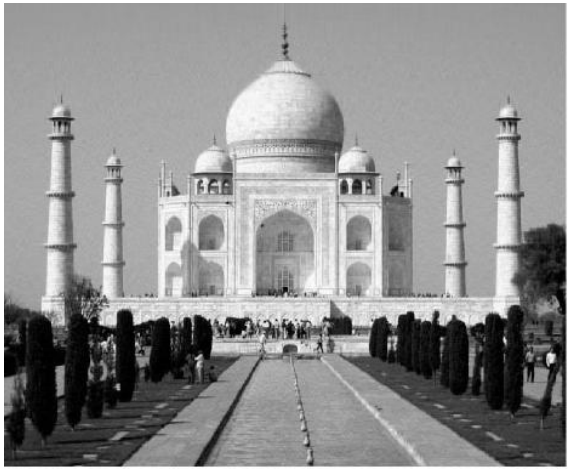
2.8 % of original data

A Smaller Matrix - 2

k = 64

64*2*572

11.1 % of original data



k = 128

128*2*572

22.2 % of original data

Condition Number of a Matrix

- Moment method matrices are dense
  - Can't throw out any elements that are bigger than 1/condition number
  - Example – condition number = 1e6 … Can't throw out an element 1e-6 big … assuming largest element is 1
  - For an iterative solver – number of iterations ~ condition number

$$\begin{bmatrix} 1 & & .0014 \\ & 0.5 & \\ 1e\text{-}6 & & 1.5 \end{bmatrix}$$

Can't set to 0

Bad things are going on …

- Must have high accuracy-math
- Can't use any approximations
- Eventually – just won't solve

When is the condition number bad?