

Advances in Recent PCB Design Verification flows

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Design and Verification Flows



- Design Flow: EM is used while making the circuit.
 - Checking a model's accuracy: a wide output line on a power amplifier
 - A model doesn't exist: an octagonal spiral inductor
 - Coupling between parts of the circuit: lines coupling to a distributed filter
 - The completed circuit is sent out to external tools for manufacturing and other layout
 - Microwave Office software has nice technology for this flow: extraction, parameterbased layout, shape simplification rules, PDK cells, hierarchical layout
- Verification Flow: A layout is brought into Microwave Office software to simulate in EM
 - Checking a completed layout to see if any signal integrity issues: sufficient grounding or radiation
 - The finished layout might be very complicated: multiple power planes, traces
 - The AXIEM EM simulator, is set up: port type and location
 - The layout is meshed and simulated





EM Verification Flow Requirements

- Must work well for commercially complicated board topologies
 - Hundreds of nets
 - Multiple power planes connected by many vias
 - Dozens of surface-mount parts
- Must work with commercial layout tools
 - Cadence Allegro, Zuken, Mentor Graphics, Altium
- Should have knowledge of board stackup and material properties
- Ability to select nets and surrounding layout easily
- Ability to simplify layout as needed to get reasonable mesh
- Ability to easily have ports added







Recent Advances in EM Verification Flows

- ODB++ and IPC-2581 layout languages based (had some of this V13)
 - Supported by all commercial tools.
 - Have a lot information besides the layout: nets, materials, and board stackup
- Imports directly into Microwave Office software (in V13 had to go through a third-party tool)
- Controlled with the PCB import wizard
 - Tabular display and control of nets, layers, and materials
 - STACKUP block is automatically created for EM simulation
- Nets can be identified easily and layout simplified as needed
- Ports (point ports) are automatically added at selected component pins
- Net selection understands surface mount part gaps, and more complicated multiple connected parts
- S-parameter block in schematic has layout-like symbol and appropriate net names



An Example – A Board Made in Zuken

Imported board

- Imported as IPC 2581
- 11 layer FR4 board
- 10 conducting layers
- 14 via types

Close-up 3D view of vias

The Import Wizard

options Layers Nets Stackup		
Options		
Import Format	IPC-2581	\sim
Filename	3DI	
Merge paths	IPC-2581	
	ODB++ (file)	
	ODB++ (dir)	

Select import format

PCB Import - Layers (Showing 83 of 83) Options Layers Nets Stackup ✓ Import Name Type ✓ Negative \checkmark Conductor-1 SIGNAL \checkmark Conductor-2 SIGNAL \checkmark Conductor-3 SIGNAL \checkmark Conductor-4 SIGNAL \checkmark Conductor-5 MIXED \checkmark Conductor-6 MIXED \checkmark Conductor-7 SIGNAL \checkmark Conductor-8 SIGNAL \checkmark Conductor-9 SIGNAL \checkmark Conductor-10 SIGNAL SILKSCREEN Symbol-A Resist-A SOLDERMASK MetalMask-A SOLDERPASTE \square HeightLimit-A GRAPHIC CompArea-A GRAPHIC

Layers imported

PC	B Import - Stackup	(Showing	g 21 of 21)					
C	ptions Layers Ne	ts Stad	kup					
	Layer Name Materia		Thickness (mm)	Conductivity (S/m)	Dielectric Constant	Loss Tar		
	Conductor-1	COPPER	0.02	5.969e+07	1	0		
	Resist-A	mat1	0.02	0	4.5	0.02		
	InsulateLayer 1-2	ABF	0.075	0	4.5	0.02		
	Conductor-2	COPPER	0.02	5.969e+07	1	0		
	InsulateLayer2-3	ABF	0.075	0	4.5	0.02		
	Conductor-3	COPPER	0.02	5.969e+07	1	0		
	InsulateLayer3-4	ABF	0.075	0	4.5	0.02		
	Conductor-4 COPPER		0.04	5.969e+07	1	0		
	InsulateLayer4-5 FR-4		0.1	0	4.5	0.02		
	Conductor-5 COPPER		0.018	5.969e+07	1	0		
	InsulateLayer5-6	FR-4	0.1	0	4.5	0.02		
	Conductor-6	COPPER	0.018	5.969e+07	1	0		
	InsulateLayer6-7	FR-4	0.1	0	4.5	0.02		
	Conductor-7	COPPER	0.04	5.969e+07	1	0		
	InsulateLayer7-8	ABF	0.075	0	4.5	0.02		

Stackup creation

Nets imported

The EM Setup Wizard

- Normally desired pins are selected
- Smart select selects net attached to pin
- Can select other pins on component with smart select
- Can propagate through series component

PCB EIVI Setup (0755)		_	
itatus				
Restored selected comp Run select "Nets" comm	onent pins and to select paths	and other net shapes	1	
nformation				
	Po	wer/Ground Nets	Select	ed Shape I
election				
Gelection General Options				
General Options	ver/ground nets	Select pins	only	
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Selection General Options Do not select pow Auto zoom after s Smart Select Options Select all compo Max pin count Deselect All	ver/ground nets selection nent pins Nets Undo	Components	only	Smart Selev Save

The Selected Pins and Nets

Create the Boundary for the Region for EM

Shape Simplification

Simplification Properties		×
Decimation Decimate paths Decimate circles Decimate cutouts Minimum points per circle Maximum deformation Maximum radius fillets Minimum path width or clearance	 ✓ ✓ ✓ 4 7.5 um 50 um 75 um 	Reset Defaults Reset Selected Show Mods Only
ОК	Cancel Help	Show Secondary

AWR ni.com/awr

Ports Have Been Added Automatically

These ports are called point ports

NATIONAL

81K unknowns

22K unknowns

Meshing Comparison

- Now have fewer meshes
 - Faster to simulate
 - Solve time for iterative solver is N^1.6
- They are more square and equilateral triangles fewer slivers
 - Better conditioned matrix easier to solve iteratively
- The mesh is not mirrored through planes
- Shape simplification reduces rounded corners and circular vias
- ... and –a lot of time was spent working on mesh algorithms!

The sub-circuit block looks like the layout

IND IDER1 DER1 DER DER T

Easy to place elements

The pin names are in the symbol

Conclusions

- New capabilities have improved layout import for verification flow
- The software directly can read ODB++ and IPC-2581 layout files
 - Layers, materials, pins and nets are included
- It is controlled by the PCB import wizard
- A new EM setup wizard enables:
 - Selection of the desired pins and nets
 - Creation of a cutout region of the layout automatically
 - Simplifies bends, vias, and pa.
 - Pin ports are automatically added without manual placement
- AXIEM simulator has been improved
 - Meshing has been improved for board layout geometries

Appendix: Point Ports

The Point Port

EDI CON 2018 Electronic Design Innovation Conference & Exhibition

- The point port is new to V14
- Problems it solves:
 - Automatically placed in center of pins (shapes)
 - V13 edge ports have to be manually placed. Edge of shape has to be selected.
 - Note: In V14 a point port can be manually added by selecting a shape and adding a port
 - Grounding set to implicit none
 - V13 the auto port usually places a strap down to the nearest metal
 - It might not be a ground
 - It would have to calibrated, which adds a lot of simulation time
 - Apoint port ground type can be changed to explicit ground to lower manually
 - It doesn't use a reference strap, as a normal edge port does

The Grounding Assumptions of Point Ports

- The grounding type of a point port is implicit
- There is no ground reference strap
- Advantage: this leads to low parasitics and no calibration is required
 - This assumption works better at lower frequencies with nearby power planes
- Advantage: the ground reference is automatically set
 - The ground reference is actually at infinity!
 - This sounds bad, but:
 - The designer is on a board at lower frequencies such that a ground is electrically close
 - Boards then have pairs of these ports together
 - Differential pair lines
 - Opposing ports for surface mount parts
 - The errors of one port tend to be canceled by the other

An Example Showing Point Port Issues

Open stub above a ground plane

3D view showing mesh

Close-up of the Mesh

Point port

- Ground at infinity
- The default setting

Edge Port – explicit ground to lower

- Ground at bottom of strap
- Autoports will probably pick this
- Strap parasitics calibrated out

Point port – ground to lower

- There is a "-" port on ground plane
- You can't see the "-" port
- Like a differential +/- pair
- Must be set manually

The Results

The point port fails badly

The edge port and the point port with reference to metal below are both good

- Phase shift from reference plane location difference
- The physics is completely different between the two ports
- The edge port has metal connecting the port to the ground plane
- The point ports has a hidden "-" port on the ground plane

A Through Line

8																			
	· · · · · · ·																		
	. MLIN																		
	ID=TL5				MLIN .						·M	IN ·							
	. W=1 mm				ID=TL1						-10	-TI 2							
	L=1 mm				W = 5 r	nm						-115							
DODT	MSUB-Lave	r01 Cu 01			1-5 mr	n					VV	=1 mr	n ·						
PORT	- WOOD-Layer				L-J IIII						·L=	1 mm							
P=1 · · ·					W20B=	Layeru	1_Cu_	01 .			M	SUB=L	Laye	r01_	Cu_	01			
Z=50 Ohm																			
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Two ports for each case

... and a circuit model

Results for the Thru Line – Return Loss

Point port not very goo.

At least it is inside the Smith chart

Edge port and model agree well

Point ports with explicit grounds are much better than the default

Differential Pairs – Open Circuit

Pair of lines

They are excited differentially

Differential Pairs – The Results

The point ports and edge ports agree reasonably well through 5 GHz

- The ports are close together
- They are excited out of phase
- Errors tend to cancel
- Really the same physics as explicit ground for the pin port with the negative port on the ground plane ... yet still close

Point Port Conclusion

- Advantages
 - They are placed automatically
 - They work well enough for low frequencies (close-by ground plane)
 - They work well with differential pairs and small surface-mount gaps depending on the model
- Disadvantages
 - Higher frequencies thicker boards not as accurate
 - Reference plane is the middle of the shape
 - Not as accurate as de-embedded (calibrated) edge ports
- To Make More Accurate
 - Go into Edit > Ports, and change implicit ground type to explicit below
 - Must have ground plane below ports!

